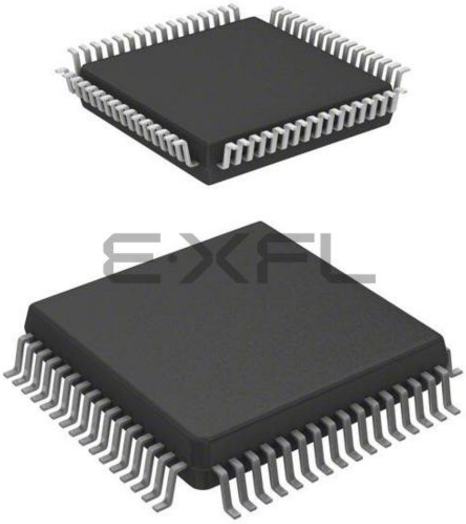

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300H
Core Size	16-Bit
Speed	20MHz
Connectivity	CANbus, SCI, SSU
Peripherals	PWM, WDT
Number of I/O	45
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	64-BQFP
Supplier Device Package	64-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df36034hv

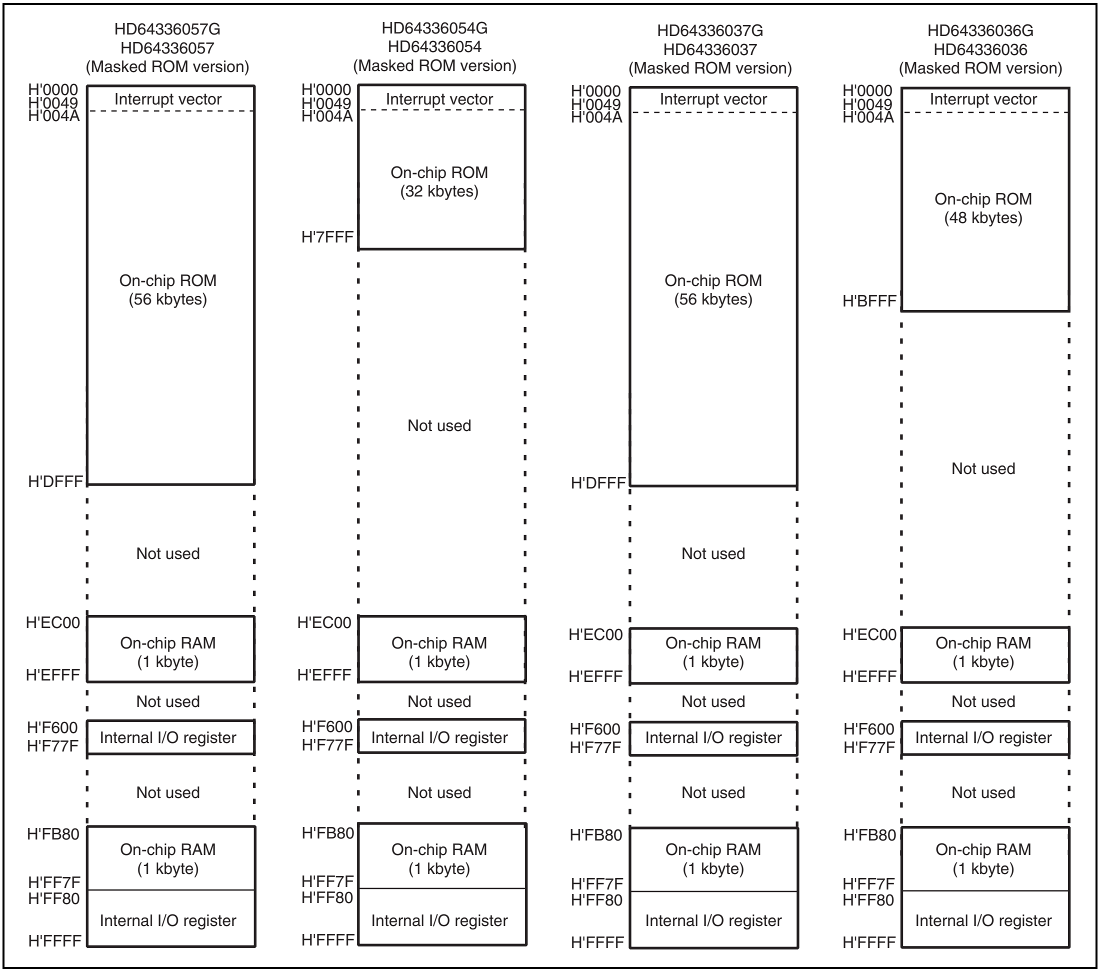


Figure 2.1 Memory Map (2)

2.6.2 On-Chip Peripheral Modules

On-chip peripheral modules are accessed in two states, three states, or four states. The data bus width is 8 bits or 16 bits depending on the register. For description on the data bus width and number of accessing states of each register, refer to section 21.1, Register Addresses (Address Order). Registers with 16-bit data bus width can be accessed by word size only. Registers with 8-bit data bus width can be accessed by byte or word size. When a register with 8-bit data bus width is accessed by word size, a bus cycle occurs twice. In two-state access, the operation timing is the same as that for on-chip memory. Figure 2.10 shows the operation timing in the case of three-state access to an on-chip peripheral module. In four-state access, the operation timing is such that a wait cycle is inserted between the T_2 and T_3 states.

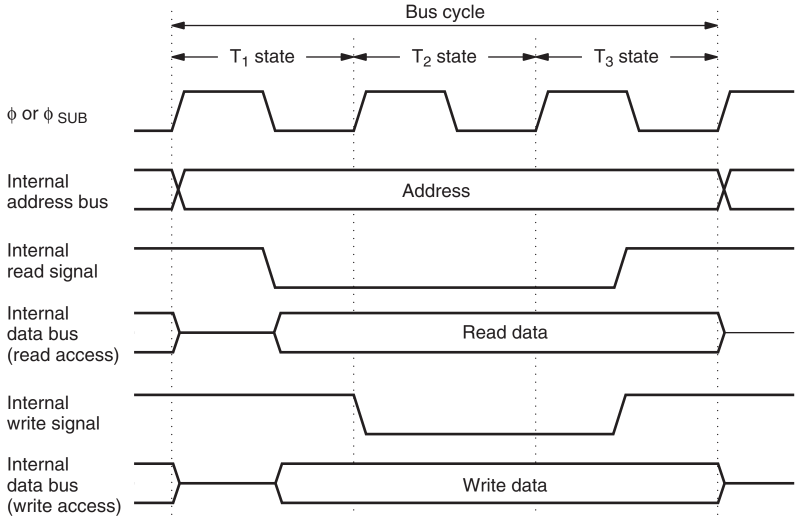


Figure 2.10 On-Chip Peripheral Module Access Cycle (3-State Access)

Bit	Bit Name	Initial Value	R/W	Description
2	PV	0	R/W	Program-Verify When this bit is set to 1, the flash memory changes to program-verify mode. When it is cleared to 0, program-verify mode is cancelled.
1	E	0	R/W	Erase When this bit is set to 1 while SWE = 1 and ESU = 1, the flash memory changes to erase mode. When it is cleared to 0, erase mode is cancelled.
0	P	0	R/W	Program When this bit is set to 1 while SWE = 1 and PSU = 1, the flash memory changes to program mode. When it is cleared to 0, program mode is cancelled.

7.2.2 Flash Memory Control Register 2 (FLMCR2)

FLMCR2 is a register that displays the state of flash memory programming/erasing. FLMCR2 is a read-only register, and should not be written to.

Bit	Bit Name	Initial Value	R/W	Description
7	FLER	0	R	Flash Memory Error Indicates that an error has occurred during an operation on flash memory (programming or erasing). When FLER is set to 1, flash memory goes to the error-protection state. See section 7.5.3, Error Protection, for details.
6 to 0	—	All 0	—	Reserved These bits are always read as 0.

12.3.8 General Registers A, B, C, and D (GRA, GRB, GRC, and GRD)

GR are 16-bit registers. Timer Z has eight general registers (GR), four for each channel. The GR registers are dual function 16-bit readable/writable registers, functioning as either output compare or input capture registers. Functions can be switched by TIORA and TIORC.

The values in GR and TCNT are constantly compared with each other when the GR registers are used as output compare registers. When the both values match, the IMFA to IMFD flags in TSR are set to 1. Compare match outputs can be selected by TIORA and TIORC.

When the GR registers are used as input capture registers, the TCNT value is stored after detecting external signals. At this point, IMFA to IMFD flags in the corresponding TSR are set to 1. Detection edges for input capture signals can be selected by TIORA and TIORC.

When PWM mode, complementary PWM mode, or reset synchronous PWM mode is selected, the values in TIORA and TIORC are ignored. Upon reset, the GR registers are set as output compare registers (no output) and initialized to H'FFFF. The GR registers cannot be accessed in 8-bit units; they must always be accessed as a 16-bit unit.

Examples of Waveform Output Operation: Figure 12.13 shows an example of 0 output/1 output.

In this example, TCNT has been designated as a free-running counter, and settings have been made such that 0 is output by compare match A, and 1 is output by compare match B. When the set level and the pin level coincide, the pin level does not change.

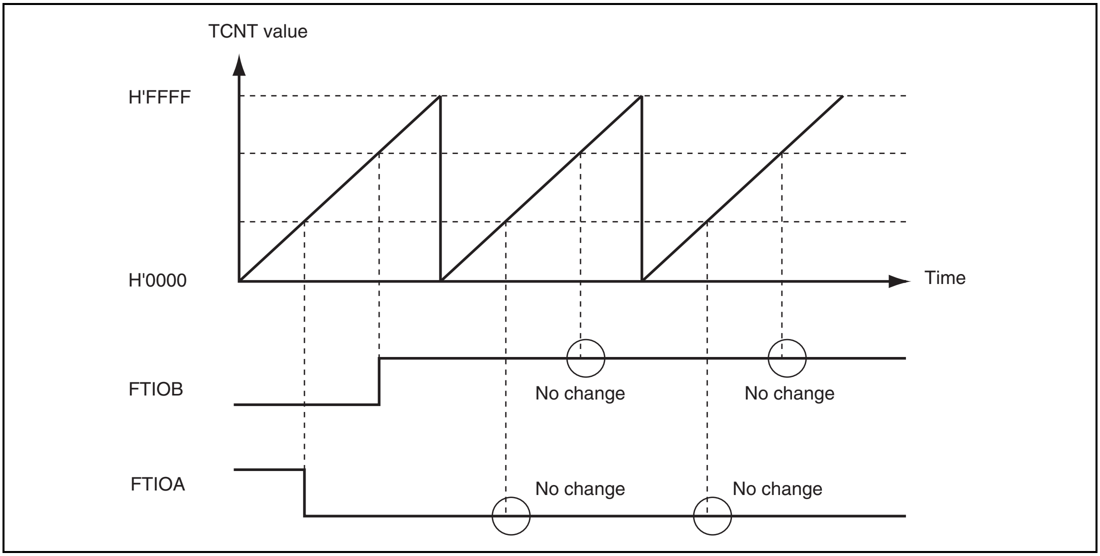


Figure 12.13 Example of 0 Output/1 Output Operation

TOCR has been set to H'06. Compare match B0 and compare match C0 are used. The FTIOB0 pin is in the 1 output state, and is set to the toggle output or the 0 output by compare match B0.
When BCLR#2, @TOCR is executed to clear the TOC0 bit (the FTIOC0 signal is low) and compare match B0 occurs at the same timing as shown below, the H'02 writing to TOCR has priority and compare match B0 does not drive the FTIOB0 signal low; the FTIOB0 signal remains high.

Bit	7	6	5	4	3	2	1	0
TOCR	TOD1	TOC1	TOB1	TOA1	TOD0	TOC0	TOB0	TOA0
Set value	0	0	0	0	0	1	1	0

BCLR#2, @TOCR
(1) TOCR read operation: Read H'06
(2) Modify operation: Modify H'06 to H'02
(3) Write operation to TOCR: Write H'02

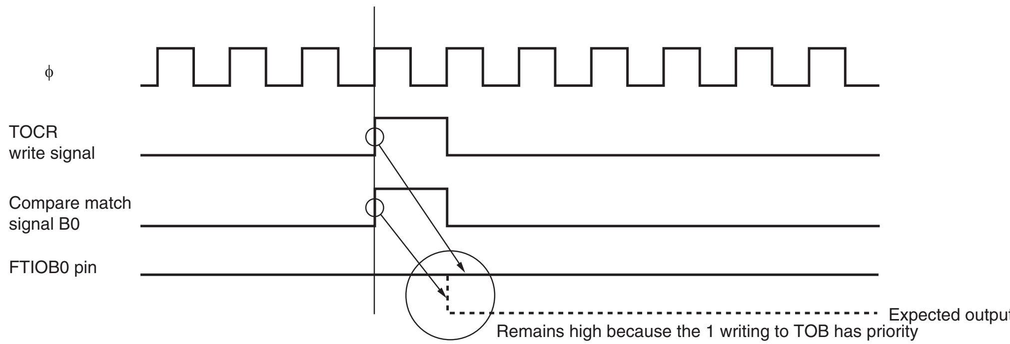


Figure 12.59 When Compare Match and Bit Manipulation Instruction to TOCR Occur at the Same Timing

- Break detection: Break can be detected by reading the RXD pin level directly in the case of a framing error

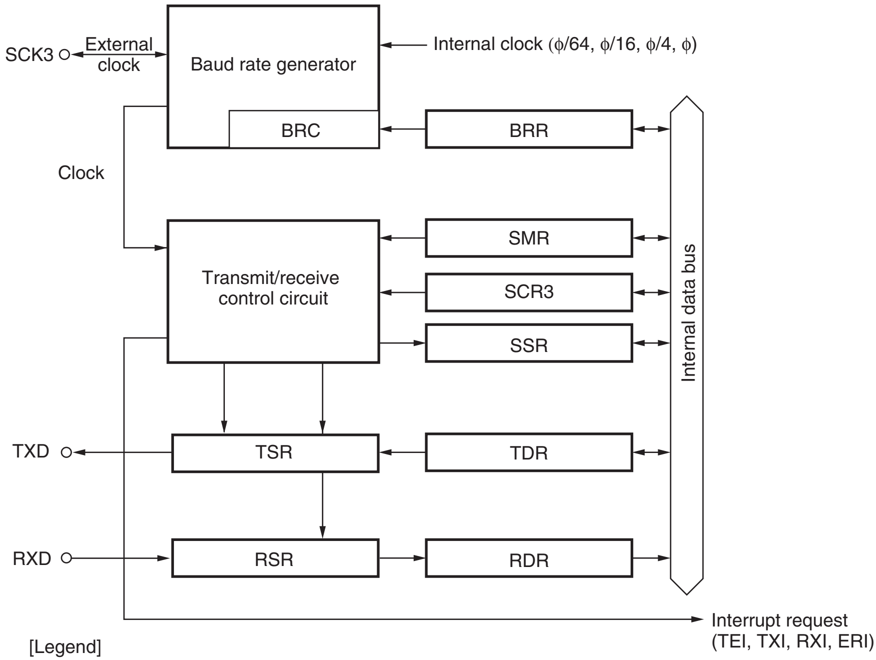
Clocked synchronous mode

- Data length: 8 bits
- Receive error detection: Overrun errors

Table 14.1 Channel Configuration

Channel	Abbreviation	Pin	Register	Register Address
Channel 1*[1]	SCI3	SCK3 RXD TXD	SMR	H'FFA8
			BRR	H'FFA9
			SCR3	H'FFAA
			TDR	H'FFAB
			SSR	H'FFAC
			RDR	H'FFAD
			RSR	—
			TSR	—
Channel 2*[2]	SCI3_2	SCK3_2 RXD_2 TXD_2	SMR_2	H'F740
			BRR_2	H'F741
			SCR3_2	H'F742
			TDR_2	H'F743
			SSR_2	H'F744
			RDR_2	H'F745
			RSR_2	—
			TSR_2	—

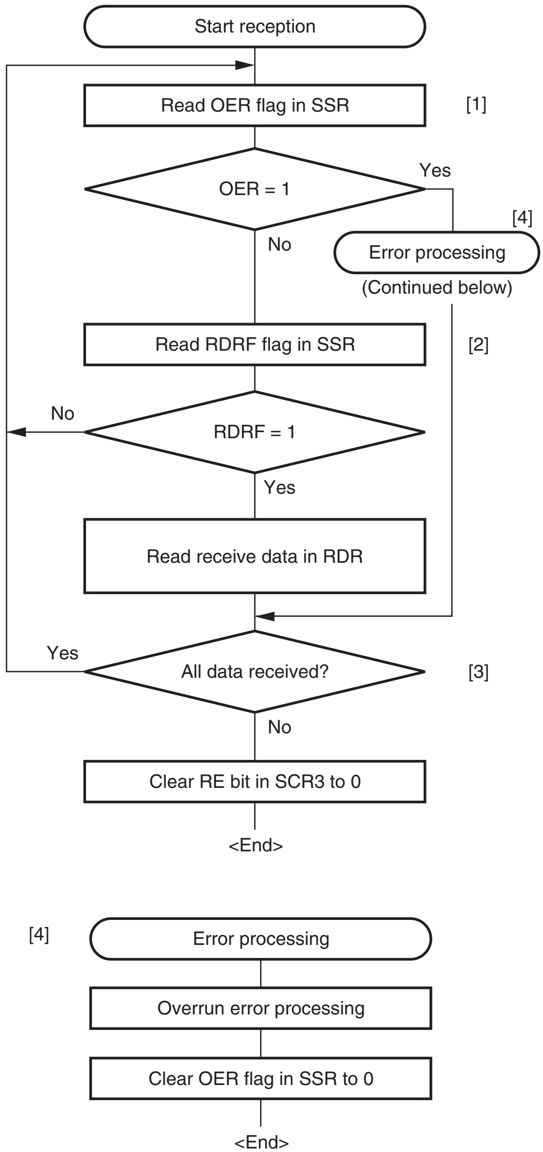
Notes: 1. Channel 1 is used in on-board programming mode by boot mode.
2. The H8/36037 Group does not have the channel 2.



[Legend]

RSR:	Receive shift register
RDR:	Receive data register
TSR:	Transmit shift register
TDR:	Transmit data register
SMR:	Serial mode register
SCR3:	Serial control register 3
SSR:	Serial status register
BRR:	Bit rate register
BRC:	Bit rate counter

Figure 14.1 Block Diagram of SCI3



[1] Read the OER flag in SSR to determine if there is an error. If an overrun error has occurred, execute overrun error processing.

[2] Read SSR and check that the RDRF flag is set to 1, then read the receive data in RDR. When data is read from RDR, the RDRF flag is automatically cleared to 0.

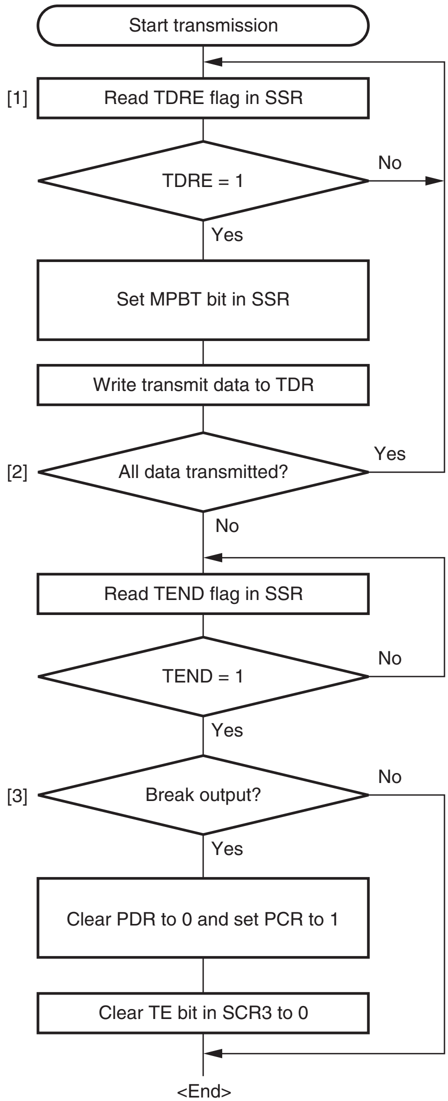
[3] To continue serial reception, before the MSB (bit 7) of the current frame is received, reading the RDRF flag and reading RDR should be finished. When data is read from RDR, the RDRF flag is automatically cleared to 0.

[4] If an overrun error occurs, read the OER flag in SSR, and after performing the appropriate error processing, clear the OER flag to 0. Reception cannot be resumed if the OER flag is set to 1.

Figure 14.13 Sample Serial Reception Flowchart (Clocked Synchronous Mode)

14.5.5 Simultaneous Serial Data Transmission and Reception

Figure 14.14 shows a sample flowchart for simultaneous serial transmit and receive operations. The following procedure should be used for simultaneous serial data transmit and receive operations. To switch from transmit mode to simultaneous transmit and receive mode, after checking that the SCI3 has finished transmission and the TDRE and TEND flags are set to 1, clear TE to 0. Then simultaneously set TE and RE to 1 with a single instruction. To switch from receive mode to simultaneous transmit and receive mode, after checking that the SCI3 has finished reception, clear RE to 0. Then after checking that the RDRF and receive error flags (OER, FER, and PER) are cleared to 0, simultaneously set TE and RE to 1 with a single instruction.



[1] Read SSR and check that the TDRE flag is set to 1, set the MPBT bit in SSR to 0 or 1, then write transmit data to TDR. When data is written to TDR, the TDRE flag is automatically cleared to 0.

[2] To continue serial transmission, be sure to read 1 from the TDRE flag to confirm that writing is possible, then write data to TDR. When data is written to TDR, the TDRE flag is automatically cleared to 0.

[3] To output a break in serial transmission, set the port PCR to 1, clear PDR to 0, then clear the TE bit in SCR3 to 0.

Figure 14.16 Sample Multiprocessor Serial Transmission Flowchart

14.6.2 Multiprocessor Serial Data Reception

Figure 14.17 shows a sample flowchart for multiprocessor serial data reception. If the MPIE bit in SCR3 is set to 1, data is skipped until data with a 1 multiprocessor bit is sent. On receiving data with a 1 multiprocessor bit, the receive data is transferred to RDR. An RXI interrupt request is

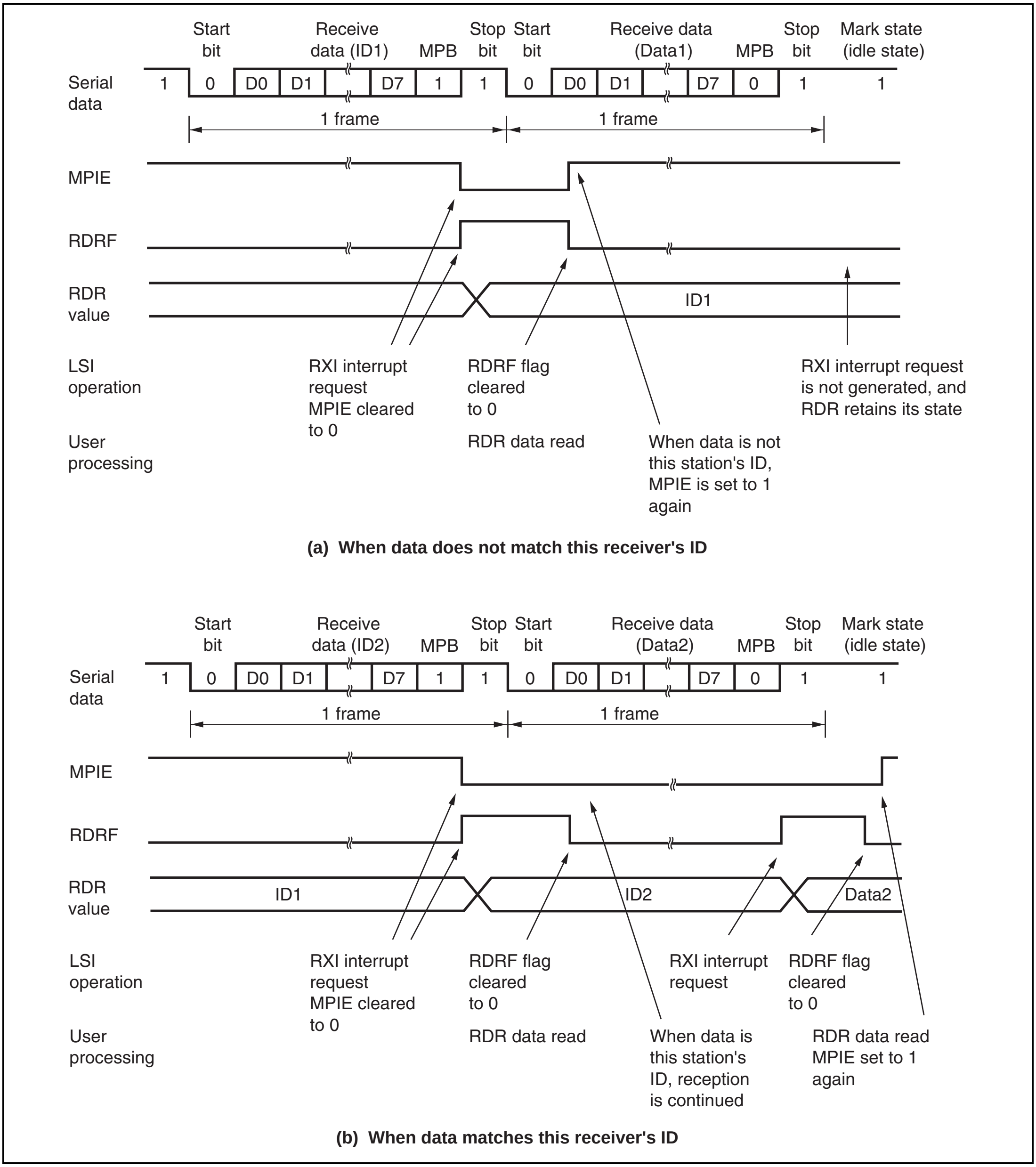


Figure 14.18 Example of SCI3 Reception Using Multiprocessor Format (Example with 8-Bit Data, Multiprocessor Bit, One Stop Bit)

14.8 Usage Notes

14.8.1 Break Detection and Processing

When framing error detection is performed, a break can be detected by reading the RXD pin value directly. In a break, the input from the RXD pin becomes all 0s, setting the FER flag, and possibly the PER flag. Note that as the SCI3 continues the receive operation after receiving a break, even if the FER flag is cleared to 0, it will be set to 1 again.

14.8.2 Mark State and Break Sending

When TE is 0, the TXD pin is used as an I/O port whose direction (input or output) and level are determined by PCR and PDR. This can be used to set the TXD pin to mark state (high level) or send a break during serial data transmission. To maintain the communication line at mark state until TE is set to 1, set both PCR and PDR to 1. As TE is cleared to 0 at this point, the TXD pin becomes an I/O port, and 1 is output from the TXD pin. To send a break during serial transmission, first set PCR to 1 and clear PDR to 0, and then clear TE to 0. When TE is cleared to 0, the transmitter is initialized regardless of the current transmission state, the TXD pin becomes an I/O port, and 0 is output from the TXD pin.

14.8.3 Receive Error Flags and Transmit Operations (Clocked Synchronous Mode Only)

Transmission cannot be started when a receive error flag (OER, PER, or FER) is set to 1, even if the TDRE flag is cleared to 0. Be sure to clear the receive error flags to 0 before starting transmission. Note also that receive error flags cannot be cleared to 0 even if the RE bit is cleared to 0.

15.3.14 TinyCAN Interrupt Registers 0, 1 (TCIRR0, TCIRR1)

TCIRR is a status flag for each interrupt source.

- TCIRR0

Bit	Bit Name	Initial Value	R/W	Description
7	OVLI	0	R/(W)*	Overload Frame Transmit Interrupt Flag Status flag indicating that the TinyCAN has transmitted an overload frame. [Setting condition] When an overload frame is transmitted [Clearing condition] When 1 is written to this bit
6	BOFI	0	R/(W)*	Bus Off Interrupt Flag Status flag indicating the bus off state caused by the TEC or recovery from the bus off state to the error-active state. [Setting condition] When TEC ≥ 256 or when 11 bits are received for 128 times in the bus off state [Clearing condition] When 1 is written to this bit
5	EPI	0	R/(W)*	Error Passive Interrupt Flag Status flag indicating the error-passive state caused by REC or TEC. [Setting condition] When TEC ≥ 128 or REC ≥ 128 [Clearing condition] When 1 is written to this bit
4	ROWI	0	R/(W)*	Receive Overload Warning Interrupt Flag Status flag indicating the error warning state caused by REC. [Setting condition] When REC ≥ 96 [Clearing condition] When 1 is written to this bit

15.4.2 Local Acceptance Filter Mask (LAFMHn1, LAFMHn0, LAFMLn1, LAFMLn0 [n = 0 to 3])

LAFM consists of four registers for one Mailbox. LAFM filters mask of bit-unit comparison between the message identifier of RXn (n = 0 to 3) stored in the receive Mailbox and the receive message identifier. Since LAFM is in RAM, initial values are undefined after power-on. Be sure to initialize each bit by writing 0 or 1.

Register Name	Bit	Bit Name	R/W	Description
LAFMLn1 (n = 0 to 3)	7 to 0	LAFMLn7 to LAFMLn0	R/W	Filter mask for bits 7 to 0 of the extended identifier. 0: Receive message is stored in RXn because the RXn message identifier bits match the receive message identifier bits 1: Receive message is stored in RXn regardless of whether the RXn message identifier bits match the receive message identifier bits
LAFMLn0 (n = 0 to 3)	7 to 0	LAFMLn15 to LAFMLn8	R/W	Filter mask for bits 15 to 8 of the extended identifier. 0: Receive message is stored in RXn because the RXn message identifier bits match the receive message identifier bits 1: Receive message is stored in RXn regardless of whether the RXn message identifier bits match the receive message identifier bits
LAFMHn1 (n = 0 to 3)	7 to 5	LAFMHn7 to LAFMHn5	R/W	Filter mask for bits 2 to 0 of the standard identifier. 0: Receive message is stored in RXn because the RXn message identifier bits match the receive message identifier bits 1: Receive message is stored in RXn regardless of whether the RXn message identifier bits match the receive message identifier bits

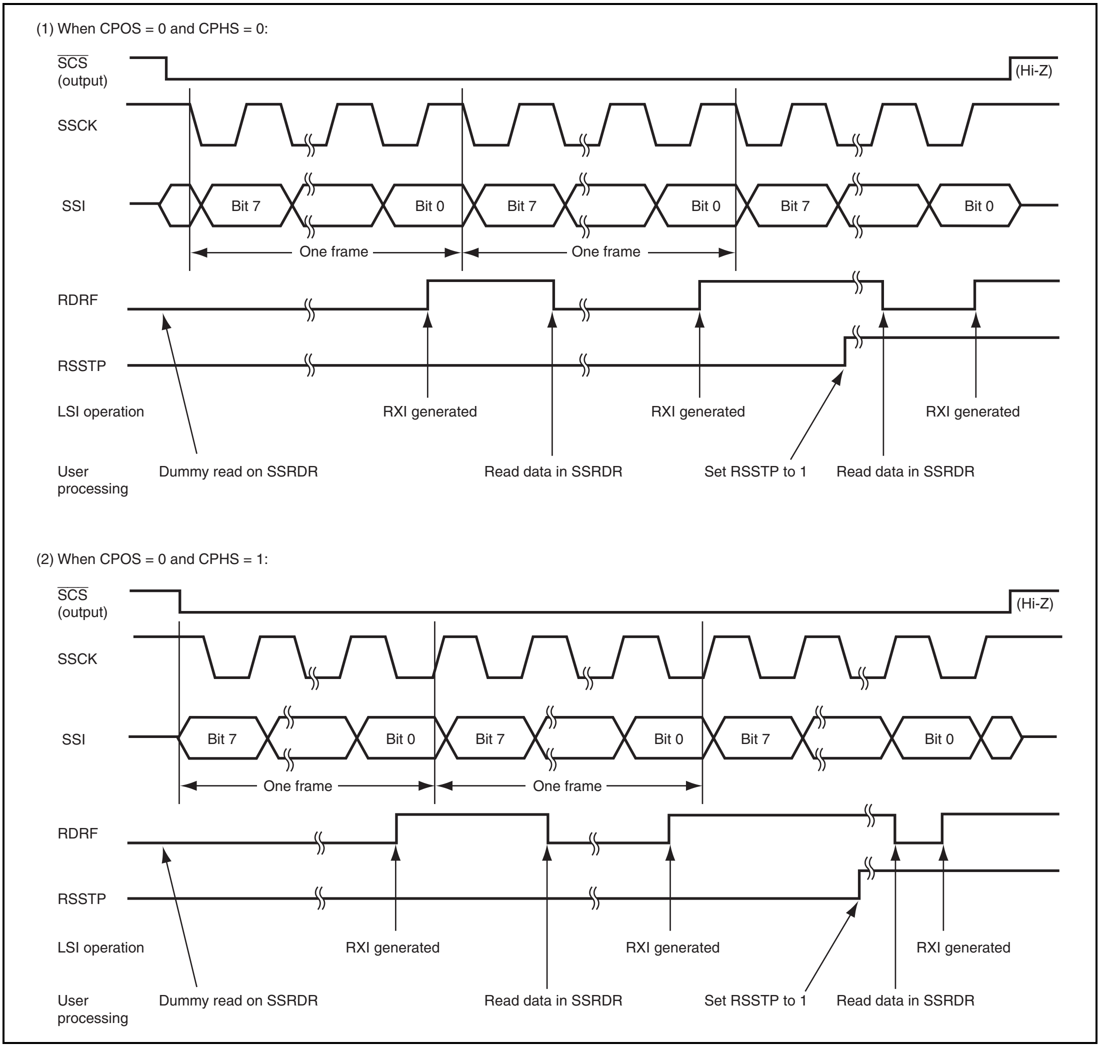


Figure 16.12 Example of Operation in Data Reception (MSS = 1)

Register Name	Abbre-viation	Bit No	Address	Module Name	Data Bus Width	Access State
—	—	—	H'FFED to H'FFEF	—	—	—
System control register 1	SYSCR1	8	H'FFF0	Power-down	8	2
System control register 2	SYSCR2	8	H'FFF1	Power-down	8	2
Interrupt edge select register 1	IEGR1	8	H'FFF2	Interrupt	8	2
Interrupt edge select register 2	IEGR2	8	H'FFF3	Interrupt	8	2
Interrupt enable register 1	IENR1	8	H'FFF4	Interrupt	8	2
Interrupt enable register 2	IENR2	8	H'FFF5	Interrupt	8	2
Interrupt flag register 1	IRR1	8	H'FFF6	Interrupt	8	2
Interrupt flag register 2	IRR2	8	H'FFF7	Interrupt	8	2
Wakeup interrupt flag register	IWPR	8	H'FFF8	Interrupt	8	2
Module standby control register 1	MSTCR1	8	H'FFF9	Power-down	8	2
Module standby control register 2	MSTCR2	8	H'FFFA	Power-down	8	2
—	—	—	H'FFFB to H'FFFF	—	—	—

Notes: 1. LVDC: Low-voltage detection circuits (optional)
2. WDT: Watchdog timer
3. The H8/36037 Group does not have the SCI3_2.

Register Abbreviation	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name
PUCR1	PUCR17	PUCR16	PUCR15	PUCR14	—	PUCR12	PUCR11	PUCR10	I/O port
PUCR5	—	—	PUCR55	PUCR54	PUCR53	PUCR52	PUCR51	PUCR50	
PDR1	P17	P16	P15	P14	—	P12	P11	P10	
PDR2	—	—	—	P24	P23	P22	P21	P20	
PDR5	P57	P56	P55	P54	P53	P52	P51	P50	
PDR6	P67	P66	P65	P64	P63	P62	P61	P60	
PDR7	—	P76	P75	P74	—	P72	P71	P70	
PDR8	P87	P86	P85	—	—	—	—	—	
PDR9	P97	P96	P95	P94	P93	P92	P91	P90	
PDRB	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	
PMR1	IRQ3	IRQ2	IRQ1	IRQ0	TXD2*4	—	TXD	—	
PMR5	POF57	POF56	WKP5	WKP4	WKP3	WKP2	WKP1	WKP0	
PMR3	—	—	—	POF24	POF23	—	—	—	
PCR1	PCR17	PCR16	PCR15	PCR14	—	PCR12	PCR11	PCR10	
PCR2	—	—	—	PCR24	PCR23	PCR22	PCR21	PCR20	
PCR5	PCR57	PCR56	PCR55	PCR54	PCR53	PCR52	PCR51	PCR50	
PCR6	PCR67	PCR66	PCR65	PCR64	PCR63	PCR62	PCR61	PCR60	
PCR7	—	PCR76	PCR75	PCR74	—	PCR72	PCR71	PCR70	
PCR8	PCR87	PCR86	PCR85	—	—	—	—	—	
PCR9	PCR97	PCR96	PCR95	PCR94	PCR93	PCR92	PCR91	PCR90	
SYSCR1	SSBY	STS2	STS1	STS0	—	—	—	—	Power-down
SYSCR2	SMSEL	LSON	DTON	MA2	MA1	MA0	SA1	SA0	
IEGR1	NMIEG	—	—	—	IEG3	IEG2	IEG1	IEG0	Interrupt
IEGR2	—	—	WPEG5	WPEG4	WPEG3	WPEG2	WPEG1	WPEG0	
IENR1	IENDT	—	IENWP	—	IEN3	IEN2	IEN1	IEN0	
IENR2	—	—	IENTB1	—	—	—	—	—	
IRR1	IRRDT	—	—	—	IRRI3	IRRI2	IRRI1	IRRI0	
IRR2	—	—	IRRTB1	—	—	—	—	—	
IWPR	—	—	IWPF5	IWPF4	IWPF3	IWPF2	IWPF1	IWPF0	
MSTCR1	—	—	MSTS3	MSTAD	MSTWD	—	MSTTV	—	Power-down
MSTCR2	MSTS3_2*4	—	—	MSTTB1	—	—	MSTTZ	—	

22.3.2 DC Characteristics

Table 22.12 DC Characteristics (1)

V_{CC} = 2.7 to 5.5 V, V_{SS} = 0.0 V, T_a = –20 to +75°C (regular specifications) or T_a = –40 to +85°C (wide-range specifications), unless otherwise indicated.

				Values				
Item	**Symbol**	**Applicable Pins**	**Test Condition**	**Min.**	**Typ.**	**Max.**	**Unit**	**Notes**
Input high voltage	V_{IH}	$\overline{\text{RES}}$, $\overline{\text{NMI}}$, $\overline{\text{WKP0}}$ to $\overline{\text{WKP5}}$, $\overline{\text{IRQ0}}$ to $\overline{\text{IRQ3}}$, $\overline{\text{ADTRG}}$,TMRIV, TMCIV, FTIOA0 to FTIOD0, FTIOA1 to FTIOD1, SCK3, SCK3_2*[1], $\overline{\text{SCS}}$, SSCK, TRGV, TMIB1	V_{CC} = 4.0 to 5.5 V	$V_{CC} \times 0.8$	—	$V_{CC} + 0.3$	V	
				$V_{CC} \times 0.9$	—	$V_{CC} + 0.3$		
		RXD, RXD_2*[1], SSI, SSO, HRXD, P10 to P12, P14 to P17, P20 to P24, P50 to P57, P60 to P67, P70 to P72, P74 to P76, P85 to P87 P90 to P97	V_{CC} = 4.0 to 5.5 V	$V_{CC} \times 0.7$	—	$V_{CC} + 0.3$	V	
				$V_{CC} \times 0.8$	—	$V_{CC} + 0.3$		
	V_{IH}	PB0 to PB7	V_{CC} = 4.0 to 5.5 V	$V_{CC} \times 0.7$	—	$AV_{CC} + 0.3$	V	
				$V_{CC} \times 0.8$	—	$AV_{CC} + 0.3$		
		OSC1	V_{CC} = 4.0 to 5.5 V	$V_{CC} - 0.5$	—	$V_{CC} + 0.3$	V	
				$V_{CC} - 0.3$	—	$V_{CC} + 0.3$		

Instruction	Mnemonic	Instruction Fetch I	Branch Addr. Read J	Stack Operation K	Byte Data Access L	Word Data Access M	Internal Operation N
ROTXR	ROTXR.B Rd	1					
	ROTXR.W Rd	1					
	ROTXR.L ERd	1					
RTE	RTE	2		2			2
RTS	RTS	2		1			2
SHAL	SHAL.B Rd	1					
	SHAL.W Rd	1					
	SHAL.L ERd	1					
SHAR	SHAR.B Rd	1					
	SHAR.W Rd	1					
	SHAR.L ERd	1					
SHLL	SHLL.B Rd	1					
	SHLL.W Rd	1					
	SHLL.L ERd	1					
SHLR	SHLR.B Rd	1					
	SHLR.W Rd	1					
	SHLR.L ERd	1					
SLEEP	SLEEP	1					
STC	STC CCR, Rd	1					
	STC CCR, @ERd	2				1	
	STC CCR, @(d:16,ERd)	3				1	
	STC CCR, @(d:24,ERd)	5				1	
	STC CCR,@-ERd	2				1	2
	STC CCR, @aa:16	3				1	
	STC CCR, @aa:24	4				1	
SUB	SUB.B Rs, Rd	1					
	SUB.W #xx:16, Rd	2					
	SUB.W Rs, Rd	1					
	SUB.L #xx:32, ERd	3					
	SUB.L ERs, ERd	1					
SUBS	SUBS #1/2/4, ERd	1					