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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300H
Core Size	16-Bit
Speed	20MHz
Connectivity	CANbus, SCI, SSU
Peripherals	PWM, WDT
Number of I/O	45
Program Memory Size	56KB (56K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df36037fpv

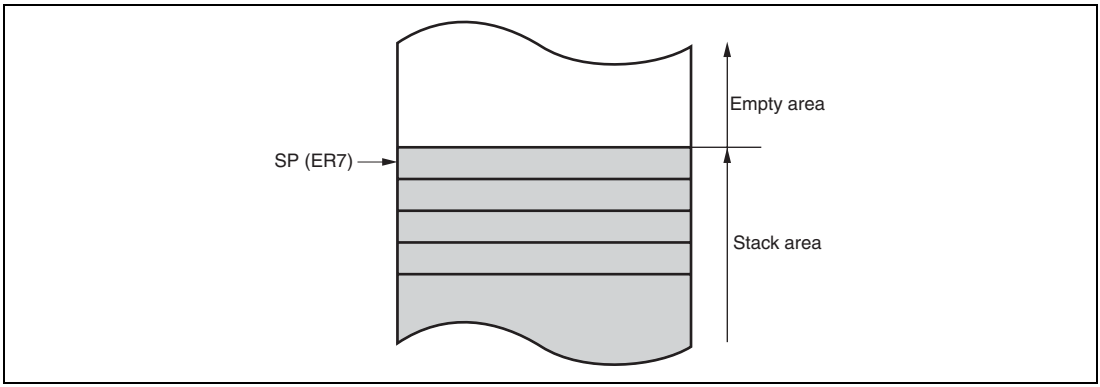

Figure 2.4 Relationship between Stack Pointer and Stack Area

2.2.2 Program Counter (PC)

This 24-bit counter indicates the address of the next instruction the CPU will execute. The length of all CPU instructions is 2 bytes (one word), so the least significant PC bit is ignored. (When an instruction is fetched, the least significant PC bit is regarded as 0). The PC is initialized when the start address is loaded by the vector address generated during reset exception-handling sequence.

2.2.3 Condition-Code Register (CCR)

This 8-bit register contains internal CPU status information, including an interrupt mask bit (I) and half-carry (H), negative (N), zero (Z), overflow (V), and carry (C) flags. The I bit is initialized to 1 by reset exception-handling sequence, but other bits are not initialized.

Some instructions leave flag bits unchanged. Operations can be performed on the CCR bits by the LDC, STC, ANDC, ORC, and XORC instructions. The N, Z, V, and C flags are used as branching conditions for conditional branch (Bcc) instructions.

For the action of each instruction on the flag bits, see appendix A.1, Instruction List.

Table 2.6 Bit Manipulation Instructions (2)

Instruction	Size*	Function
BXOR	B	C ⊕ (<bit-No.> of <EAd>) → C XORs the carry flag with a specified bit in a general register or memory operand and stores the result in the carry flag.
BIXOR	B	C ⊕ ¬ (<bit-No.> of <EAd>) → C XORs the carry flag with the inverse of a specified bit in a general register or memory operand and stores the result in the carry flag. The bit number is specified by 3-bit immediate data.
BLD	B	(<bit-No.> of <EAd>) → C Transfers a specified bit in a general register or memory operand to the carry flag.
BILD	B	¬ (<bit-No.> of <EAd>) → C Transfers the inverse of a specified bit in a general register or memory operand to the carry flag. The bit number is specified by 3-bit immediate data.
BST	B	C → (<bit-No.> of <EAd>) Transfers the carry flag value to a specified bit in a general register or memory operand.
BIST	B	¬ C → (<bit-No.> of <EAd>) Transfers the inverse of the carry flag value to a specified bit in a general register or memory operand. The bit number is specified by 3-bit immediate data.

[Legend]

B: Byte

Note: * Refers to the operand size.

2.7 CPU States

There are four CPU states: the reset state, program execution state, program halt state, and exception-handling state. The program execution state includes active mode and subactive mode. For the program halt state, there are a sleep mode, standby mode, and sub-sleep mode. These states are shown in figure 2.11. Figure 2.12 shows the state transitions. For details on program execution state and program halt state, refer to section 6, Power-Down Modes. For details on exception processing, refer to section 3, Exception Handling.

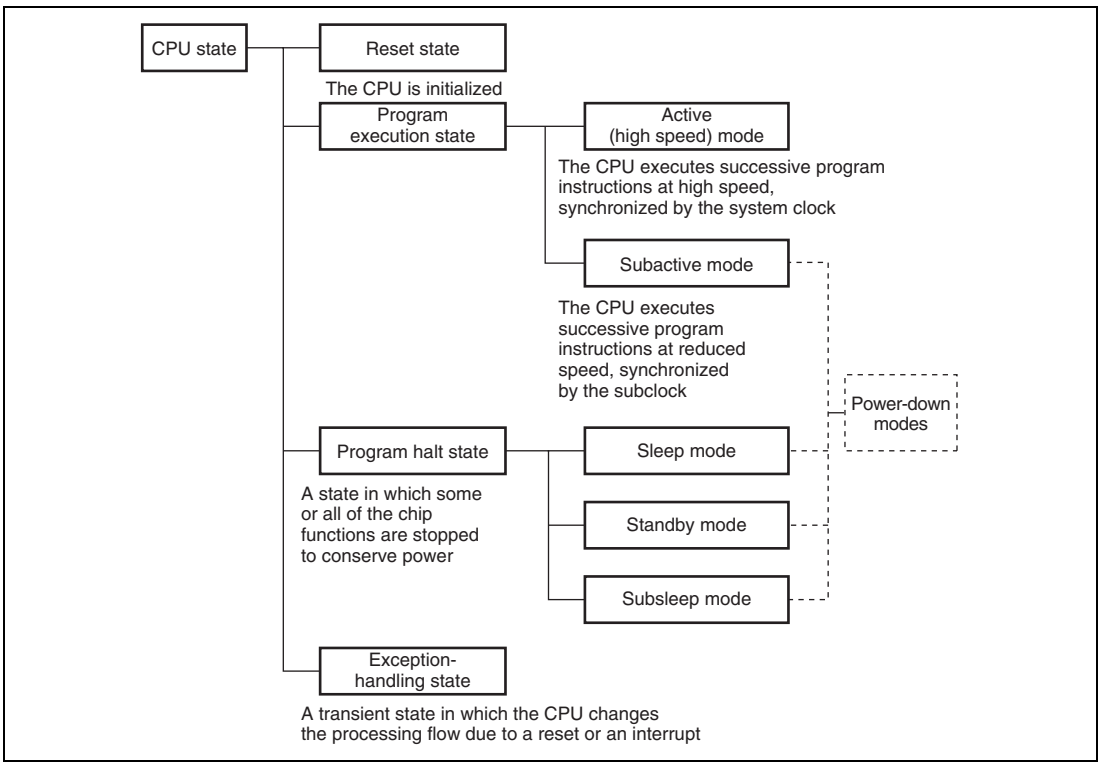

Figure 2.11 CPU Operation States

2.8 Usage Notes

2.8.1 Notes on Data Access to Empty Areas

The address space of this LSI includes empty areas in addition to the ROM, RAM, and on-chip I/O registers areas available to the user. When data is transferred from CPU to empty areas, the transferred data will be lost. This action may also cause the CPU to malfunction. When data is transferred from an empty area to CPU, the contents of the data cannot be guaranteed.

2.8.2 EEPMOV Instruction

EEPMOV is a block-transfer instruction and transfers the byte size of data indicated by R4L, which starts from the address indicated by R5, to the address indicated by R6. Set R4L and R6 so that the end address of the destination address (value of R6 + R4L) does not exceed H'FFFF (the value of R6 must not change from H'FFFF to H'0000 during execution).

2.8.3 Bit-Manipulation Instruction

The BSET, BCLR, BNOT, BST, and BIST instructions read data from the specified address in byte units, manipulate the data of the target bit, and write data to the same address again in byte units. Special care is required when using these instructions in cases where two registers are assigned to the same address, or when a bit is directly manipulated for a port or a register containing a write-only bit, because this may rewrite data of a bit other than the bit to be manipulated.

(1) Bit manipulation for two registers assigned to the same address

Example 1: Bit manipulation for the timer load register and timer counter

(Applicable for timer B1 in the H8/36057 Group and H8/36037 Group.)

Figure 2.13 shows an example of a timer in which two timer registers are assigned to the same address. When a bit-manipulation instruction accesses the timer load register and timer counter of a reloadable timer, since these two registers share the same address, the following operations takes place.

1. Data is read in byte units.
2. The CPU sets or resets the bit to be manipulated with the bit-manipulation instruction.
3. The written data is written again in byte units to the timer load register.

When the address break is specified in the data read cycle

Register setting
- ABRKCR = H'A0
- BAR = H'025A

Program

```
  0258  NOP
  025A  NOP
* 025C  MOV.W @H'025A,R0
  0260  NOP
  0262  NOP
    :     :
```

Underline indicates the address to be stacked.

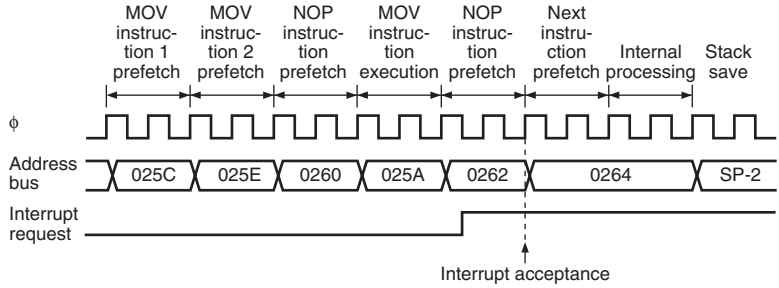

Figure 4.2 Address Break Interrupt Operation Example (2)

9.3.4 Port Pull-Up Control Register 5 (PUCR5)

PUCR5 controls the pull-up MOS in bit units of the pins set as the input ports.

Bit	Bit Name	Initial Value	R/W	Description
7, 6	—	All 0	—	Reserved These bits are always read as 0.
5	PUCR55	0	R/W	Only bits for which PCR5 is cleared are valid. The pull-up MOS of the corresponding pins enters the on-state when these bits are set to 1, while they enter the off-state when these bits are cleared to 0.
4	PUCR54	0	R/W	
3	PUCR53	0	R/W	
2	PUCR52	0	R/W	
1	PUCR51	0	R/W	
0	PUCR50	0	R/W	

9.3.5 Pin Functions

The correspondence between the register specification and the port functions is shown below.

- P57 pin

Register	PCR5	
Bit Name	**PCR57**	**Pin Function**
Setting Value	0	P57 input pin
	1	P57 output pin

- P56 pin

Register	PCR5	
Bit Name	**PCR56**	**Pin Function**
Setting Value	0	P56 input pin
	1	P56 output pin

- P60/FTIOA0 pin

Register	TOER	TFCR	TFCR	TIORA0	PCR6	
Bit Name	EA0	CMD1, CMD0	STCLK	IOA2 to IOA0	PCR60	Pin Function
Setting Value	1	XX	X	000 or 1XX	0	P60 input/FTIOA0 input pin
					1	P60 output pin
	0	00	0	001 or 01X	X	FTIOA0 output pin

[Legend]
X: Don't care.

9.5 Port 7

Port 7 is a general I/O port also functioning as a timer V I/O pin and SCI3_2 I/O pin. Each pin of the port 7 is shown in figure 9.5. The register settings of the timer V and SCI3_2* have priority for functions of the pins for both uses.

Note: * The H8/36037 Group does not have the SCI3_2.

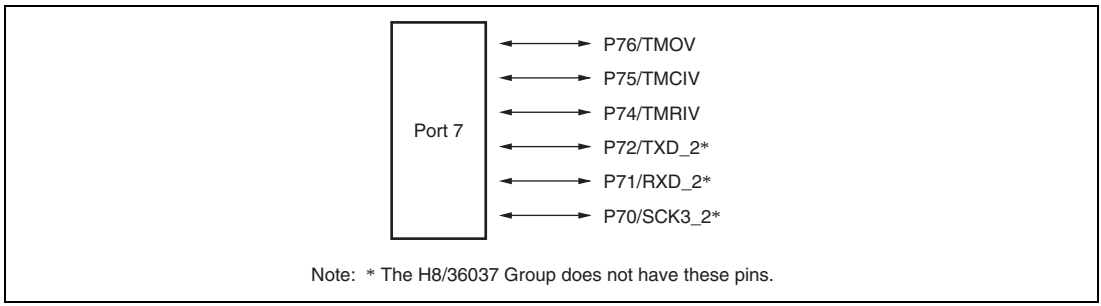

Figure 9.5 Port 7 Pin Configuration

Port 7 has the following registers.

- Port control register 7 (PCR7)
- Port data register 7 (PDR7)

10.3 Register Descriptions

The timer B1 has the following registers.

- Timer mode register B1 (TMB1)
- Timer counter B1 (TCB1)
- Timer load register B1 (TLB1)

10.3.1 Timer Mode Register B1 (TMB1)

TMB1 selects the auto-reload function and input clock.

Bit	Bit Name	Initial Value	R/W	Description
7	TMB17	0	R/W	Auto-reload function select 0: Interval timer function selected 1: Auto-reload function selected
6 to 3	—	All 1	—	Reserved These bits are always read as 1.
2	TMB12	0	R/W	Clock select
1	TMB11	0	R/W	000: Internal clock: ϕ/8192
0	TMB10	0	R/W	001: Internal clock: ϕ/2048 010: Internal clock: ϕ/512 011: Internal clock: ϕ/256 100: Internal clock: ϕ/64 101: Internal clock: ϕ/16 110: Internal clock: ϕ/4 111: External event (TMIB1): rising or falling edge* Note: * The edge of the external event signal is selected by bit IEG1 in the interrupt edge select register 1 (IEGR1). See section 3.2.1, Interrupt Edge Select Register 1 (IEGR1), for details. Before setting TMB12 to TMB10 to 1, IRQ1 in the port mode register 1 (PMR1) should be set to 1.

10.4 Operation

10.4.1 Interval Timer Operation

When bit TMB17 in TMB1 is cleared to 0, timer B1 functions as an 8-bit interval timer. Upon reset, TCB1 is cleared to H'00 and bit TMB17 is cleared to 0, so up-counting and interval timing resume immediately. The operating clock of the timer B1 is selected from seven internal clock signals output by prescaler S, or an external clock input at pin TMB1. The selection is made by bits TMB12 to TMB10 in TMB1.

After the count value in TMB1 reaches H'FF, the next clock signal input causes timer B1 to overflow, setting flag IRRTB1 in IRR2 to 1. If IENTB1 in IENR2 is 1, an interrupt is requested to the CPU.

At overflow, TCB1 returns to H'00 and starts counting up again. During interval timer operation (TMB17 = 0), when a value is set in TLB1, the same value is set in TCB1.

10.4.2 Auto-Reload Timer Operation

Setting bit TMB17 in TMB1 to 1 causes timer B1 to function as an 8-bit auto-reload timer. When a reload value is set in TLB1, the same value is loaded into TCB1, becoming the value from which TCB1 starts its count. After the count value in TCB1 reaches H'FF, the next clock signal input causes timer B1 to overflow. The TLB1 value is then loaded into TCB1, and the count continues from that value. The overflow period can be set within a range from 1 to 256 input clocks, depending on the TLB1 value.

The clock sources and interrupts in auto-reload mode are the same as in interval mode. In auto-reload mode (TMB17 = 1), when a new value is set in TLB1, the TLB1 value is also loaded into TCB1.

10.4.3 Event Counter Operation

Timer B1 can operate as an event counter in which TMIB1 is set to an event input pin. External event counting is selected by setting bits TMB12 to TMB10 in TMB1 to 1. TCB1 counts up at rising or falling edge of an external event signal input at pin TMB1.

When timer B1 is used to count external event input, bit IRQ1 in PMR1 should be set to 1 and IEN1 in IENR1 should be cleared to 0 to disable IRQ1 interrupt requests.

Bit	Bit Name	Initial Value	R/W	Description
1	—	1	—	Reserved This bit is always read as 1.
0	ICKS0	0	R/W	Internal Clock Select 0 This bit selects clock signals to input to TCNTV in combination with CKS2 to CKS0 in TCRV0. Refer to table 11.2.

11.4 Operation

11.4.1 Timer V Operation

1. According to table 11.2, six internal/external clock signals output by prescaler S can be selected as the timer V operating clock signals. When the operating clock signal is selected, TCNTV starts counting-up. Figure 11.2 shows the count timing with an internal clock signal selected, and figure 11.3 shows the count timing with both edges of an external clock signal selected.
2. When TCNTV overflows (changes from H'FF to H'00), the overflow flag (OVF) in TCRV0 will be set. The timing at this time is shown in figure 11.4. An interrupt request is sent to the CPU when OVIE in TCRV0 is 1.
3. TCNTV is constantly compared with TCORA and TCORB. Compare match flag A or B (CMFA or CMFB) is set to 1 when TCNTV matches TCORA or TCORB, respectively. The compare-match signal is generated in the last state in which the values match. Figure 11.5 shows the timing. An interrupt request is generated for the CPU when CMIEA or CMIEB in TCRV0 is 1.
4. When a compare match A or B is generated, the TMOV responds with the output value selected by bits OS3 to OS0 in TCSRV. Figure 11.6 shows the timing when the output is toggled by compare match A.
5. When CCLR1 or CCLR0 in TCRV0 is 01 or 10, TCNTV can be cleared by the corresponding compare match. Figure 11.7 shows the timing.
6. When CCLR1 or CCLR0 in TCRV0 is 11, TCNTV can be cleared by the rising edge of the input of TMRIV pin. A TMRIV input pulse-width of at least 1.5 system clocks is necessary. Figure 11.8 shows the timing.
7. When a counter-clearing source is generated with TRGE in TCRV1 set to 1, the counting-up is halted as soon as TCNTV is cleared. TCNTV resumes counting-up when the edge selected by TVEG1 or TVEG0 in TCRV1 is input from the TGRV pin.

Bit	Bit Name	Initial Value	R/W	Description
2	EC0	1	R/W	Master Enable C0 0: FTIOC0 pin output is enabled according to the TPMR, TFCR, and TIORC_0 settings 1: FTIOC0 pin output is disabled regardless of the TPMR, TFCR, and TIORC_0 settings (FTIOC0 pin is operated as an I/O port).
1	EB0	1	R/W	Master Enable B0 0: FTIOB0 pin output is enabled according to the TPMR, TFCR, and TIORA_0 settings 1: FTIOB0 pin output is disabled regardless of the TPMR, TFCR, and TIORA_0 settings (FTIOB0 pin is operated as an I/O port).
0	EA0	1	R/W	Master Enable A0 0: FTIOA0 pin output is enabled according to the TPMR, TFCR, and TIORA_0 settings 1: FTIOA0 pin output is disabled regardless of the TPMR, TFCR, and TIORA_0 settings (FTIOA0 pin is operated as an I/O port).

12.3.6 Timer Output Control Register (TOCR)

TOCR selects the initial outputs before the first occurrence of a compare match. Note that bits OLS1 and OLS0 in TFCR set these initial outputs in reset synchronous PWM mode and complementary PWM mode.

Bit	Bit Name	Initial Value	R/W	Description
7	TOD1	0	R/W	Output Level Select D1 0: 0 output at the FTIOD1 pin* 1: 1 output at the FTIOD1 pin*
6	TOC1	0	R/W	Output Level Select C1 0: 0 output at the FTIOC1 pin* 1: 1 output at the FTIOC1 pin*
5	TOB1	0	R/W	Output Level Select B1 0: 0 output at the FTIOB1 pin* 1: 1 output at the FTIOB1 pin*

Figure 12.9 illustrates periodic counter operation.

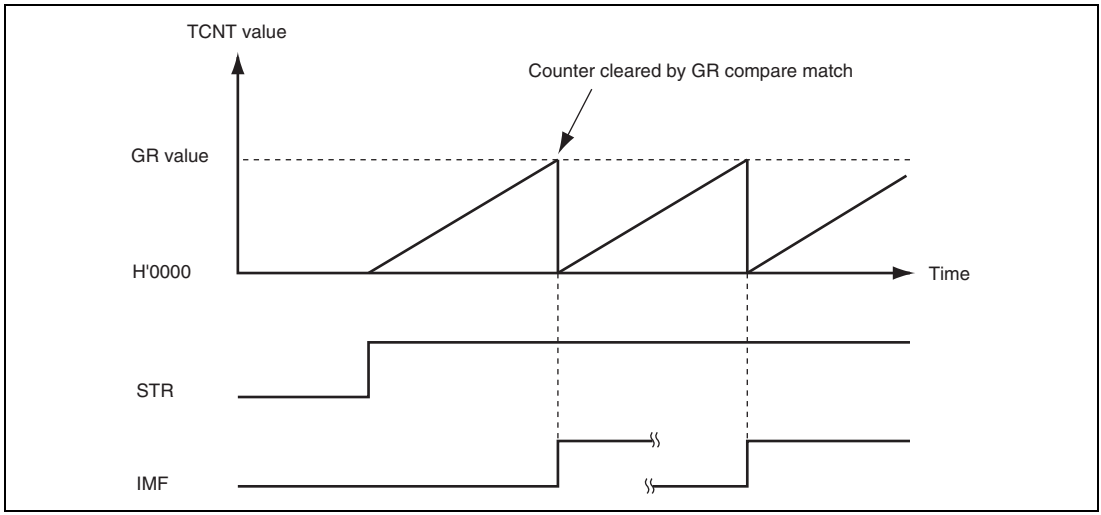

Figure 12.9 Periodic Counter Operation

TCNT Count Timing:

- Internal clock operation

  A system clock (ϕ) or three types of clocks (ϕ/2, ϕ/4, or ϕ/8) that divides the system clock can be selected by bits TPSC2 to TPSC0 in TCR.

  Figure 12.10 illustrates this timing.

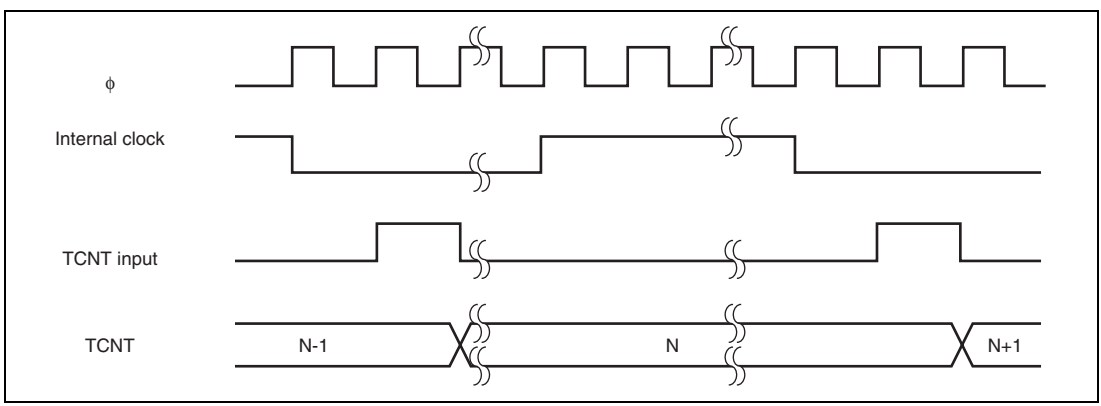

Figure 12.10 Count Timing at Internal Clock Operation

Figures 12.27 and 12.28 show examples of operation in reset synchronous PWM mode.

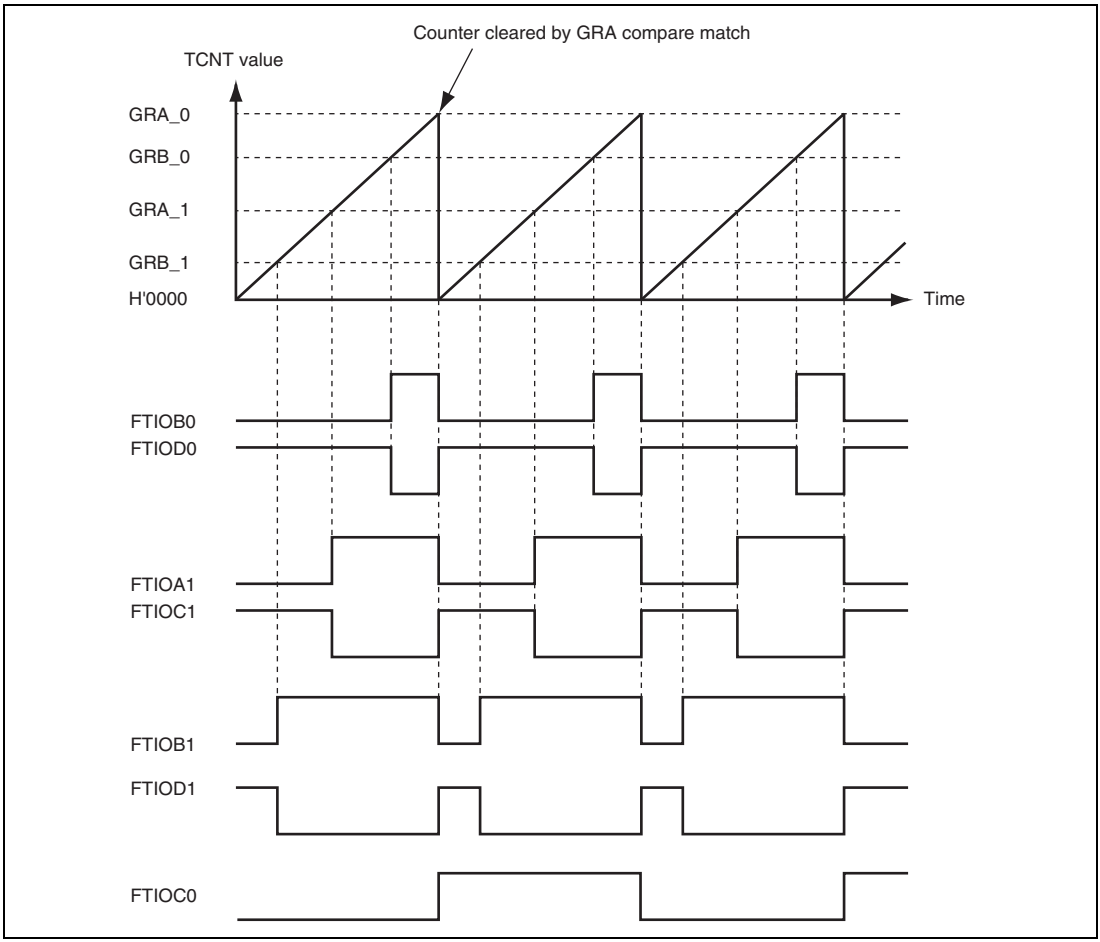

Figure 12.27 Example of Reset Synchronous PWM Mode Operation (OLS0 = OLS1 = 1)

Table 12.7 Register Settings in Complementary PWM Mode

Register	Description
TCNT_0	Initial setting of non-overlapped periods (non-overlapped periods are differences with TCNT_1)
TCNT_1	Initial setting of H'0000
GRA_0	Sets (upper limit value – 1) of TCNT_0
GRB_0	Set a changing point of the PWM waveform output from pins FTIOB0 and FTIOD0.
GRA_1	Set a changing point of the PWM waveform output from pins FTIOA1 and FTIOC1.
GRB_1	Set a changing point of the PWM waveform output from pins FTIOB1 and FTIOD1.

	Operating Frequency ϕ (MHz)											
	3.6864			4			4.9152			5		
Bit Rate (bit/s)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	64	0.70	2	70	0.03	2	86	0.31	2	88	–0.25
150	1	191	0.00	1	207	0.14	1	255	0.00	2	64	0.14
300	1	95	0.00	1	103	0.14	1	127	0.00	1	129	0.14
600	0	191	0.00	0	207	0.14	0	255	0.00	1	64	0.14
1200	0	95	0.00	0	103	0.14	0	127	0.00	0	129	0.14
2400	0	47	0.00	0	51	0.14	0	63	0.00	0	64	0.14
4800	0	23	0.00	0	25	0.14	0	31	0.00	0	32	–1.36
9600	0	11	0.00	0	12	0.14	0	15	0.00	0	15	1.73
19200	0	5	0.00	0	6	–6.99	0	7	0.00	0	7	1.73
31250	—	—	—	0	3	0.00	0	4	–1.70	0	4	0.00
38400	0	2	0.00	0	2	8.51	0	3	0.00	0	3	1.73

[Legend]

—: A setting is available but error occurs.

15.3.5 Bit Configuration Registers 0, 1 (BCR0, BCR1)

BCR configures the CAN bit timing parameters and baud rate prescaler for the CDLC.

- BCR0

Bit	Bit Name	Initial Value	R/W	Description
7	SJW1	0	R/W	Re-Synchronization Jump Width
6	SJW0	0	R/W	These bits set the maximum value of synchronization width. 00: 1 time quantum 01: 2 time quanta 10: 3 time quanta 11: 4 time quanta
5	BRP5	0	R/W	Baud Rate Prescaler
4	BRP4	0	R/W	These bits set the clock used for time quanta.
3	BRP3	0	R/W	000000: Setting prohibited
2	BRP2	0	R/W	000001: 2 system clocks
1	BRP1	0	R/W	: : (BRP + 1) system clocks
0	BRP0	0	R/W	111111: 64 system clocks

- BCR1

Bit	Bit Name	Initial Value	R/W	Description
7	—	0	—	Reserved This bit is always read as 0. The write value should always be 0.

16.4.6 Operation in Four-Line Bus Communication Mode

Four-line bus communication mode is a mode which communicates with the four-line bus; a clock line, a data input line, a data output line, and a chip select line. This mode includes bidirectional mode in which the data input line and the data output line function as a single pin. The data input line and the data output line are changed according to the settings of the MSS and BIDE bits in SSCRH. For details, refer to section 16.4.3, Relationship between Data Input/Output Pin and Shift Register. In this mode, relationship between clock polarity and phase, and data can be set by the CPOS and CPHS bits in SSMR. For details, refer to section 16.4.2, Relationship between Clock Polarity and Phase, and Data.

When the SSU is set as a master device, the chip select line controls output. When the SSU is set as a slave device, the chip select line controls input. When the SSU is set as a master device, the chip select line controls output of the $\overline{\text{SCS}}$ pin or controls output of a general port by setting the CSS1 bit in SSCRH to 1. When the SSU is set as a slave device, the chip select line sets the $\overline{\text{SCS}}$ pin as an input pin by setting the CSS1 and CSS0 bits in SSCRH to 01.

In four-line bus communication mode, the MLS bit in SSMR is set to 1 and transfer is performed in MSB-first order.

- Subclock error

  In addition to the above rounding error, the subtimer may have a count error caused by time lag between the system clock and the on-chip oscillator. The example is shown below.

Table 17.1 Example of Subclock Error

Condition: System clock = 10 MHz, on-chip oscillator = 400 kHz, and subclock = 12 kHz

	Min.	Expected Value	Max.
Count Value n	**49**	**50**	**51**
Division ratio k	34	33	33
Rounding error of division ratio σ	—	+1.0 %	—
Rounding error of division ratio σ + count error	–2.0 %	—	+1.0 %

After deciding the division ratio according to formulas (1) to (3), the division ratio is configured in ROPCR. After ROPCR divides clocks of the on-chip oscillator, clocks for the subtimer counter, input clocks to the system, and input clocks to the watchdog timer are generated.

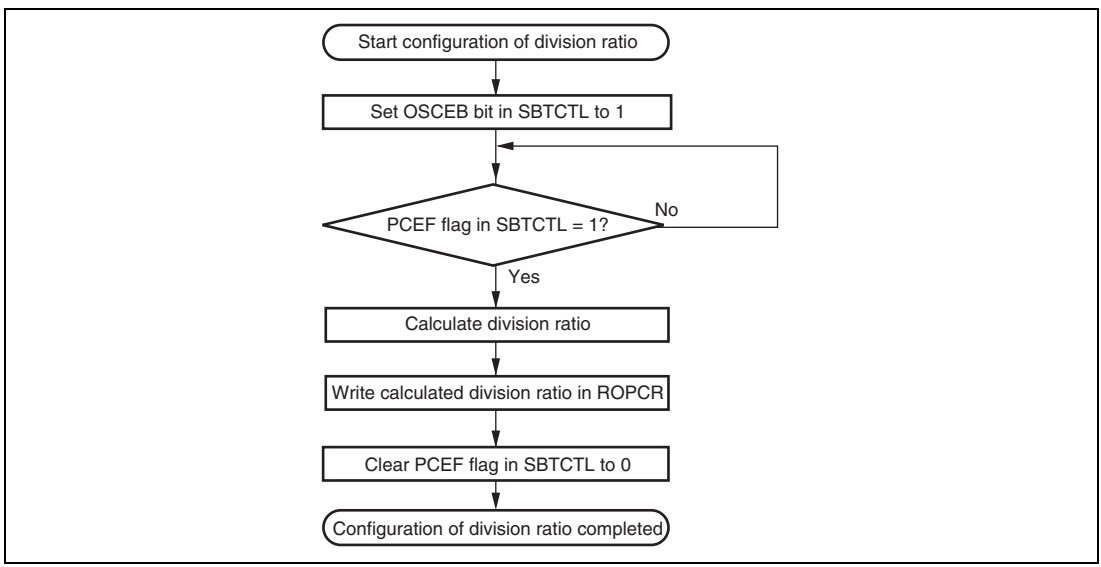

Figure 17.3 SBTPS Setting Flowchart

Register Abbreviation	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name
MC 1 [4]	ID20	ID19	ID18	RTR	IDE	—	ID17	ID16	TinyCAN
MC 1 [5]	ID28	ID27	ID26	ID25	ID24	ID23	ID22	ID21	
MC 1 [6]	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	
MC 1 [7]	ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8	
MC 2 [0]	DART	NMC	—	—	DLC3	DLC2	DLC1	DLC0	
MC 2 [4]	ID20	ID19	ID18	RTR	IDE	—	ID17	ID16	
MC 2 [5]	ID28	ID27	ID26	ID25	ID24	ID23	ID22	ID21	
MC 2 [6]	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	
MC 2 [7]	ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8	
MC 3 [0]	DART	NMC	—	—	DLC3	DLC2	DLC1	DLC0	
MC 3 [4]	ID20	ID19	ID18	RTR	IDE	—	ID17	ID16	
MC 3 [5]	ID28	ID27	ID26	ID25	ID24	ID23	ID22	ID21	
MC 3 [6]	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	
MC 3 [7]	ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8	
MD 0 [0]	MD07	MD06	MD05	MD04	MD03	MD02	MD01	MD00	
MD 0 [1]	MD17	MD16	MD15	MD14	MD13	MD12	MD11	MD10	
MD 0 [2]	MD27	MD26	MD25	MD24	MD23	MD22	MD21	MD20	
MD 0 [3]	MD37	MD36	MD35	MD34	MD33	MD32	MD31	MD30	
MD 0 [4]	MD47	MD46	MD45	MD44	MD43	MD42	MD41	MD40	
MD 0 [5]	MD57	MD56	MD55	MD54	MD53	MD52	MD51	MD50	
MD 0 [6]	MD67	MD66	MD65	MD64	MD63	MD62	MD61	MD60	
MD 0 [7]	MD77	MD76	MD75	MD74	MD73	MD72	MD71	MD70	
MD 1 [0]	MD07	MD06	MD05	MD04	MD03	MD02	MD01	MD00	
MD 1 [1]	MD17	MD16	MD15	MD14	MD13	MD12	MD11	MD10	
MD 1 [2]	MD27	MD26	MD25	MD24	MD23	MD22	MD21	MD20	
MD 1 [3]	MD37	MD36	MD35	MD34	MD33	MD32	MD31	MD30	
MD 1 [4]	MD47	MD46	MD45	MD44	MD43	MD42	MD41	MD40	
MD 1 [5]	MD57	MD56	MD55	MD54	MD53	MD52	MD51	MD50	
MD 1 [6]	MD67	MD66	MD65	MD64	MD63	MD62	MD61	MD60	
MD 1 [7]	MD77	MD76	MD75	MD74	MD73	MD72	MD71	MD70	

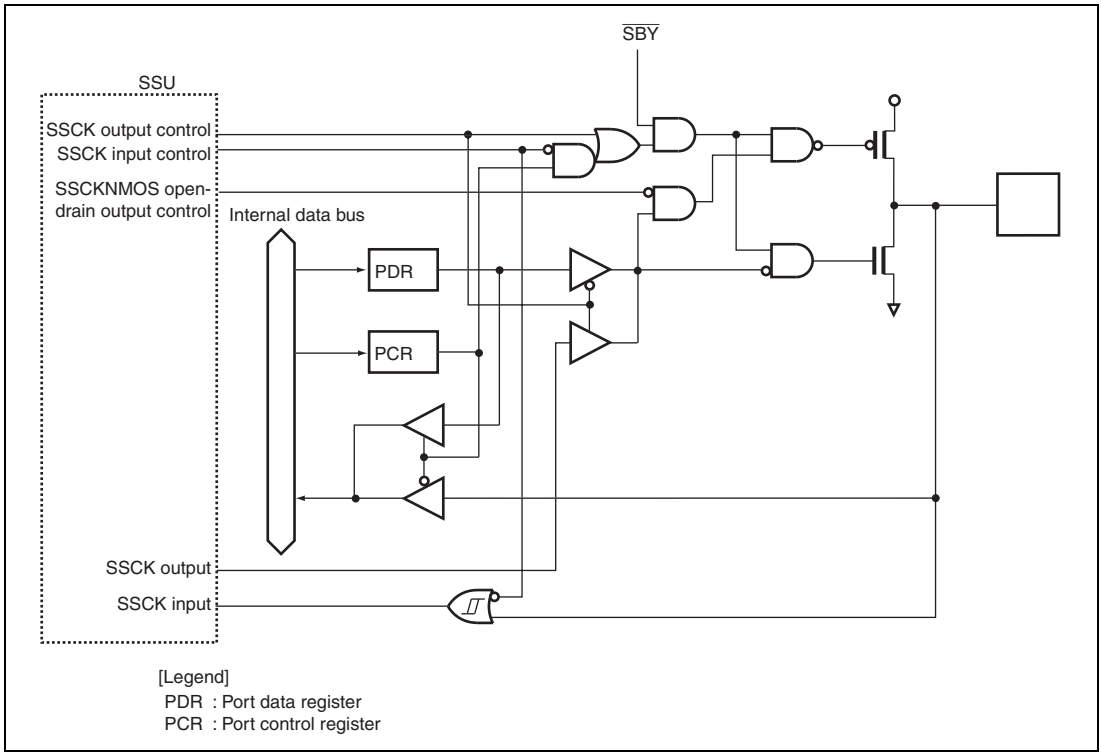

Figure B.25 Port 9 Block Diagram (P91)