Renesas Electronics America Inc - DF36037GFPV Datasheet

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300H
Core Size	16-Bit
Speed	20MHz
Connectivity	CANbus, SCI, SSU
Peripherals	LVD, POR, PWM, WDT
Number of I/O	45
Program Memory Size	56KB (56K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df36037gfpv

- BCLR instruction executed

```
BCLR   #0,    @PCR5
```

The BCLR instruction is executed for PCR5.

- After executing BCLR instruction

	P57	P56	P55	P54	P53	P52	P51	P50
Input/output	Output	Output	Output	Output	Output	Output	Output	Input
Pin state	Low level	High level	Low level	Low level	Low level	Low level	Low level	High level
PCR5	1	1	1	1	1	1	1	0
PDR5	1	0	0	0	0	0	0	0

- Description on operation

1. When the BCLR instruction is executed, first the CPU reads PCR5. Since PCR5 is a write-only register, the CPU reads a value of H'FF, even though the PCR5 value is actually H'3F.
2. Next, the CPU clears bit 0 in the read data to 0, changing the data to H'FE.
3. Finally, H'FE is written to PCR5 and BCLR instruction execution ends.

As a result of this operation, bit 0 in PCR5 becomes 0, making P50 an input port. However, bits 7 and 6 in PCR5 change to 1, so that P57 and P56 change from input pins to output pins. To prevent this problem, store a copy of the PDR5 data in a work area in memory and manipulate data of the bit in the work area, then write this data to PDR5.

- Prior to executing BCLR instruction

```
MOV.B   #3F,   R0L
MOV.B   R0L,   @RAM0
MOV.B   R0L,   @PCR5
```

The PCR5 value (H'3F) is written to a work area in memory (RAM0) as well as to PCR5.

	P57	P56	P55	P54	P53	P52	P51	P50
Input/output	Input	Input	Output	Output	Output	Output	Output	Output
Pin state	Low level	High level	Low level	Low level	Low level	Low level	Low level	Low level
PCR5	0	0	1	1	1	1	1	1
PDR5	1	0	0	0	0	0	0	0
RAM0	0	0	1	1	1	1	1	1

Section 6 Power-Down Modes

This LSI has six modes of operation after a reset. These include a normal active mode and four power-down modes, in which power consumption is significantly reduced. Module standby mode reduces power consumption by selectively halting on-chip module functions.

- Active mode

  The CPU and all on-chip peripheral modules are operable on the system clock. The system clock frequency can be selected from ϕosc, ϕosc/8, ϕosc/16, ϕosc/32, and ϕosc/64.
- Subactive mode

  The CPU and all on-chip peripheral modules are operable on the subclock. The subclock frequency can be selected from ϕw/2, ϕw/4, and ϕw/8.
- Sleep mode

  The CPU halts. On-chip peripheral modules are operable on the system clock.
- Subsleep mode

  The CPU halts. On-chip peripheral modules are operable on the subclock.
- Standby mode

  The CPU and all on-chip peripheral modules halt.
- Module standby mode

  Independent of the above modes, power consumption can be reduced by halting on-chip peripheral modules that are not used in module units.

11.3.2 Time Constant Registers A and B (TCORA, TCORB)

TCORA and TCORB have the same function.

TCORA and TCORB are 8-bit read/write registers.

TCORA and TCNTV are compared at all times. When the TCORA and TCNTV contents match, CMFA is set to 1 in TCSRV. If CMIEA is also set to 1 in TCRV0, a CPU interrupt is requested. Note that they must not be compared during the T3 state of a TCORA write cycle.

Timer output from the TMOV pin can be controlled by the identifying signal (compare match A) and the settings of bits OS3 to OS0 in TCSRV.

TCORA and TCORB are initialized to H'FF.

11.3.3 Timer Control Register V0 (TCRV0)

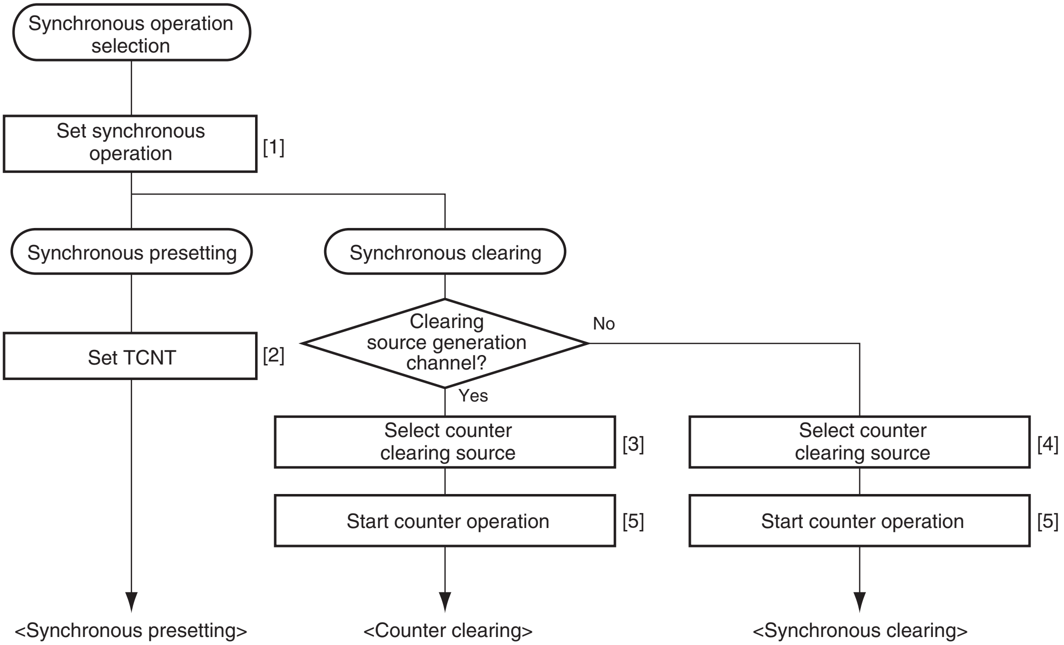
TCRV0 selects the input clock signals of TCNTV, specifies the clearing conditions of TCNTV, and controls each interrupt request.

Bit	Bit Name	Initial Value	R/W	Description
7	CMIEB	0	R/W	Compare Match Interrupt Enable B When this bit is set to 1, interrupt request from the CMFB bit in TCSRV is enabled.
6	CMIEA	0	R/W	Compare Match Interrupt Enable A When this bit is set to 1, interrupt request from the CMFA bit in TCSRV is enabled.
5	OVIE	0	R/W	Timer Overflow Interrupt Enable When this bit is set to 1, interrupt request from the OVF bit in TCSRV is enabled.
4	CCLR1	0	R/W	Counter Clear 1 and 0
3	CCLR0	0	R/W	These bits specify the clearing conditions of TCNTV. 00: Clearing is disabled 01: Cleared by compare match A 10: Cleared by compare match B 11: Cleared on the rising edge of the TMRIV pin. The operation of TCNTV after clearing depends on TRGE in TCRV1.

12.4.4 Synchronous Operation

In synchronous operation, the values in a number of TCNT counters can be rewritten simultaneously (synchronous presetting). Also, a number of TCNT counters can be cleared simultaneously by making the appropriate setting in TCR (synchronous clearing). Synchronous operation enables GR to be increased with respect to a single time base.

Figure 12.19 shows an example of the synchronous operation setting procedure.



[1] Set the SYNC bits in TMDR to 1.
[2] When a value is written to either of the TCNT counters, the same value is simultaneously written to the other TCNT counter.
[3] Set bits CCLR1 and CCLR0 in TCR to specify counter clearing by compare match/input capture.
[4] Set bits CCLR1 and CCLR0 in TCR to designate synchronous clearing for the counter clearing source.
[5] Set the STR bit in TSTR to 1 to start the count operation.

Figure 12.19 Example of Synchronous Operation Setting Procedure

Table 14.5 Examples of BRR Settings for Various Bit Rates (Clocked Synchronous Mode) (2)

	Operating Frequency ϕ (MHz)			
	18		20	
Bit Rate (bit/s)	n	N	n	N
110	—	—	—	—
250	—	—	—	—
500	3	140	3	155
1k	3	69	3	77
2.5k	2	112	2	124
5k	1	224	1	249
10k	1	112	1	124
25k	0	179	0	199
50k	0	89	0	99
100k	0	44	0	49
250k	0	17	0	19
500k	0	8	0	9
1M	0	4	0	4
2M	—	—	—	—
2.5M	—	—	0	1
4M	—	—	—	—

[Legend]

Blank:	No setting is available.
—:	A setting is available but error occurs.
*:	Continuous transfer is not possible.

14.4.3 Data Transmission

Figure 14.5 shows an example of operation for transmission in asynchronous mode. In transmission, the SCI3 operates as described below.

1. The SCI3 monitors the TDRE flag in SSR. If the flag is cleared to 0, the SCI3 recognizes that data has been written to TDR, and transfers the data from TDR to TSR.
2. After transferring data from TDR to TSR, the SCI3 sets the TDRE flag to 1 and starts transmission. If the TIE bit is set to 1 at this time, a TXI interrupt request is generated. Continuous transmission is possible because the TXI interrupt routine writes next transmit data to TDR before transmission of the current transmit data has been completed.
3. The SCI3 checks the TDRE flag at the timing for sending the stop bit.
4. If the TDRE flag is 0, the data is transferred from TDR to TSR, the stop bit is sent, and then serial transmission of the next frame is started.
5. If the TDRE flag is 1, the TEND flag in SSR is set to 1, the stop bit is sent, and then the "mark state" is entered, in which 1 is output. If the TEIE bit in SCR3 is set to 1 at this time, a TEI interrupt request is generated.
6. Figure 14.6 shows a sample flowchart for transmission in asynchronous mode.

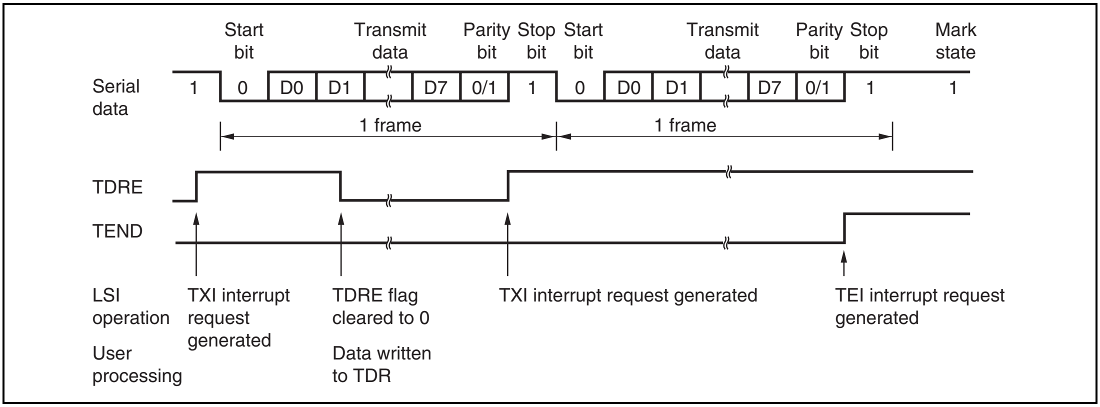


Figure 14.5 Example of SCI3 Transmission in Asynchronous Mode (8-Bit Data, Parity, One Stop Bit)

14.7 Interrupts

The SCI3 creates the following six interrupt requests: transmission end, transmit data empty, receive data full, and receive errors (overrun error, framing error, and parity error). Table 14.7 shows the interrupt sources.

Table 14.7 SCI3 Interrupt Requests

Interrupt Requests	Abbreviation	Interrupt Sources
Receive Data Full	RXI	Setting RDRF in SSR
Transmit Data Empty	TXI	Setting TDRE in SSR
Transmission End	TEI	Setting TEND in SSR
Receive Error	ERI	Setting OER, FER, and PER in SSR

The initial value of the TDRE flag in SSR is 1. Thus, when the TIE bit in SCR3 is set to 1 before transferring the transmit data to TDR, a TXI interrupt request is generated even if the transmit data is not ready. The initial value of the TEND flag in SSR is 1. Thus, when the TEIE bit in SCR3 is set to 1 before transferring the transmit data to TDR, a TEI interrupt request is generated even if the transmit data has not been sent. It is possible to make use of the most of these interrupt requests efficiently by transferring the transmit data to TDR in the interrupt routine. To prevent the generation of these interrupt requests (TXI and TEI), set the enable bits (TIE and TEIE) that correspond to these interrupt requests to 1, after transferring the transmit data to TDR.

Bit	Bit Name	Initial Value	R/W	Description
2	TCMPL	1	R	Message Transmission Complete Flag Indicates whether the TinyCAN has finished message transmission. [Setting condition] When the TinyCAN has finished message transmission [Clearing condition] While a message is being transmitted (period from SOF (start of frame) to the third bit of the intermission space)
1	ECWRG	0	R	Error Counter Warning Flag Indicates an error warning. [Setting condition] When 96 ≤ TEC ≤ 256 or 96 ≤ REC ≤ 256 [Clearing condition] When TEC< 96, REC < 96, or TEC ≥ 256
0	BOFF	0	R	Bus Off Flag Indicates the bus off state. [Setting condition] When TEC ≥ 256 (bus off state) [Clearing condition] When the TinyCAN recovers from the bus off state

15.3.13 Unread Message Status Register (UMSR)

UMSR is a status flag that indicates that an unread message in each Mailbox has been overwritten by a new receive message or a new receive message has been discarded.

Bit	Bit Name	Initial Value	R/W	Description
7 to 4	—	All 0	—	Reserved These bits are always read as 0.
3	MB3	0	R/(W)*	Status flags indicating that a new receive message has overwritten/overrun an unread message. [Setting condition] When a new message is received before the corresponding bit in RXPR or RFPR is cleared to 0 [Clearing condition] When 1 is written to these bits
2	MB2	0	R/(W)*	
1	MB1	0	R/(W)*	
0	MB0	0	R/(W)*	

Note: * Only 1 can be written to clear the flag.

4. If an arbitration loss occurs in the arbitration field, the TinyCAN starts reception. When the DART or MBn bit in TXCR is set to 1, a transmit request for message 1 is canceled. At this time, the MBn bits in TXPR and TXCR are cleared to 0 and the MBn bit in ABACK and the EMPI bit in TCIRR1 are set to 1. The MBn bit in TXACK is always 0.
5. When there is a transmit request after reception has completed (for details, see section 15.5.4, Message Reception), the arbitration for message 2 is determined and it is transmitted to the CAN bus. When there is no transmit request, the TinyCAN starts reception.

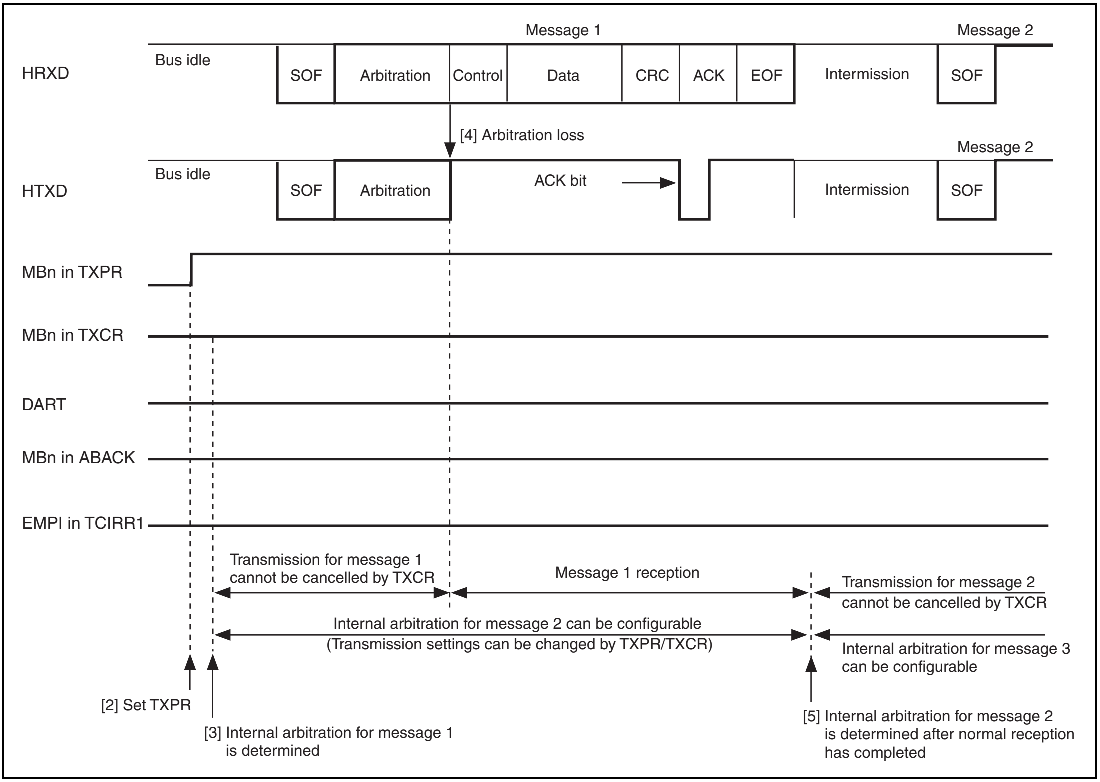

Message 1
Message 2
HRXD
Bus idle
SOF
Arbitration
Control
Data
CRC
ACK
EOF
Intermission
SOF
[4] Arbitration loss
Message 2
HTXD
Bus idle
SOF
Arbitration
ACK bit
Intermission
SOF
MBn in TXPR
MBn in TXCR
DART
MBn in ABACK
EMPI in TCIRR1
Transmission for message 1 cannot be cancelled by TXCR
Message 1 reception
Transmission for message 2 cannot be cancelled by TXCR
Internal arbitration for message 2 can be configurable (Transmission settings can be changed by TXPR/TXCR)
Internal arbitration for message 3 can be configurable
[2] Set TXPR
[3] Internal arbitration for message 1 is determined
[5] Internal arbitration for message 2 is determined after normal reception has completed

Figure 15.8 Internal Arbitration at Reception Caused by CAN Bus Arbitration Loss (MBn in TXCR = 0 and DART = 0)

Bit	Bit Name	Initial Value	R/W	Description
2	CKS2	0	R/W	Transfer clock rate select
1	CKS1	0	R/W	Sets transfer clock rate (prescaler division ratio) when the internal clock is selected.
0	CKS0	0	R/W	000: φ/256 001: φ/128 010: φ/64 011: φ/32 100: φ/16 101: φ/8 110: φ/4 111: Reserved

16.3.4 SS Enable Register (SSER)

SSER is a register that sets transmit enable, receive enable, and interrupt enable.

Bit	Bit Name	Initial Value	R/W	Description
7	TE	0	R/W	Transmit enable When this bit is 1, transmit operation is enabled.
6	RE	0	R/W	Receive enable When this bit is 1, receive operation is enabled.
5	RSSTP	0	R/W	Receive single stop When this bit is 1, receive operation is completed after receiving one byte.
4	—	0	—	Reserved This bit is always read as 0.
3	TEIE	0	R/W	Transmit End Interrupt Enable When this bit is set to 1, a TEI interrupt request is enabled.
2	TIE	0	R/W	Transmit Interrupt Enable When this bit is set to 1, a TXI interrupt request is enabled.

- Subclock error

  In addition to the above rounding error, the subtimer may have a count error caused by time lag between the system clock and the on-chip oscillator. The example is shown below.

Table 17.1 Example of Subclock Error

Condition: System clock = 10 MHz, on-chip oscillator = 400 kHz, and subclock = 12 kHz

	Min.	Expected Value	Max.
Count Value n	**49**	**50**	**51**
Division ratio k	34	33	33
Rounding error of division ratio σ	—	+1.0 %	—
Rounding error of division ratio σ + count error	–2.0 %	—	+1.0 %

After deciding the division ratio according to formulas (1) to (3), the division ratio is configured in ROPCR. After ROPCR divides clocks of the on-chip oscillator, clocks for the subtimer counter, input clocks to the system, and input clocks to the watchdog timer are generated.

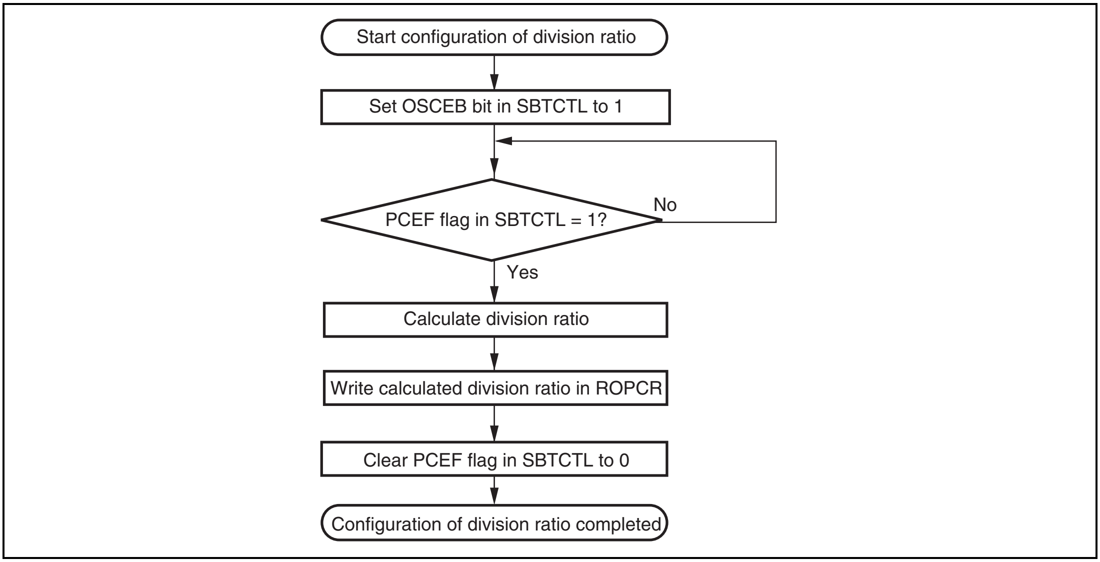

Start configuration of division ratio
Set OSCEB bit in SBTCTL to 1
PCEF flag in SBTCTL = 1?
No
Yes
Calculate division ratio
Write calculated division ratio in ROPCR
Clear PCEF flag in SBTCTL to 0
Configuration of division ratio completed

Figure 17.3 SBTPS Setting Flowchart

18.3 Register Descriptions

The A/D converter has the following registers.

- A/D data register A (ADDRA)
- A/D data register B (ADDRB)
- A/D data register C (ADDRC)
- A/D data register D (ADDRD)
- A/D control/status register (ADCSR)
- A/D control register (ADCR)

18.3.1 A/D Data Registers A to D (ADDRA to ADDRD)

There are four 16-bit read-only ADDR registers; ADDRA to ADDRD, used to store the results of A/D conversion. The ADDR registers, which store a conversion result for each analog input channel, are shown in table 18.2.

The converted 10-bit data is stored in bits 15 to 6. The lower 6 bits are always read as 0.

The data bus width between the CPU and the A/D converter is 8 bits. The upper byte can be read directly from the CPU, however the lower byte should be read via a temporary register. The temporary register contents are transferred from the ADDR when the upper byte data is read. Therefore, byte access to ADDR should be done by reading the upper byte first then the lower one. Word access is also possible. ADDR is initialized to H'0000.

Table 18.2 Analog Input Channels and Corresponding ADDR Registers

Analog Input Channel		
Group 0	**Group 1**	**A/D Data Register to be Stored Results of A/D Conversion**
AN0	AN4	ADDRA
AN1	AN5	ADDRB
AN2	AN6	ADDRC
AN3	AN7	ADDRD

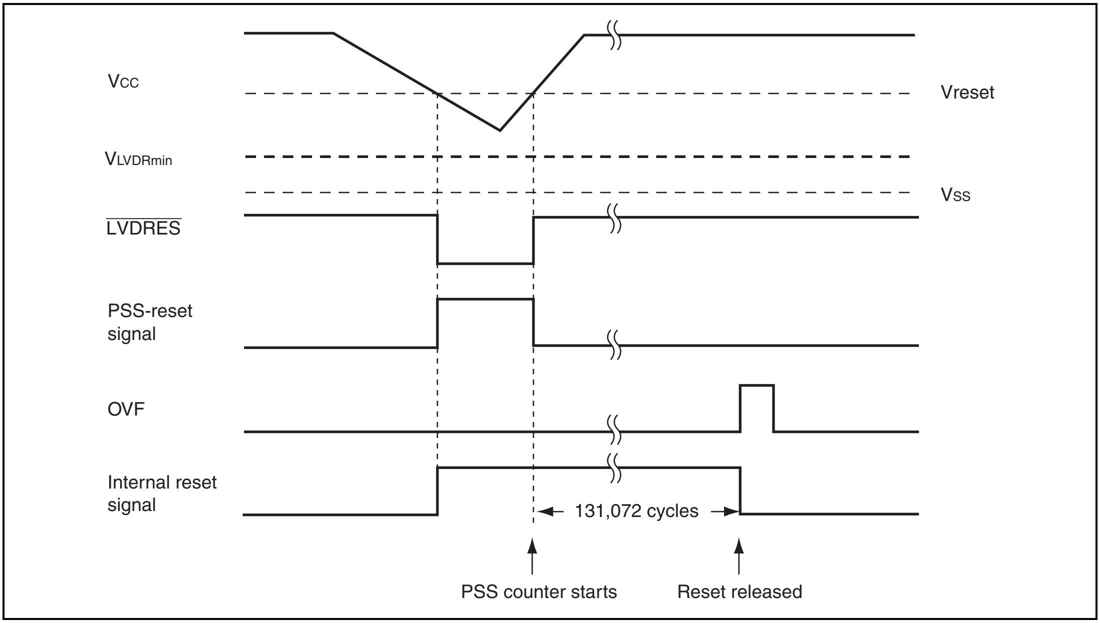


Figure 19.3 Operational Timing of LVDR Circuit

LVDI (Interrupt by Low Voltage Detect) Circuit:

Figure 19.4 shows the timing of LVDI functions. The LVDI enters the module-standby state after a power-on reset is canceled. To operate the LVDI, set the LVDE bit in LVDCR to 1, wait for 50 µs (t_{LVDON}) until the reference voltage and the low-voltage-detection power supply have stabilized by a software timer, etc., then set the LVDDE and LVDUE bits in LVDCR to 1. After that, the output settings of ports must be made. To cancel the low-voltage detection circuit, first the LVDDE and LVDUE bits should all be cleared to 0 and then the LVDE bit should be cleared to 0. The LVDE bit must not be cleared to 0 at the same timing as the LVDDE and LVDUE bits because incorrect operation may occur.

When the power-supply voltage falls below Vint (D) (typ. = 3.7 V) voltage, the LVDI clears the $\overline{\text{LVDINT}}$ signal to 0 and the LVDDF bit in LVDSR is set to 1. If the LVDDE bit is 1 at this time, an IRQ0 interrupt request is simultaneously generated. In this case, the necessary data must be saved in the external EEPROM, etc, and a transition must be made to standby mode or subsleep mode. Until this processing is completed, the power supply voltage must be higher than the lower limit of the guaranteed operating voltage.

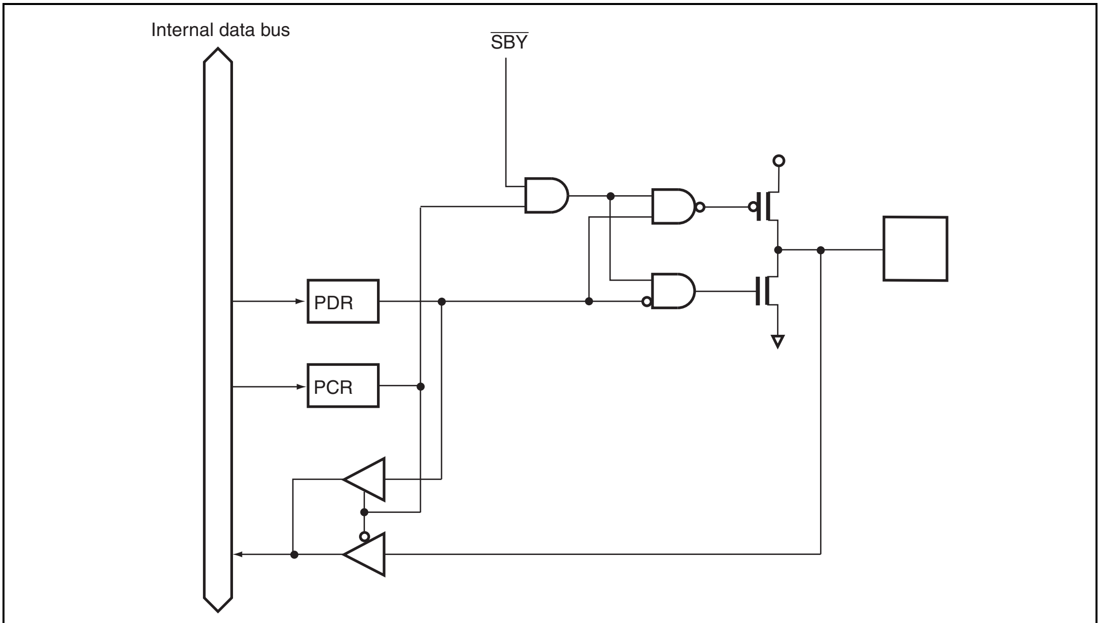
When the power-supply voltage does not fall below Vreset1 (typ. = 2.3 V) voltage but rises above Vint (U) (typ. = 4.0 V) voltage, the LVDI sets the $\overline{\text{LVDINT}}$ signal to 1. If the LVDUE bit is 1 at

Register Name	Abbre-viation	Bit No	Address	Module Name	Data Bus Width	Access State
Serial status register_2	SSR_2	8	H'F744	SCI3_2*[3]	8	3
Receive data register_2	RDR_2	8	H'F745	SCI3_2*[3]	8	3
—	—	—	H'F746 to H'F75F	—	—	—
Timer mode register B1	TMB1	8	H'F760	Timer B1	8	2
Timer counter B1	TCB1	8	H'F761	Timer B1	8	2
Timer load register B1	TLB1	8	H'F761	Timer B1	8	2
—	—	—	H'F762 to H'FF8F	—	—	—
Flash memory control register 1	FLMCR1	8	H'FF90	ROM	8	2
Flash memory control register 2	FLMCR2	8	H'FF91	ROM	8	2
Flash memory power control register	FLPWCR	8	H'FF92	ROM	8	2
Erase block register 1	EBR1	8	H'FF93	ROM	8	2
—	—	—	H'FF94 to H'FF9A	—	—	—
Flash memory enable register	FENR	8	H'FF9B	ROM	8	2
—	—	—	H'FF9C to H'FF9F	—	—	—
Timer control register V0	TCRV0	8	H'FFA0	Timer V	8	3
Timer control/status register V	TCSRV	8	H'FFA1	Timer V	8	3
Time constant register A	TCORA	8	H'FFA2	Timer V	8	3
Time constant register B	TCORB	8	H'FFA3	Timer V	8	3
Timer counter V	TCNTV	8	H'FFA4	Timer V	8	3
Timer control register V1	TCRV1	8	H'FFA5	Timer V	8	3
—	—	—	H'FFA6, H'FFA7	—	—	—
Serial mode register	SMR	8	H'FFA8	SCI3	8	3
Bit rate register	BRR	8	H'FFA9	SCI3	8	3
Serial control register 3	SCR3	8	H'FFAA	SCI3	8	3
Transmit data register	TDR	8	H'FFAB	SCI3	8	3
Serial status register	SSR	8	H'FFAC	SCI3	8	3

Notes: 1. LVDC: Low-voltage detection circuits (optional)
2. The H8/36037 Group does not have the SCI3_2.
3. WDT: Watchdog timer
4. These bits are reserved in the H8/36037 Group.

Register Abbreviation	Reset	Active	Sleep	Subactive	Subsleep	Standby	Module
TMDR	Initialized	—	—	—	—	—	Timer Z
TPMR	Initialized	—	—	—	—	—	
TFCR	Initialized	—	—	—	—	—	
TOER	Initialized	—	—	—	—	—	
TOCR	Initialized	—	—	—	—	—	
LVDCR	Initialized	—	—	—	—	—	LVDC (optional)*1
LVDSR	Initialized	—	—	—	—	—	
SMR_2	Initialized	—	—	Initialized	Initialized	Initialized	SCI3_2*3
BRR_2	Initialized	—	—	Initialized	Initialized	Initialized	
SCR3_2	Initialized	—	—	Initialized	Initialized	Initialized	
TDR_2	Initialized	—	—	Initialized	Initialized	Initialized	
SSR_2	Initialized	—	—	Initialized	Initialized	Initialized	
RDR_2	Initialized	—	—	Initialized	Initialized	Initialized	
TMB1	Initialized	—	—	—	—	—	Timer B1
TCB1	Initialized	—	—	—	—	—	
Tlb1	Initialized	—	—	—	—	—	
FLMCR1	Initialized	—	—	Initialized	Initialized	Initialized	ROM
FLMCR2	Initialized	—	—	—	—	—	
FLPWCR	Initialized	—	—	—	—	—	
EBR1	Initialized	—	—	Initialized	Initialized	Initialized	
FENR	Initialized	—	—	—	—	—	
TCRV0	Initialized	—	—	Initialized	Initialized	Initialized	Timer V
TCSRV	Initialized	—	—	Initialized	Initialized	Initialized	
TCORA	Initialized	—	—	Initialized	Initialized	Initialized	
TCORB	Initialized	—	—	Initialized	Initialized	Initialized	
TCNTV	Initialized	—	—	Initialized	Initialized	Initialized	
TCRV1	Initialized	—	—	Initialized	Initialized	Initialized	
SMR	Initialized	—	—	Initialized	Initialized	Initialized	SCI3
BRR	Initialized	—	—	Initialized	Initialized	Initialized	
SCR3	Initialized	—	—	Initialized	Initialized	Initialized	
TDR	Initialized	—	—	Initialized	Initialized	Initialized	

Mnemonic		Operand Size	Addressing Mode and Instruction Length (bytes)									Operation	Condition Code						No. of States*1	
			#xx	Rn	@ERn	@(d, ERn)	@−ERn/@ERn+	@aa	@(d, PC)	@@aa	—		I	H	N	Z	V	C	Normal	Advanced
BLD	BLD #xx:3, @ERd	B			4							(#xx:3 of @ERd) → C	—	—	—	—	—	↕	6	
	BLD #xx:3, @aa:8	B						4				(#xx:3 of @aa:8) → C	—	—	—	—	—	↕	6	
BILD	BILD #xx:3, Rd	B		2								¬ (#xx:3 of Rd8) → C	—	—	—	—	—	↕	2	
	BILD #xx:3, @ERd	B			4							¬ (#xx:3 of @ERd) → C	—	—	—	—	—	↕	6	
	BILD #xx:3, @aa:8	B						4				¬ (#xx:3 of @aa:8) → C	—	—	—	—	—	↕	6	
BST	BST #xx:3, Rd	B		2								C → (#xx:3 of Rd8)	—	—	—	—	—	—	2	
	BST #xx:3, @ERd	B			4							C → (#xx:3 of @ERd24)	—	—	—	—	—	—	8	
	BST #xx:3, @aa:8	B						4				C → (#xx:3 of @aa:8)	—	—	—	—	—	—	8	
BIST	BIST #xx:3, Rd	B		2								¬ C → (#xx:3 of Rd8)	—	—	—	—	—	—	2	
	BIST #xx:3, @ERd	B			4							¬ C → (#xx:3 of @ERd24)	—	—	—	—	—	—	8	
	BIST #xx:3, @aa:8	B						4				¬ C → (#xx:3 of @aa:8)	—	—	—	—	—	—	8	
BAND	BAND #xx:3, Rd	B		2								C∧(#xx:3 of Rd8) → C	—	—	—	—	—	↕	2	
	BAND #xx:3, @ERd	B			4							C∧(#xx:3 of @ERd24) → C	—	—	—	—	—	↕	6	
	BAND #xx:3, @aa:8	B						4				C∧(#xx:3 of @aa:8) → C	—	—	—	—	—	↕	6	
BIAND	BIAND #xx:3, Rd	B		2								C∧ ¬ (#xx:3 of Rd8) → C	—	—	—	—	—	↕	2	
	BIAND #xx:3, @ERd	B			4							C∧ ¬ (#xx:3 of @ERd24) → C	—	—	—	—	—	↕	6	
	BIAND #xx:3, @aa:8	B						4				C∧ ¬ (#xx:3 of @aa:8) → C	—	—	—	—	—	↕	6	
BOR	BOR #xx:3, Rd	B		2								C∨(#xx:3 of Rd8) → C	—	—	—	—	—	↕	2	
	BOR #xx:3, @ERd	B			4							C∨(#xx:3 of @ERd24) → C	—	—	—	—	—	↕	6	
	BOR #xx:3, @aa:8	B						4				C∨(#xx:3 of @aa:8) → C	—	—	—	—	—	↕	6	
BIOR	BIOR #xx:3, Rd	B		2								C∨ ¬ (#xx:3 of Rd8) → C	—	—	—	—	—	↕	2	
	BIOR #xx:3, @ERd	B			4							C∨ ¬ (#xx:3 of @ERd24) → C	—	—	—	—	—	↕	6	
	BIOR #xx:3, @aa:8	B						4				C∨ ¬ (#xx:3 of @aa:8) → C	—	—	—	—	—	↕	6	
BXOR	BXOR #xx:3, Rd	B		2								C⊕(#xx:3 of Rd8) → C	—	—	—	—	—	↕	2	
	BXOR #xx:3, @ERd	B			4							C⊕(#xx:3 of @ERd24) → C	—	—	—	—	—	↕	6	
	BXOR #xx:3, @aa:8	B						4				C⊕(#xx:3 of @aa:8) → C	—	—	—	—	—	↕	6	
BIXOR	BIXOR #xx:3, Rd	B		2								C⊕ ¬ (#xx:3 of Rd8) → C	—	—	—	—	—	↕	2	
	BIXOR #xx:3, @ERd	B			4							C⊕ ¬ (#xx:3 of @ERd24) → C	—	—	—	—	—	↕	6	
	BIXOR #xx:3, @aa:8	B						4				C⊕ ¬ (#xx:3 of @aa:8) → C	—	—	—	—	—	↕	6	



[Legend]
PMR : Port mode register
PCR : Port control register

Figure B.22 Port 9 Block Diagram (P94, P95)