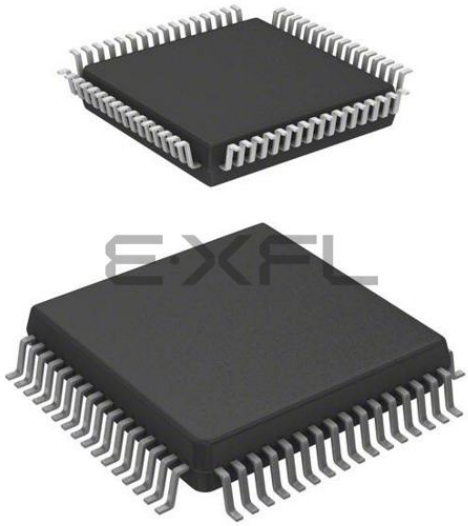

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300H
Core Size	16-Bit
Speed	20MHz
Connectivity	CANbus, SCI, SSU
Peripherals	PWM, WDT
Number of I/O	45
Program Memory Size	56KB (56K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	64-BQFP
Supplier Device Package	64-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df36037hv

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2.2 Register Configuration

The H8/300H CPU has the internal registers shown in figure 2.2. There are two types of registers; general registers and control registers. The control registers are a 24-bit program counter (PC), and an 8-bit condition-code register (CCR).

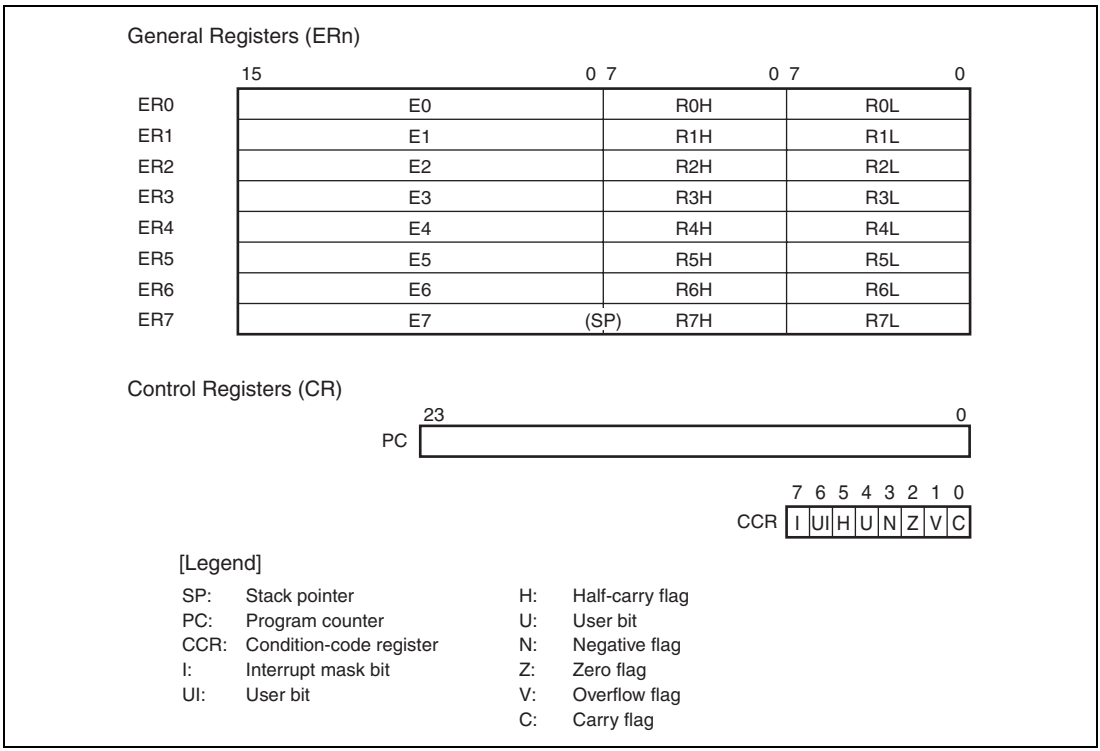
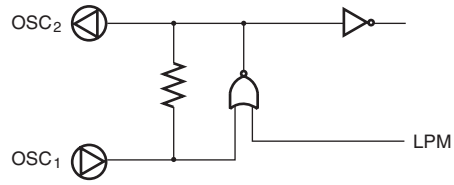


Figure 2.2 CPU Registers

5.1 System Clock Generator

Clock pulses can be supplied to the system clock divider either by connecting a crystal or ceramic resonator, or by providing external clock input. Figure 5.2 shows a block diagram of the system clock generator.



LPM: Low-power mode (standby mode, subactive mode, subsleep mode)

Figure 5.2 Block Diagram of System Clock Generator

5.1.1 Connecting Crystal Resonator

Figure 5.3 shows a typical method of connecting a crystal resonator. An AT-cut parallel-resonance crystal resonator should be used. Figure 5.4 shows the equivalent circuit of a crystal resonator. A resonator having the characteristics given in table 5.1 should be used.

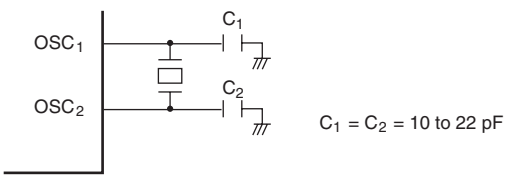


Figure 5.3 Typical Connection to Crystal Resonator

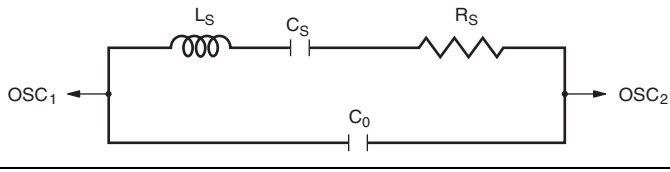


Figure 5.4 Equivalent Circuit of Crystal Resonator

Table 6.1 Operating Frequency and Waiting Time

Bit Name				Operating Frequency							
STS2	STS1	STS0	Waiting Time	20 MHz	16 MHz	10 MHz	8 MHz	4 MHz	2 MHz	1 MHz	0.5 MHz
0	0	0	8,192 states	0.4	0.5	0.8	1.0	2.0	4.1	8.1	16.4
		1	16,384 states	0.8	1.0	1.6	2.0	4.1	8.2	16.4	32.8
	1	0	32,768 states	1.6	2.0	3.3	4.1	8.2	16.4	32.8	65.5
		1	65,536 states	3.3	4.1	6.6	8.2	16.4	32.8	65.5	131.1
1	0	0	131,072 states	6.6	8.2	13.1	16.4	32.8	65.5	131.1	262.1
		1	1,024 states	0.05	0.06	0.10	0.13	0.26	0.51	1.02	2.05
	1	0	128 states	0.00	0.00	0.01	0.02	0.03	0.06	0.13	0.26
		1	16 states	0.00	0.00	0.00	0.00	0.00	0.01	0.02	0.03

Note: Time unit is ms.

6.1.2 System Control Register 2 (SYSCR2)

SYSCR2 controls the power-down modes, as well as SYSCR1.

Bit	Bit Name	Initial Value	R/W	Description
7	SMSEL	0	R/W	Sleep Mode Selection
6	LSON	0	R/W	Low Speed on Flag
5	DTON	0	R/W	Direct Transfer on Flag These bits select the mode to enter after the execution of a SLEEP instruction, as well as the SSBY bit in SYSCR1. For details, see table 6.2.
4	MA2	0	R/W	Active Mode Clock Select 2 to 0
3	MA1	0	R/W	These bits select the operating clock frequency in active and sleep modes. The operating clock frequency changes to the set frequency after the SLEEP instruction is executed. 0XX: ϕ_{osc} 100: $\phi_{osc}/8$ 101: $\phi_{osc}/16$ 110: $\phi_{osc}/32$ 111: $\phi_{osc}/64$
2	MA0	0	R/W	

- P16/$\overline{\text{IRQ2}}$ pin

Register	PMR1	PCR1	
Bit Name	**IRQ2**	**PCR16**	**Pin Function**
Setting value	0	0	P16 input pin
		1	P16 output pin
	1	X	$\overline{\text{IRQ2}}$ input pin

[Legend]
X: Don't care.

- P15/$\overline{\text{IRQ1}}$/TMIB1 pin

Register	PMR1	PCR1	
Bit Name	**IRQ1**	**PCR15**	**Pin Function**
Setting value	0	0	P15 input pin
		1	P15 output pin
	1	X	$\overline{\text{IRQ1}}$ input/TMIB1 input pin

[Legend]
X: Don't care.

- P14/$\overline{\text{IRQ0}}$ pin

Register	PMR1	PCR1	
Bit Name	**IRQ0**	**PCR14**	**Pin Function**
Setting value	0	0	P14 input pin
		1	P14 output pin
	1	X	$\overline{\text{IRQ0}}$ input pin

[Legend]
X: Don't care.

- P12 pin

Register	PCR1	
Bit Name	**PCR12**	**Pin Function**
Setting value	0	P12 input pin
	1	P12 output pin

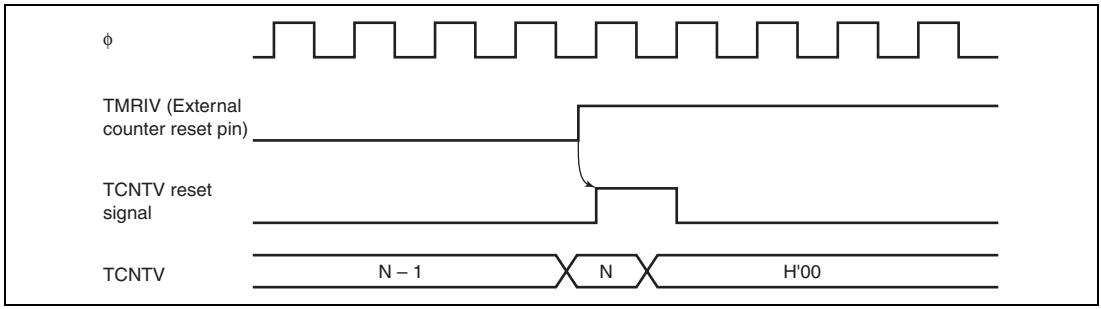


Figure 11.8 Clear Timing by TMRIV Input

11.5 Timer V Application Examples

11.5.1 Pulse Output with Arbitrary Duty Cycle

Figure 11.9 shows an example of output of pulses with an arbitrary duty cycle.

1. Set bits CCLR1 and CCLR0 in TCRV0 so that TCNTV will be cleared by compare match with TCORA.
2. Set bits OS3 to OS0 in TCSRV so that the output will go to 1 at compare match with TCORA and to 0 at compare match with TCORB.
3. Set bits CKS2 to CKS0 in TCRV0 and bit ICKS0 in TCRV1 to select the desired clock source.
4. With these settings, a waveform is output without further software intervention, with a period determined by TCORA and a pulse width determined by TCORB.

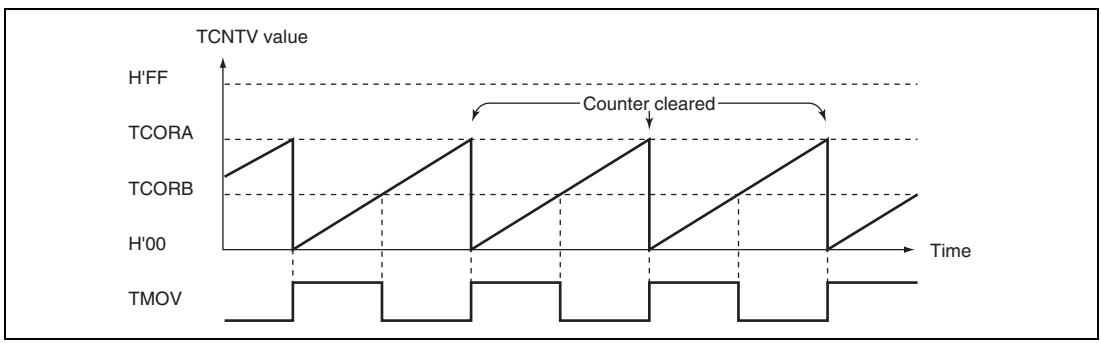


Figure 11.9 Pulse Output Example

11.6 Usage Notes

The following types of contention or operation can occur in timer V operation.

1. Writing to registers is performed in the T3 state of a TCNTV write cycle. If a TCNTV clear signal is generated in the T3 state of a TCNTV write cycle, as shown in figure 11.11, clearing takes precedence and the write to the counter is not carried out. If counting-up is generated in the T3 state of a TCNTV write cycle, writing takes precedence.
2. If a compare match is generated in the T3 state of a TCORA or TCORB write cycle, the write to TCORA or TCORB takes precedence and the compare match signal is inhibited. Figure 11.12 shows the timing.
3. If compare matches A and B occur simultaneously, any conflict between the output selections for compare match A and compare match B is resolved by the following priority: toggle output > output 1 > output 0.
4. Depending on the timing, TCNTV may be incremented by a switch between different internal clock sources. When TCNTV is internally clocked, an increment pulse is generated from the falling edge of an internal clock signal that is a divided system clock (ϕ). Therefore, as shown in figure 11.3 the switch is from a high clock signal to a low clock signal, the switchover is seen as a falling edge, causing TCNTV to increment. TCNTV can also be incremented by a switch between internal and external clocks.

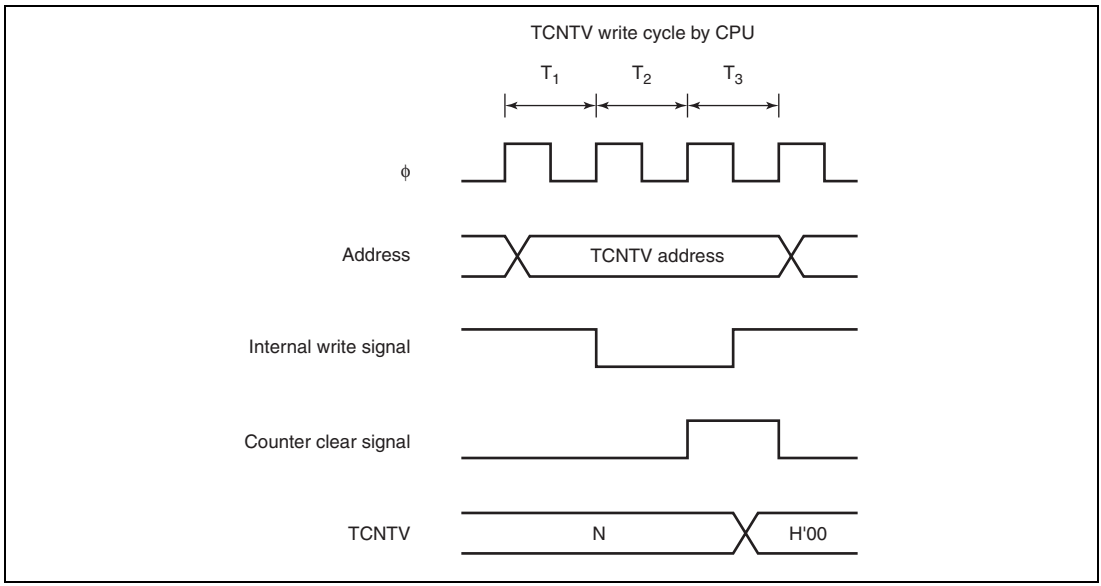


Figure 11.11 Contention between TCNTV Write and Clear

12.3.2 Timer Mode Register (TMDR)

TMDR selects buffer operation settings and synchronized operation.

Bit	Bit Name	Initial Value	R/W	Description
7	BFD1	0	R/W	Buffer Operation D1 0: GRD_1 operates normally 1: GRB_1 and GRD_1 are used together for buffer operation
6	BFC1	0	R/W	Buffer Operation C1 0: GRC_1 operates normally 1: GRA_1 and GRD_1 are used together for buffer operation
5	BFD0	0	R/W	Buffer Operation D0 0: GRD_0 operates normally 1: GRB_0 and GRD_0 are used together for buffer operation
4	BFC0	0	R/W	Buffer Operation C0 0: GRC_0 operates normally 1: GRA_0 and GRC_0 are used together for buffer operation
3 to 1	—	All 1	—	Reserved These bits are always read as 1 and cannot be modified.
0	SYNC	0	R/W	Timer Synchronization 0: TCNT_1 and TCNT_0 operate as a different timer 1: TCNT_1 and TCNT_0 are synchronized TCNT_1 and TCNT_0 can be pre-set or cleared synchronously

12.4.8 Buffer Operation

Buffer operation differs depending on whether GR has been designated for an input capture register or an output compare register, or in reset synchronous PWM mode or complementary PWM mode.

Table 12.8 shows the register combinations used in buffer operation.

Table 12.8 Register Combinations in Buffer Operation

General Register	Buffer Register
GRA	GRC
GRB	GRD

When GR is Output Compare Register: When a compare match occurs, the value in the buffer register of the corresponding channel is transferred to the general register.

This operation is illustrated in figure 12.35.

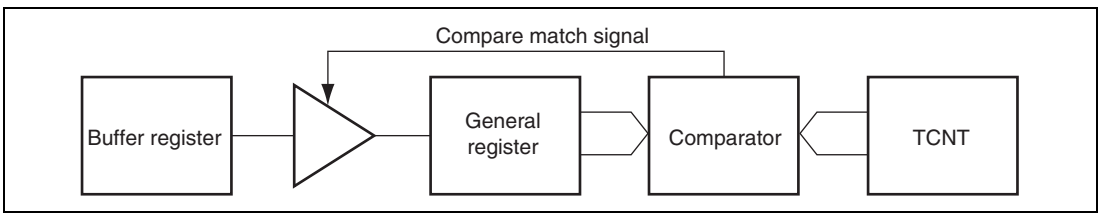


Figure 12.35 Compare Match Buffer Operation

When GR is Input Capture Register: When an input capture occurs, the value in TCNT is transferred to the general register and the value previously stored in the general register is transferred to the buffer register.

This operation is illustrated in figure 12.36.

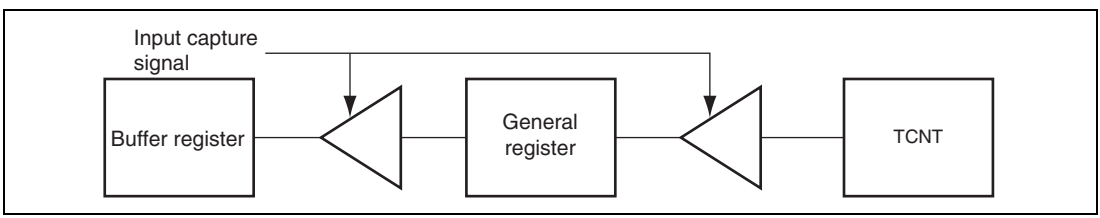


Figure 12.36 Input Capture Buffer Operation

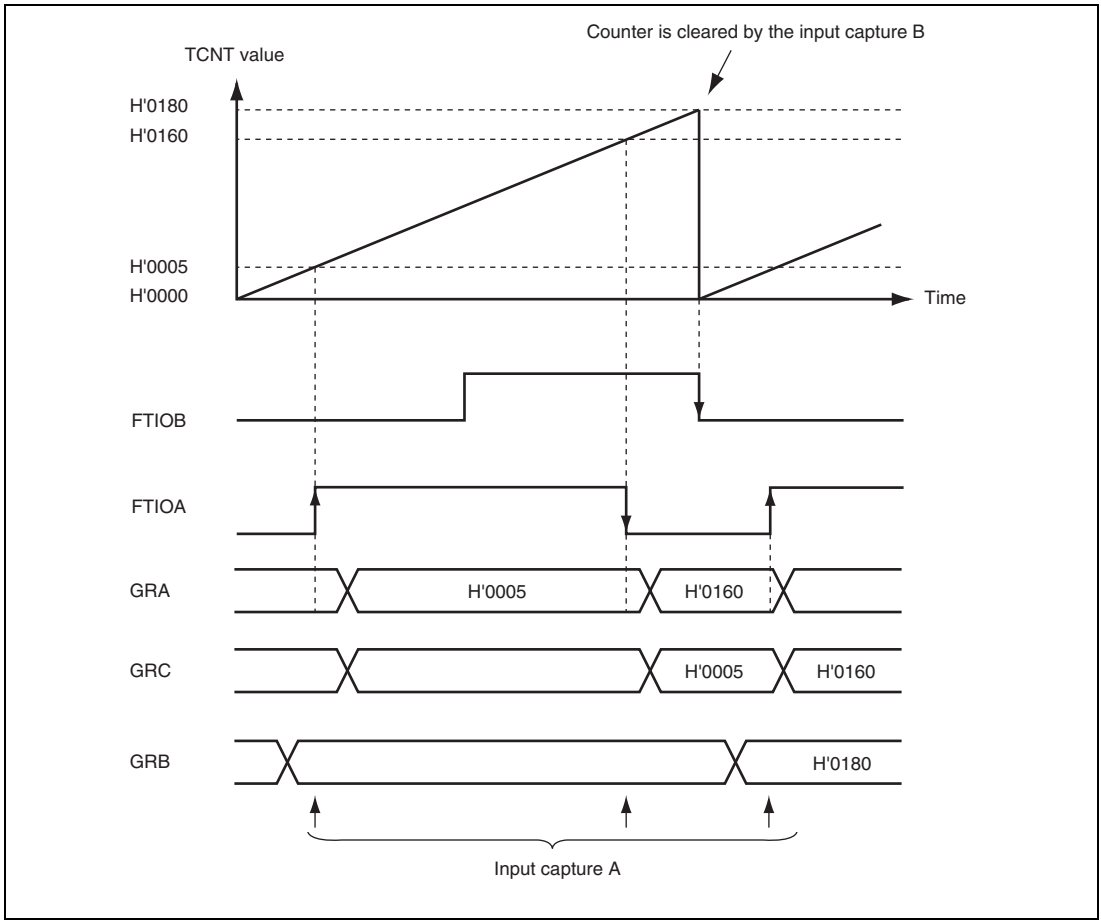


Figure 12.40 Example of Buffer Operation (2)
(Buffer Operation for Input Capture Register)

Section 13 Watchdog Timer

The watchdog timer is an 8-bit timer that can generate an internal reset signal for this LSI if a system crash prevents the CPU from writing to the timer counter, thus allowing it to overflow.

The block diagram of the watchdog timer is shown in figure 13.1.

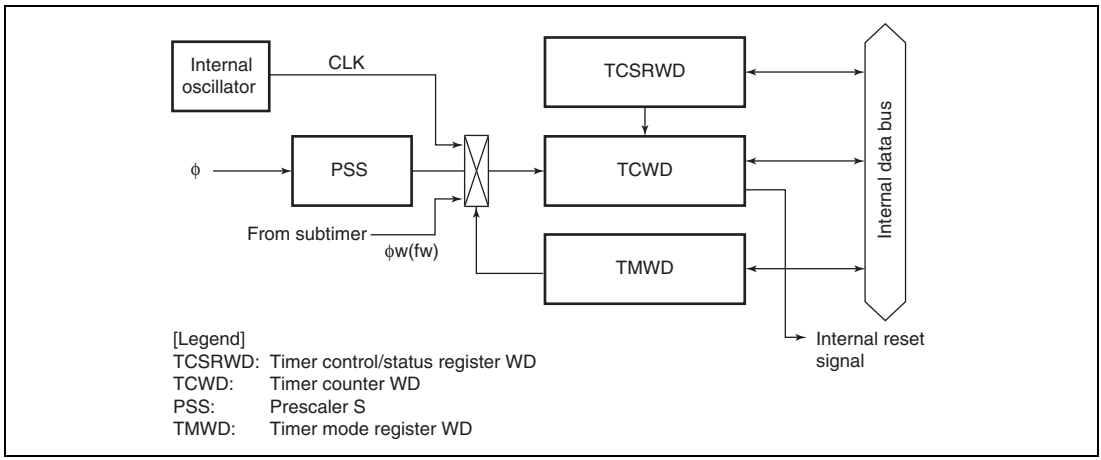


Figure 13.1 Block Diagram of Watchdog Timer

13.1 Features

- Selectable from nine counter input clocks.

  Eight internal clock sources (ϕ/64, ϕ/128, ϕ/256, ϕ/512, ϕ/1024, ϕ/2048, ϕ/4096, and ϕ/8192) or the internal oscillator (WDT and SBT) can be selected as the timer-counter clock. When the internal oscillator is selected, it can operate as the watchdog timer in any operating mode.
- Reset signal generated on counter overflow

  An overflow period of 1 to 256 times the selected clock can be set.

[Legend]
WDT: Watchdog timer
SBT: Subtimer

13.3 Operation

The watchdog timer is provided with an 8-bit counter. If 1 is written to WDON while writing 0 to B2WI when the TCSRWE bit in TCSRWD is set to 1, TCWD begins counting up. (To operate the watchdog timer, two write accesses to TCSRWD are required.) When a clock pulse is input after the TCWD count value has reached H'FF, the watchdog timer overflows and an internal reset signal is generated. The internal reset signal is output for a period of 256 ϕ_{osc} clock cycles. TCWD is a writable counter, and when a value is set in TCWD, the count-up starts from that value. An overflow period in the range of 1 to 256 input clock cycles can therefore be set, according to the TCWD set value.

Figure 13.2 shows an example of watchdog timer operation.

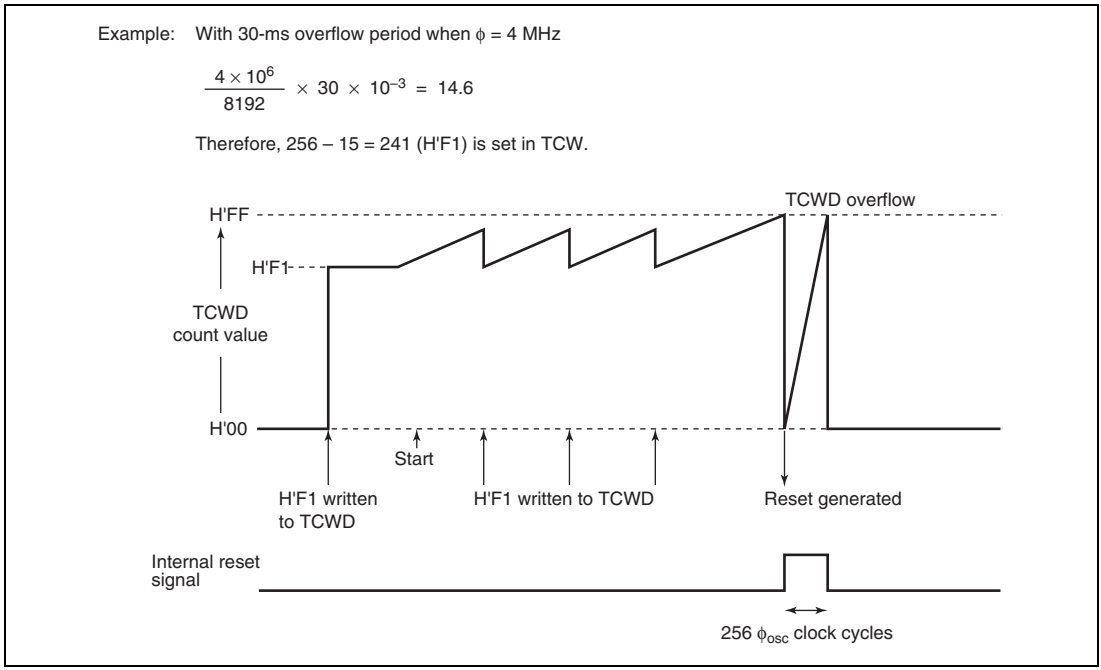


Figure 13.2 Watchdog Timer Operation Example

14.4.4 Serial Data Reception

Figure 14.7 shows an example of operation for reception in asynchronous mode. In serial reception, the SCI3 operates as described below.

1. The SCI3 monitors the communication line. If a start bit is detected, the SCI3 performs internal synchronization, receives receive data in RSR, and checks the parity bit and stop bit.
2. If an overrun error occurs (when reception of the next data is completed while the RDRF flag is still set to 1), the OER bit in SSR is set to 1. If the RIE bit in SCR3 is set to 1 at this time, an ERI interrupt request is generated. Receive data is not transferred to RDR.
3. If a parity error is detected, the PER bit in SSR is set to 1 and receive data is transferred to RDR. If the RIE bit in SCR3 is set to 1 at this time, an ERI interrupt request is generated.
4. If a framing error is detected (when the stop bit is 0), the FER bit in SSR is set to 1 and receive data is transferred to RDR. If the RIE bit in SCR3 is set to 1 at this time, an ERI interrupt request is generated.
5. If reception is completed successfully, the RDRF bit in SSR is set to 1, and receive data is transferred to RDR. If the RIE bit in SCR3 is set to 1 at this time, an RXI interrupt request is generated. Continuous reception is possible because the RXI interrupt routine reads the receive data transferred to RDR before reception of the next receive data has been completed.

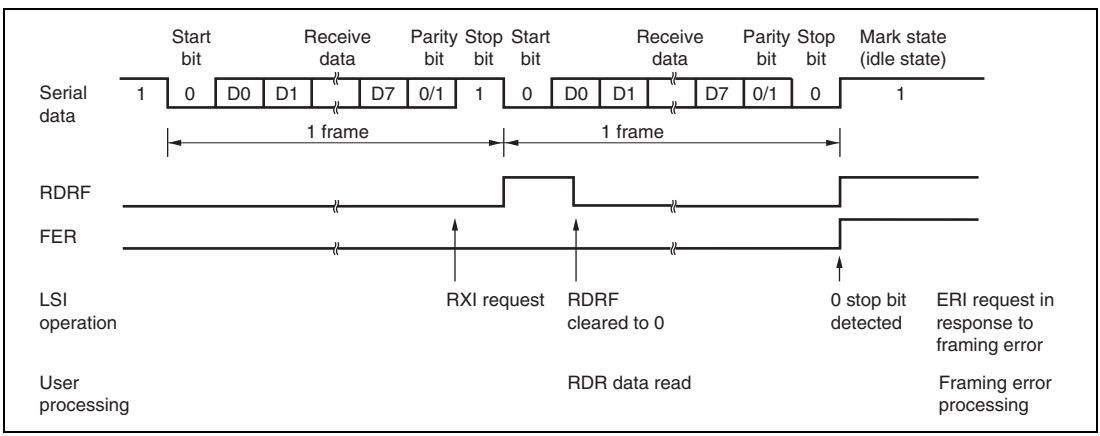


Figure 14.7 Example of SCI3 Reception in Asynchronous Mode (8-Bit Data, Parity, One Stop Bit)

15.3.7 Transmit Pending Register (TXPR)

TXPR sets transmit pending (CAN bus arbitration wait) for the transmit message that is stored in a Mailbox. Setting the corresponding bit in TXPR to 1 enables a message to be transmitted. Writing 0 to the bit in TXPR is ignored.

Bit	Bit Name	Initial Value	R/W	Description
7 to 4	—	All 0	—	Reserved These bits are always read as 0.
3	MB3	0	R/W	[Setting condition] When the corresponding MBCR bit for a mailbox is 0, the corresponding bit in TXPR is set to 1 (n = 3 to 1) [Clearing conditions] • When message transmission has completed successfully (TXACKn set) • When transmission cancellation for an untransmitted message has finished (ABACKn set) • When a transmission cancellation request has occurred during message transmission, and an error occurs or arbitration is lost on the CAN bus (ABACKn set) • When a transmit error or arbitration loss occurred with the corresponding DART bit for a message being transmitted set to 1 If the message is not transmitted successfully, the MBn bit is not cleared to 0. If any of these MB bits in TXPR are cleared to 0, the EMPI bit in TCIRR1 is set to 1. The TinyCAN automatically attempts retransmission as long as the DART bit in the message control of the corresponding Mailbox is not set to 1 or the corresponding bit in TXCR is not set to 1. Note: When the MBn bit in MBCR is set to 1, the TinyCAN does not transmit a message even if the MBn bit in TXPR is set to 1. To clear the MBn bit in TXPR to 0, set the MBn bit in TXCR to 1 beforehand.
2	MB2	0	R/W	
1	MB1	0	R/W	
0	—	0	—	Reserved This bit is always read as 0. This bit is relevant to the receive-only Mailbox, and its value cannot be changed.

19.2 Register Descriptions

The low-voltage detection circuit has the following registers.

- Low-voltage-detection control register (LVDCR)
- Low-voltage-detection status register (LVDSR)

19.2.1 Low-Voltage-Detection Control Register (LVDCR)

LVDCR is used to enable or disable the low-voltage detection circuit, set the detection levels for the LVDR function, enable or disable the LVDR function, and enable or disable generation of an interrupt when the power-supply voltage rises above or falls below the respective levels.

Table 19.1 shows the relationship between the LVDCR settings and select functions. LVDCR should be set according to table 19.1.

Bit	Bit Name	Initial Value	R/W	Description
7	LVDE	0*	R/W	LVD Enable 0: The low-voltage detection circuit is not used (In standby mode) 1: The low-voltage detection circuit is used
6 to 4	—	All 1	—	Reserved These bits are always read as 1 and cannot be modified.
3	LVDSEL	0*	R/W	LVDR Detection Level Select 0: Reset detection voltage is 2.3 V (typ.) 1: Reset detection voltage is 3.6 V (typ.) When the falling or rising voltage detection interrupt is used, reset detection voltage of 2.3 V (typ.) should be used. When only a reset detection interrupt is used, reset detection voltage of 3.6 V (typ.) should be used.
2	LVDRE	0*	R/W	LVDR Enable 0: Disables the LVDR function 1: Enables the LVDR function
1	LVDDE	0	R/W	Voltage-Fall-Interrupt Enable 0: Interrupt on the power-supply voltage falling below the selected detection level disabled 1: Interrupt on the power-supply voltage falling below the selected detection level enabled

21.1 Register Addresses (Address Order)

The data-bus width column indicates the number of bits. The access-state column shows the number of states of the selected basic clock that is required for access to the register.

Note: Access to undefined or reserved addresses should not take place. Correct operation of the access itself or later operations is not guaranteed when such a register is accessed.

Register Name	Abbre-viation	Bit No	Address	Module Name	Data Bus Width	Access State
—	—	—	H'F000 to H'F5FF	—	—	—
Master control register	MCR	8	H'F600	TinyCAN	8	4
General status register	GSR	8	H'F601	TinyCAN	8	4
Bit configuration register 1	BCR1	8	H'F602	TinyCAN	8	4
Bit configuration register 0	BCR0	8	H'F603	TinyCAN	8	4
Mailbox configuration register	MBCR	8	H'F604	TinyCAN	8	4
TinyCAN module control register	TCMR	8	H'F605	TinyCAN	8	4
Transmit pending register	TXPR	8	H'F606	TinyCAN	8	4
Transmit pending cancel register	TXCR	8	H'F608	TinyCAN	8	4
Transmit acknowledge register	TXACK	8	H'F60A	TinyCAN	8	4
Abort acknowledge register	ABACK	8	H'F60C	TinyCAN	8	4
Receive complete register	RXPR	8	H'F60E	TinyCAN	8	4
Remote request register	RFPR	8	H'F610	TinyCAN	8	4
TinyCAN interrupt register 1	TCIRR1	8	H'F612	TinyCAN	8	4
TinyCAN interrupt register 0	TCIRR0	8	H'F613	TinyCAN	8	4
Mailbox interrupt mask register	MBIMR	8	H'F614	TinyCAN	8	4
TinyCAN interrupt mask register 1	TCIMR1	8	H'F616	TinyCAN	8	4
TinyCAN interrupt mask register 0	TCIMR0	8	H'F617	TinyCAN	8	4
Receive error counter	REC	8	H'F618	TinyCAN	8	4
Transmit error counter	TEC	8	H'F619	TinyCAN	8	4
Test control register	TCR	8	H'F61A	TinyCAN	8	4
Unread message status register	UMSR	8	H'F61B	TinyCAN	8	4
Message control 0 [0]	MC0[0]	8	H'F620	TinyCAN	8	4

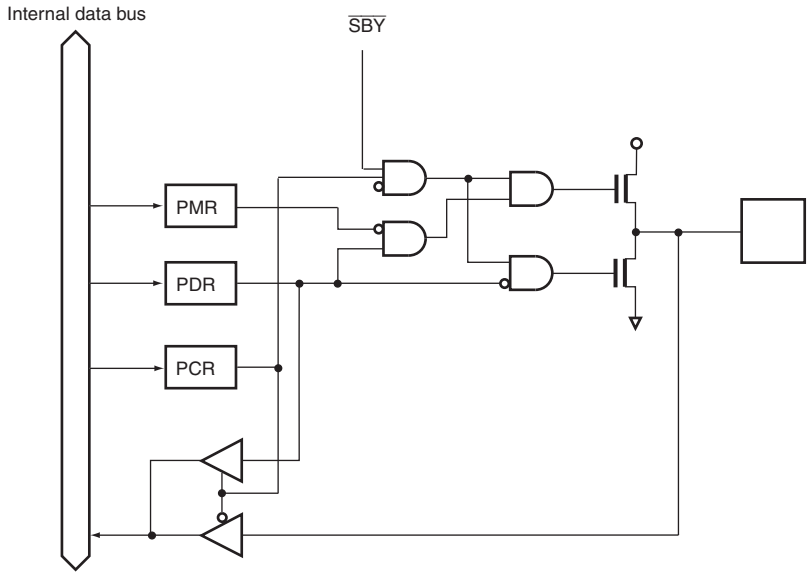
Register Abbreviation	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name
SSCRH	MSS	BIDE	SOOS	SOL	SOLP	SCKS	CSS1	CSS0	SSU
SSCRL	MSTSSU	SSUMS	SRES	SCKOS	CSOS	—	—	—	
SSMR	MLS	CPOS	CPHS	—	—	CKS2	CKS1	CKS0	
SSER	TE	RE	RSSTP	—	TEIE	TIE	RIE	CEIE	
SSSR	—	ORER	—	—	TEND	TDRE	RDRF	CE	
SSRDR	SSRDR7	SSRDR6	SSRDR5	SSRDR4	SSRDR3	SSRDR2	SSRDR1	SSRDR0	
SSTDR	SSTDR7	SSTDR6	SSTDR5	SSTDR4	SSTDR3	SSTDR2	SSTDR1	SSTDR0	
SBTCTL	PCEF	—	—	START	OSCEB	SYSCKS	SBTIB	SBTUF	Subtimer
SBTDCNT	SBTDCNT7	SBTDCNT6	SBTDCNT5	SBTDCNT4	SBTDCNT3	SBTDCNT2	SBTDCNT1	SBTDCNT0	
ROPCR	ROPCR7	ROPCR6	ROPCR5	ROPCR4	ROPCR3	ROPCR2	ROPCR1	ROPCR0	
TCR_0	CCLR2	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0	Timer Z
TIORA_0	—	IOB2	IOB1	IOB0	—	IOA2	IOA1	IOA0	
TIORC_0	—	IOD2	IOD1	IOD0	—	IOC2	IOC1	IOC0	
TSR_0	—	—	—	OVF	IMFD	IMFC	IMFB	IMFA	
TIER_0	—	—	—	OVIE	IMIED	IMIEC	IMIEB	IMIEA	
POCR_0	—	—	—	—	—	POLD	POLC	POLB	
TCNT_0	TCNT0H7	TCNT0H6	TCNT0H5	TCNT0H4	TCNT0H3	TCNT0H2	TCNT0H1	TCNT0H0	
	TCNT0L7	TCNT0L6	TCNT0L5	TCNT0L4	TCNT0L3	TCNT0L2	TCNT0L1	TCNT0L0	
GRA_0	GRA0H7	GRA0H6	GRA0H5	GRA0H4	GRA0H3	GRA0H2	GRA0H1	GRA0H0	
	GRA0L7	GRA0L6	GRA0L5	GRA0L4	GRA0L3	GRA0L2	GRA0L1	GRA0L0	
GRB_0	GRB0H7	GRB0H6	GRB0H5	GRB0H4	GRB0H3	GRB0H2	GRB0H1	GRB0H0	
	GRB0L7	GRB0L6	GRB0L5	GRB0L4	GRB0L3	GRB0L2	GRB0L1	GRB0L0	
GRC_0	GRC0H7	GRC0H6	GRC0H5	GRC0H4	GRC0H3	GRC0H2	GRC0H1	GRC0H0	
	GRC0L7	GRC0L6	GRC0L5	GRC0L4	GRC0L3	GRC0L2	GRC0L1	GRC0L0	
GRD_0	GRD0H7	GRD0H6	GRD0H5	GRD0H4	GRD0H3	GRD0H2	GRD0H1	GRD0H0	
	GRD0L7	GRD0L6	GRD0L5	GRD0L4	GRD0L3	GRD0L2	GRD0L1	GRD0L0	
TCR_1	CCLR2	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0	
TIORA_1	—	IOB2	IOB1	IOB0	—	IOA2	IOA1	IOA0	
TIORC_1	—	IOD2	IOD1	IOD0	—	IOC2	IOC1	IOC0	
TSR_1	—	—	UDF	OVF	IMFD	IMFC	IMFB	IMFA	
TIER_1	—	—	—	OVIE	IMIED	IMIEC	IMIEB	IMIEA	
POCR_1	—	—	—	—	—	POLD	POLC	POLB	

22.3.3 AC Characteristics

Table 22.14 AC Characteristics

V_{CC} = 2.7 to 5.5 V, V_{SS} = 0.0 V, T_a = –20 to +75°C (regular specifications) or T_a = –40 to +85°C (wide-range specifications), unless otherwise indicated.

Item	Symbol	Applicable Pins	Test Condition	Values			Unit	Reference Figure
				Min.	Typ.	Max.		
System clock oscillation frequency	f_{OSC}	OSC1, OSC2	VCC = 4.0 to 5.5 V	2.0	—	20.0	MHz	*1
				2.0		10.0		
System clock (ϕ) cycle time	t_{cyc}			1	—	64	t_{OSC}	*2
				—	—	12.8	µs	
Subclock oscillator oscillation frequency	f_{RO}		V_{CC} = 4.0 to 5.5 V	64.0	—	850.0	kHz	
Subclock oscillator (ϕw) cycle time	t_{RO}		V_{CC} = 4.0 to 5.5 V	1.18	—	15.6	µs	
Subclock (ϕsub) cycle time	t_{subcyc}		V_{CC} = 4.0 to 5.5 V	2	—	8	ϕw	
Instruction cycle time				2	—	—	t_{cyc} t_{subcyc}	
Oscillation stabilization time (crystal resonator)	t_{rc}	OSC1, OSC2		—	—	10.0	ms	
Oscillation stabilization time (ceramic resonator)	t_{rc}	OSC1, OSC2		—	—	5.0	ms	
External clock high width	t_{CPH}	OSC1	V_{CC} = 4.0 to 5.5 V	20.0	—	—	ns	Figure 22.1
				40.0	—	—		
External clock low width	t_{CPL}	OSC1	V_{CC} = 4.0 to 5.5 V	20.0	—	—	ns	
				40.0	—	—		
External clock rise time	t_{CPr}	OSC1	V_{CC} = 4.0 to 5.5 V	—	—	10.0	ns	
				—	—	15.0		
External clock fall time	t_{CPf}	OSC1	V_{CC} = 4.0 to 5.5 V	—	—	10.0	ns	
				—	—	15.0		



[Legend]
PMR : Port mode register
PDR : Port data register
PCR : Port control register

Figure B.9 Port 5 Block Diagram (P57, P56)