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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300H
Core Size	16-Bit
Speed	20MHz
Connectivity	CANbus, SCI, SSU
Peripherals	PWM, WDT
Number of I/O	45
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df36054fpjv

2.5 Addressing Modes and Effective Address Calculation

The following describes the H8/300H CPU. In this LSI, the upper eight bits are ignored in the generated 24-bit address, so the effective address is 16 bits.

2.5.1 Addressing Modes

The H8/300H CPU supports the eight addressing modes listed in table 2.10. Each instruction uses a subset of these addressing modes. Addressing modes that can be used differ depending on the instruction. For details, refer to appendix A.4, Combinations of Instructions and Addressing Modes.

Arithmetic and logic instructions can use the register direct and immediate modes. Data transfer instructions can use all addressing modes except program-counter relative and memory indirect. Bit-manipulation instructions use register direct, register indirect, or the absolute addressing mode (@aa:8) to specify an operand, and register direct (BSET, BCLR, BNOT, and BTST instructions) or immediate (3-bit) addressing mode to specify a bit number in the operand.

Table 2.10 Addressing Modes

No.	Addressing Mode	Symbol
1	Register direct	Rn
2	Register indirect	@ERn
3	Register indirect with displacement	@(d:16,ERn)/@(d:24,ERn)
4	Register indirect with post-increment Register indirect with pre-decrement	@ERn+ @–ERn
5	Absolute address	@aa:8/@aa:16/@aa:24
6	Immediate	#xx:8/#xx:16/#xx:32
7	Program-counter relative	@(d:8,PC)/@(d:16,PC)
8	Memory indirect	@@aa:8

(1) Register Direct—Rn

The register field of the instruction specifies an 8-, 16-, or 32-bit general register containing the operand. R0H to R7H and R0L to R7L can be specified as 8-bit registers. R0 to R7 and E0 to E7 can be specified as 16-bit registers. ER0 to ER7 can be specified as 32-bit registers.

- After executing BSET instruction

	P57	P56	P55	P54	P53	P52	P51	P50
Input/output	Input	Input	Output	Output	Output	Output	Output	Output
Pin state	Low level	High level	Low level	Low level	Low level	Low level	Low level	High level
PCR5	0	0	1	1	1	1	1	1
PDR5	0	1	0	0	0	0	0	1

- Description on operation

1. When the BSET instruction is executed, first the CPU reads port 5.
   Since P57 and P56 are input pins, the CPU reads the pin states (low-level and high-level input).
   P55 to P50 are output pins, so the CPU reads the value in PDR5. In this example PDR5 has a value of H'80, but the value read by the CPU is H'40.
2. Next, the CPU sets bit 0 of the read data to 1, changing the PDR5 data to H'41.
3. Finally, the CPU writes H'41 to PDR5, completing execution of BSET instruction.

As a result of the BSET instruction, bit 0 in PDR5 becomes 1, and P50 outputs a high-level signal. However, bits 7 and 6 of PDR5 end up with different values. To prevent this problem, store a copy of the PDR5 data in a work area in memory. Perform the bit manipulation on the data in the work area, then write this data to PDR5.

- Prior to executing BSET instruction

```
MOV.B   #80,  R0L
MOV.B   R0L,  @RAM0
MOV.B   R0L,  @PDR5
```

The PDR5 value (H'80) is written to a work area in memory (RAM0) as well as to PDR5.

	P57	P56	P55	P54	P53	P52	P51	P50
Input/output	Input	Input	Output	Output	Output	Output	Output	Output
Pin state	Low level	High level	Low level	Low level	Low level	Low level	Low level	Low level
PCR5	0	0	1	1	1	1	1	1
PDR5	1	0	0	0	0	0	0	0
RAM0	1	0	0	0	0	0	0	0

Relative Module	Exception Sources	Vector Number	Vector Address	Priority
Timer Z	Compare match/input capture A0 to D0 Timer Z overflow	26	H'0034 to H'0035	High
	Compare match/input capture A1 to D1 Timer Z overflow Timer Z underflow	27	H'0036 to H'0037	
Timer B1	Timer B1 overflow	29	H'003A to H'003B	
SCI3_2*[2]	Receive data full Transmit data empty Transmit end Receive error	32	H'0040 to H'0041	
TinyCAN	Error Reset/HALT mode processing Message reception Message transmission Wakeup	34	H'0044 to H'0045	
SSU	Overrun error Transmit data empty Transmit end Receive data full Conflict error	35	H'0046 to H'0047	
Subtimer	Underflow	36	H'0048 to H'0049	Low

Notes: 1. A low-voltage detection interrupt is enabled only in the product with an on-chip power-on reset and low-voltage detection circuit.
2. The H8/36037 Group does not have the SCI3_2.

6.1.4 Module Standby Control Register 2 (MSTCR2)

MSTCR2 allows the on-chip peripheral modules to enter a standby state in module units.

Bit	Bit Name	Initial Value	R/W	Description
7	MSTS3_2	0	R/W	SCI3_2 Module Standby The SCI3_2 enters standby mode when this bit is set to 1. Note: This bit is reserved in the H8/36037 Group. This bit is always read as 0.
6, 5	—	All 0	—	Reserved These bits are always read as 0.
4	MSTTB1	0	R/W	Timer B1 Module Standby The timer B1 enters standby mode when this bit is set to 1.
3, 2	—	All 0	—	Reserved These bits are always read as 0.
1	MSTTZ	0	R/W	Timer Z Module Standby The timer Z enters standby mode when this bit is set to 1.
0	—	0	—	Reserved This bit is always read as 0.

9.1.1 Port Mode Register 1 (PMR1)

PMR1 switches the functions of pins in port 1 and port 2.

Bit	Bit Name	Initial Value	R/W	Description
7	IRQ3	0	R/W	This bit selects the function of pin P17/$\overline{\text{IRQ3}}$/TRGV. 0: General I/O port 1: $\overline{\text{IRQ3}}$/TRGV input pin
6	IRQ2	0	R/W	This bit selects the function of pin P16/$\overline{\text{IRQ2}}$. 0: General I/O port 1: $\overline{\text{IRQ2}}$ input pin
5	IRQ1	0	R/W	This bit selects the function of pin P15/$\overline{\text{IRQ1}}$/TMIB1. 0: General I/O port 1: $\overline{\text{IRQ1}}$/TMIB1 input pin
4	IRQ0	0	R/W	This bit selects the function of pin P14/$\overline{\text{IRQ0}}$. 0: General I/O port 1: $\overline{\text{IRQ0}}$ input pin
3	TXD2	0	R/W	This bit selects the function of pin P72/TXD_2. 0: General I/O port 1: TXD_2 output pin Note: This bit is reserved in the H8/36037 Group. This bit is always read as 0.
2	—	0	—	Reserved. This bit is always read as 0.
1	TXD	0	R/W	This bit selects the function of pin P22/TXD. 0: General I/O port 1: TXD output pin
0	—	0	—	Reserved. This bit is always read as 0.

- P16/$\overline{\text{IRQ2}}$ pin

Register	PMR1	PCR1	
Bit Name	**IRQ2**	**PCR16**	**Pin Function**
Setting value	0	0	P16 input pin
		1	P16 output pin
	1	X	$\overline{\text{IRQ2}}$ input pin

[Legend]
X: Don't care.

- P15/$\overline{\text{IRQ1}}$/TMIB1 pin

Register	PMR1	PCR1	
Bit Name	**IRQ1**	**PCR15**	**Pin Function**
Setting value	0	0	P15 input pin
		1	P15 output pin
	1	X	$\overline{\text{IRQ1}}$ input/TMIB1 input pin

[Legend]
X: Don't care.

- P14/$\overline{\text{IRQ0}}$ pin

Register	PMR1	PCR1	
Bit Name	**IRQ0**	**PCR14**	**Pin Function**
Setting value	0	0	P14 input pin
		1	P14 output pin
	1	X	$\overline{\text{IRQ0}}$ input pin

[Legend]
X: Don't care.

- P12 pin

Register	PCR1	
Bit Name	**PCR12**	**Pin Function**
Setting value	0	P12 input pin
	1	P12 output pin

9.2.1 Port Control Register 2 (PCR2)

PCR2 selects inputs/outputs in bit units for pins to be used as general I/O ports of port 2.

Bit	Bit Name	Initial Value	R/W	Description
7 to 5	—	—	—	Reserved
4	PCR24	0	W	When each of the port 2 pins P24 to P20 functions as a general I/O port, setting a PCR2 bit to 1 makes the corresponding pin an output port, while clearing the bit to 0 makes the pin an input port.
3	PCR23	0	W	
2	PCR22	0	W	
1	PCR21	0	W	
0	PCR20	0	W	

9.2.2 Port Data Register 2 (PDR2)

PDR2 is a general I/O port data register of port 2.

Bit	Bit Name	Initial Value	R/W	Description
7 to 5	—	All 1	—	Reserved These bits are always read as 1.
4	P24	0	R/W	PDR2 stores output data for port 2 pins.
3	P23	0	R/W	If PDR2 is read while PCR2 bits are set to 1, the value stored in PDR2 is read. If PDR2 is read while PCR2 bits are cleared to 0, the pin states are read regardless of the value stored in PDR2.
2	P22	0	R/W	
1	P21	0	R/W	
0	P20	0	R/W	

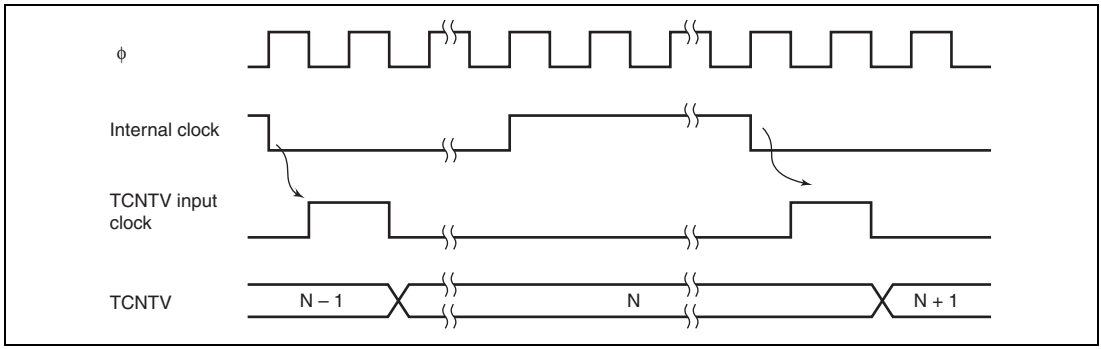

Figure 11.2 Increment Timing with Internal Clock

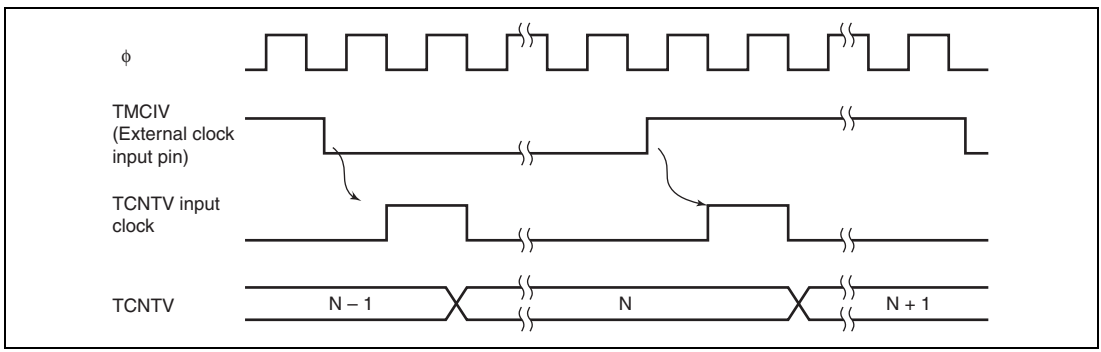

Figure 11.3 Increment Timing with External Clock

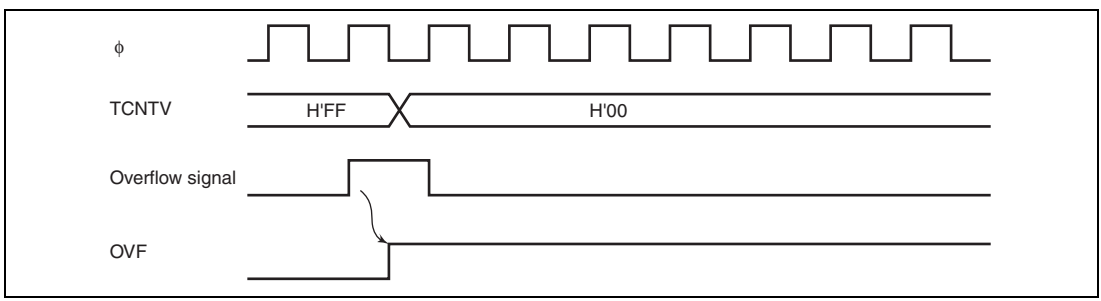

Figure 11.4 OVF Set Timing

12.2 Input/Output Pins

Table 12.2 summarizes the timer Z pins.

Table 12.2 Pin Configuration

Name	Abbreviation	I/O	Function
Input capture/output compare A0	FTIOA0	I/O	GRA_0 output compare output, GRA_0 input capture input, or external clock input (TCLK)
Input capture/output compare B0	FTIOB0	I/O	GRB_0 output compare output, GRB_0 input capture input, or PWM output
Input capture/output compare C0	FTIOC0	I/O	GRC_0 output compare output, GRC_0 input capture input, or PWM synchronous output (in reset synchronous PWM and complementary PWM modes)
Input capture/output compare D0	FTIOD0	I/O	GRD_0 output compare output, GRD_0 input capture input, or PWM output
Input capture/output compare A1	FTIOA1	I/O	GRA_1 output compare output, GRA_1 input capture input, or PWM output (in reset synchronous PWM and complementary PWM modes)
Input capture/output compare B1	FTIOB1	I/O	GRB_1 output compare output, GRB_1 input capture input, or PWM output
Input capture/output compare C1	FTIOC1	I/O	GRC_1 output compare output, GRC_1 input capture input, or PWM output
Input capture/output compare D1	FTIOD1	I/O	GRD_1 output compare output, GRD_1 input capture input, or PWM output

12.3.10 Timer I/O Control Register (TIORA and TIORC)

The TIOR registers control the general registers (GR). Timer Z has four TIOR registers (TIORA_0, TIORA_1, TIORC_0, and TIORC_1), two for each channel. In PWM mode including complementary PWM mode and reset synchronous PWM mode, the settings of TIOR are invalid.

TIORA: TIORA selects whether GRA or GRB is used as an output compare register or an input capture register. When an output compare register is selected, the output setting is selected. When an input capture register is selected, an input edge of an input capture signal is selected. TIORA also selects the function of FTIOA or FTIOB pin.

Bit	Bit Name	Initial Value	R/W	Description
7	—	1	—	Reserved This bit is always read as 1.
6	IOB2	0	R/W	I/O Control B2 to B0
5	IOB1	0	R/W	GRB is an output compare register:
4	IOB0	0	R/W	000: Disables pin output by compare match 001: 0 output by GRB compare match 010: 1 output by GRB compare match 011: Toggle output by GRB compare match GRB is an input capture register: 100: Input capture to GRB at the rising edge 101: Input capture to GRB at the falling edge 11X: Input capture to GRB at both rising and falling edges
3	—	1	—	Reserved This bit is always read as 1.

12.4.6 Reset Synchronous PWM Mode

Three normal- and counter-phase PWM waveforms are output by combining channels 0 and 1 that one of changing points of waveforms will be common.

In reset synchronous PWM mode, the FTIOB0 to FTIOD0 and FTIOA1 to FTIOD1 pins become PWM-output pins automatically. TCNT_0 performs an increment operation. Tables 12.4 and 12.5 show the PWM-output pins used and the register settings, respectively.

Figure 12.26 shows the example of reset synchronous PWM mode setting procedure.

Table 12.4 Output Pins in Reset Synchronous PWM Mode

Channel	Pin Name	I/O	Pin Function
0	FTIOC0	Output	Toggle output in synchronous with PWM cycle
0	FTIOB0	Output	PWM output 1
0	FTIOD0	Output	PWM output 1 (counter-phase waveform of PWM output 1)
1	FTIOA1	Output	PWM output 2
1	FTIOC1	Output	PWM output 2 (counter-phase waveform of PWM output 2)
1	FTIOB1	Output	PWM output 3
1	FTIOD1	Output	PWM output 3 (counter-phase waveform of PWM output 3)

Table 12.5 Register Settings in Reset Synchronous PWM Mode

Register	Description
TCNT_0	Initial setting of H'0000
TCNT_1	Not used (independently operates)
GRA_0	Sets counter cycle of TCNT_0
GRB_0	Set a changing point of the PWM waveform output from pins FTIOB0 and FTIOD0.
GRA_1	Set a changing point of the PWM waveform output from pins FTIOA1 and FTIOC1.
GRB_1	Set a changing point of the PWM waveform output from pins FTIOB1 and FTIOD1.

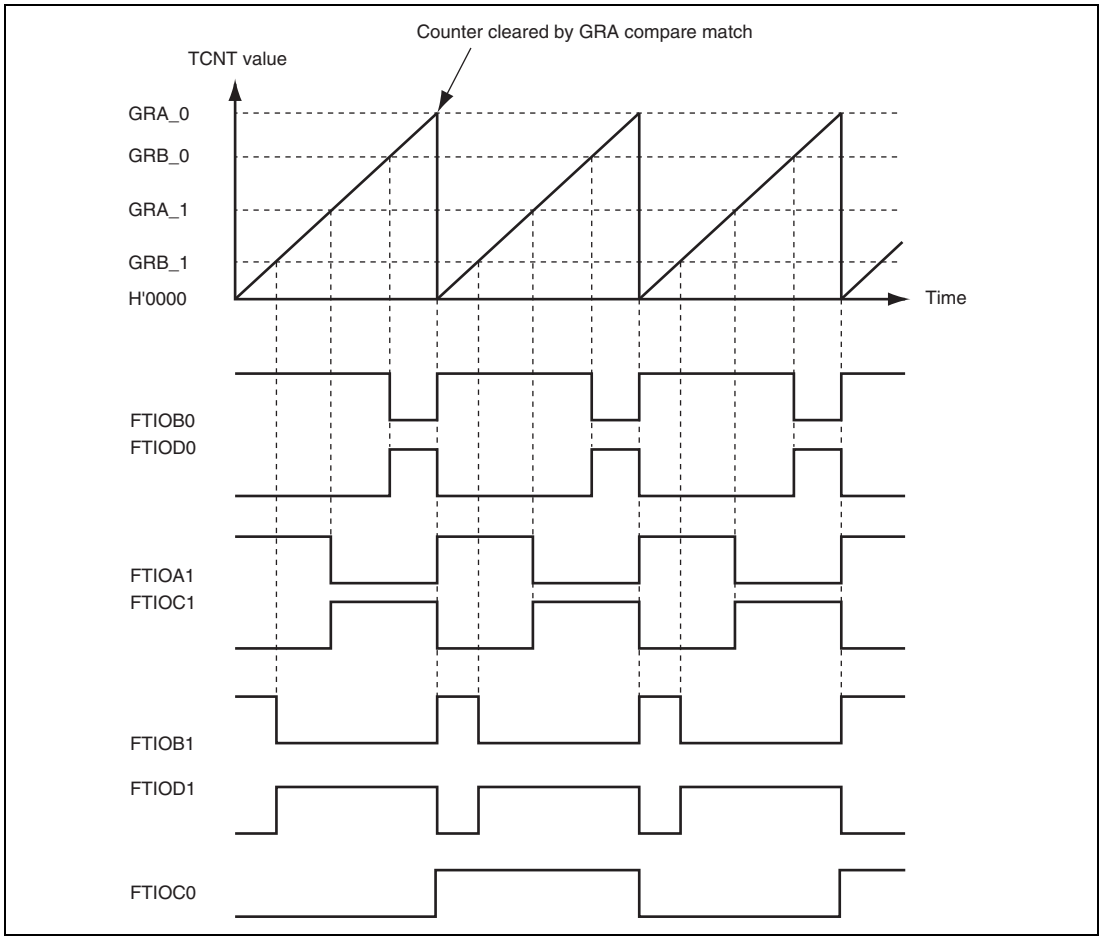

Figure 12.28 Example of Reset Synchronous PWM Mode Operation (OLS0 = OLS1 = 0)

In reset synchronous PWM mode, TCNT_0 and TCNT_1 perform increment and independent operations, respectively. However, GRA_1 and GRB_1 are separated from TCNT_1. When a compare match occurs between TCNT_0 and GRA_0, a counter is cleared and an increment operation is restarted from H'0000.

The PWM pin outputs 0 or 1 whenever a compare match between GRB_0, GRA_1, GRB_1 and TCNT_0 or counter clearing occur.

For details on operations when reset synchronous PWM mode and buffer operation are simultaneously set, refer to section 12.4.8, Buffer Operation.

15.3.7 Transmit Pending Register (TXPR)

TXPR sets transmit pending (CAN bus arbitration wait) for the transmit message that is stored in a Mailbox. Setting the corresponding bit in TXPR to 1 enables a message to be transmitted. Writing 0 to the bit in TXPR is ignored.

Bit	Bit Name	Initial Value	R/W	Description
7 to 4	—	All 0	—	Reserved These bits are always read as 0.
3	MB3	0	R/W	[Setting condition] When the corresponding MBCR bit for a mailbox is 0, the corresponding bit in TXPR is set to 1 (n = 3 to 1) [Clearing conditions] • When message transmission has completed successfully (TXACKn set) • When transmission cancellation for an untransmitted message has finished (ABACKn set) • When a transmission cancellation request has occurred during message transmission, and an error occurs or arbitration is lost on the CAN bus (ABACKn set) • When a transmit error or arbitration loss occurred with the corresponding DART bit for a message being transmitted set to 1 If the message is not transmitted successfully, the MBn bit is not cleared to 0. If any of these MB bits in TXPR are cleared to 0, the EMPI bit in TCIRR1 is set to 1. The TinyCAN automatically attempts retransmission as long as the DART bit in the message control of the corresponding Mailbox is not set to 1 or the corresponding bit in TXCR is not set to 1. Note: When the MBn bit in MBCR is set to 1, the TinyCAN does not transmit a message even if the MBn bit in TXPR is set to 1. To clear the MBn bit in TXPR to 0, set the MBn bit in TXCR to 1 beforehand.
2	MB2	0	R/W	
1	MB1	0	R/W	
0	—	0	—	Reserved This bit is always read as 0. This bit is relevant to the receive-only Mailbox, and its value cannot be changed.

15.3.14 TinyCAN Interrupt Registers 0, 1 (TCIRR0, TCIRR1)

TCIRR is a status flag for each interrupt source.

- TCIRR0

Bit	Bit Name	Initial Value	R/W	Description
7	OVLI	0	R/(W)*	Overload Frame Transmit Interrupt Flag Status flag indicating that the TinyCAN has transmitted an overload frame. [Setting condition] When an overload frame is transmitted [Clearing condition] When 1 is written to this bit
6	BOFI	0	R/(W)*	Bus Off Interrupt Flag Status flag indicating the bus off state caused by the TEC or recovery from the bus off state to the error-active state. [Setting condition] When TEC ≥ 256 or when 11 bits are received for 128 times in the bus off state [Clearing condition] When 1 is written to this bit
5	EPI	0	R/(W)*	Error Passive Interrupt Flag Status flag indicating the error-passive state caused by REC or TEC. [Setting condition] When TEC ≥ 128 or REC ≥ 128 [Clearing condition] When 1 is written to this bit
4	ROWI	0	R/(W)*	Receive Overload Warning Interrupt Flag Status flag indicating the error warning state caused by REC. [Setting condition] When REC ≥ 96 [Clearing condition] When 1 is written to this bit

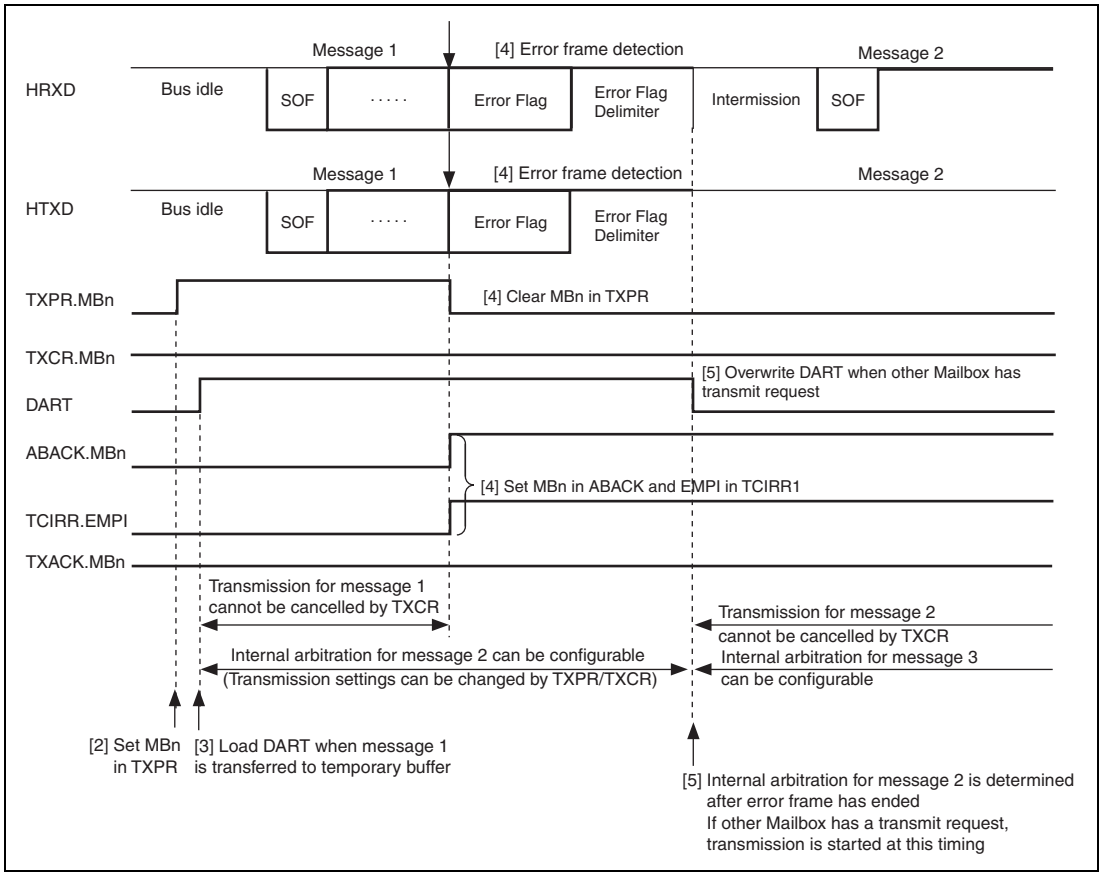

Figure 15.13 Internal Arbitration at Error Detection (DART = 1)

16.4.8 Serial Data Transmission

Figure 16.11 shows an example of the SSU operation for transmission. In serial transmission, the SSU operates as described below.

When the SSU is set as a master device, it outputs a synchronous clock and data. When the SSU is set as a slave device, the $\overline{\text{SCS}}$ pin is in the low-input state and the SSU outputs data in synchronized with the input clock.

When the SSU writes transmit data in SSTDR after setting the TE bit to 1, the TDRE flag is automatically cleared to 0 and data is transferred from SSTDR to SSTRSR. Then the SSU sets the TDRE flag to 1 and starts transmission. If the TIE bit in SSER is set to 1 at this time, a TXI is generated.

When the TDRE flag is 0 and one frame of data has transferred, data is transferred from SSTDR to SSTRSR and serial transmission of the next frame is started. If the eighth bit is transmitted while the TDRE flag is 1, the TEND bit in SSSR is set to 1 and the state is retained. If the TEIE bit in SSER is set to 1 at this time, a TEI is generated. After transmission is ended, the SSCK pin is fixed high and the $\overline{\text{SCS}}$ pin goes high. When continuous transmission is performed with the $\overline{\text{SCS}}$ pin low, the next data should be written to SSTDR before transmitting the eighth bit of the frame.

While the ORER bit in SSSR is set to 1, transmission cannot be performed. Therefore confirm that the ORER bit is cleared to 0 before transmission.

The difference between this mode and clocked synchronous communication mode is as follows: when the SSU is set as a master device, the SSO pin is in the Hi-Z state if the $\overline{\text{SCS}}$ pin is in the Hi-Z state and when the SSU is set as a slave device, the SSI pin is in the Hi-Z state if the $\overline{\text{SCS}}$ pin is in the high-input state. The sample flowchart for serial data transmission is the same as that in clocked synchronous communication mode.

16.4.10 $\overline{\text{SCS}}$ Pin Control and Arbitration

When the SSUMS bit in SSCRL is set to 1 and the CSS1 bit in SSCRH is set to 1, the MSS bit in SSCRH is set to 1 and then the arbitration of the $\overline{\text{SCS}}$ pin is checked before starting serial transfer. If the SSU detects that the synchronized internal SCS pin goes low in this period, the CE bit in SSSR is set and the MSS bit is cleared.

Note: When a conflict error is set, subsequent transmit operation is not possible. Therefore the CE bit must be cleared to 0 before starting transmission.
When the multimaster error is used, the CSOS bit in SSCRL should be set to 1.

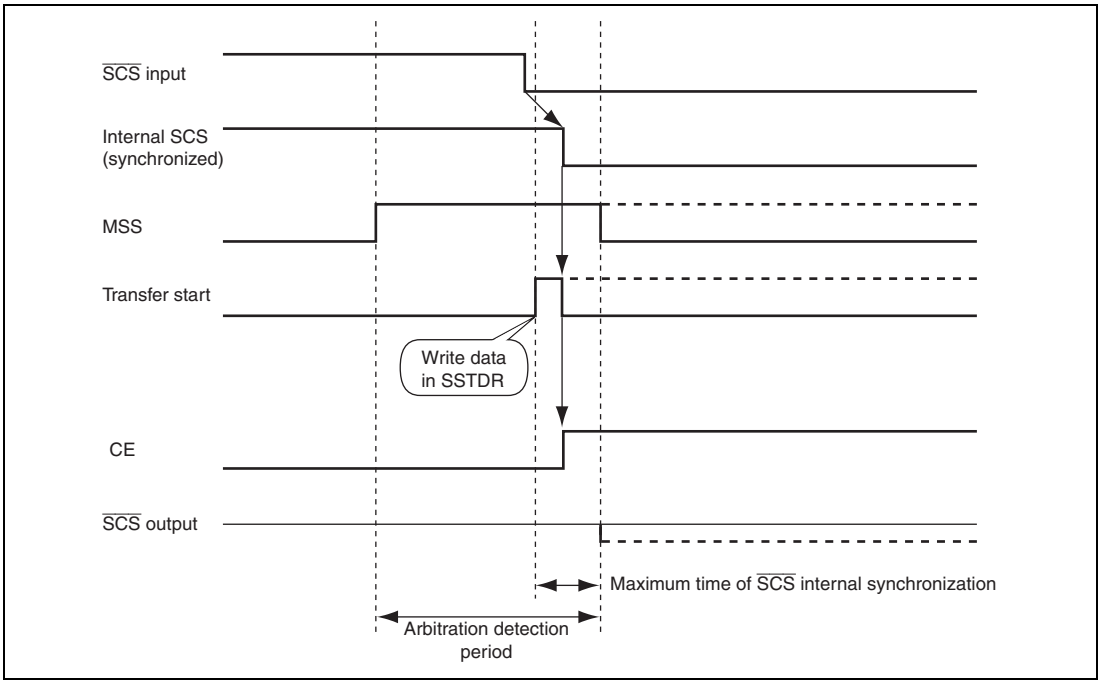

Figure 16.13 Arbitration Check Timing

Item	Symbol	Applicable Pins	Test Condition	Values Min.	Typ.	Max.	Unit	Notes
Input low voltage	V_{IL}	$\overline{RES}$, $\overline{NMI}$, $\overline{WKP0}$ to $\overline{WKP5}$, $\overline{IRQ0}$ to $\overline{IRQ3}$, $\overline{ADTRG}$, TMRIV, TMCIV, FTIOA0 to FTIOD0, FTIOA1 to FTIOD1, SCK3, SCK3_2*[1], $\overline{SCS}$, SSCK, TRGV, TMIB1	V_{CC} = 4.0 to 5.5 V	–0.3	—	$V_{CC} \times 0.2$	V	
				–0.3	—	$V_{CC} \times 0.1$		
		RXD, RXD_2*[1], SSI, SSO, HRXD, P10 to P12, P14 to P17, P20 to P24, P50 to P57, P60 to P67, P70 to P72, P74 to P76, P85 to P87, P90 to P97	V_{CC} = 4.0 to 5.5 V	–0.3	—	$V_{CC} \times 0.3$	V	
				–0.3	—	$V_{CC} \times 0.2$		
		PB0 to PB7	V_{CC} = 4.0 to 5.5 V	–0.3	—	$V_{CC} \times 0.3$	V	
				–0.3	—	$V_{CC} \times 0.2$		
		OSC1	V_{CC} = 4.0 to 5.5 V	–0.3	—	0.5	V	
				–0.3	—	0.3		
Output high voltage	V_{OH}	P10 to P12, P14 to P17, P20 to P24, P50 to P55, P60 to P67, P70 to P72, P74 to P76, P85 to P87, P90 to P97	V_{CC} = 4.0 to 5.5 V, $-I_{OH}$ = 1.5 mA	V_{CC} – 1.0	—	—	V	
			$-I_{OH}$ = 0.1 mA	V_{CC} – 0.5	—	—		
		P56, P57	V_{CC} = 4.0 to 5.5 V, $-I_{OH}$ = 0.1 mA	V_{CC} – 2.5	—	—	V	
			V_{CC} = 3.0 to 4.0 V, $-I_{OH}$ = 0.1 mA	V_{CC} – 2.0	—	—		

Table 22.15 Serial Communication Interface (SCI) Timing

V_{CC} = 2.7 to 5.5 V, V_{SS} = 0.0 V, T_a = –20 to +75°C (regular specifications) or T_a = –40 to +85°C (wide-range specifications), unless otherwise indicated.

Item		Symbol	Applicable Pins	Test Condition	Values Min.	Typ.	Max.	Unit	Reference Figure
Input clock cycle	Asynchronous	t_{scyc}	SCK3, SCK3_2*		4	—	—	t_{cyc}	Figure 22.4
	Clocked synchronous				6	—	—		
Input clock pulse width		t_{SCKW}	SCK3, SCK3_2*		0.4	—	0.6	t_{scyc}	
Transmit data delay time (clocked synchronous)		t_{TXD}	TXD, TXD_2*	V_{CC} = 4.0 to 5.5 V	—	—	1	t_{cyc}	Figure 22.5
					—	—	1		
Receive data setup time (clocked synchronous)		t_{RXS}	RXD, RXD_2*	V_{CC} = 4.0 to 5.5 V	50.0	—	—	ns	
					100.0	—	—		
Receive data hold time (clocked synchronous)		t_{RXH}	RXD, RXD_2*	V_{CC} = 4.0 to 5.5 V	50.0	—	—	ns	
					100.0	—	—		

Note: * The H8/36037 Group does not have these pins.

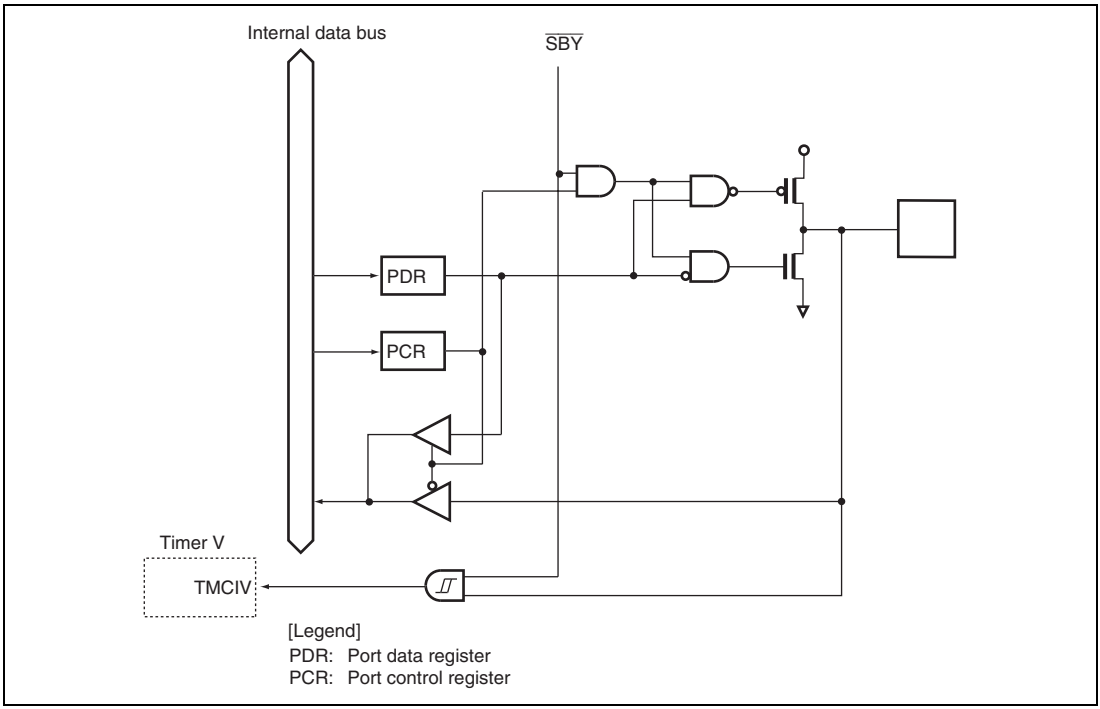

Figure B.14 Port 7 Block Diagram (P75)