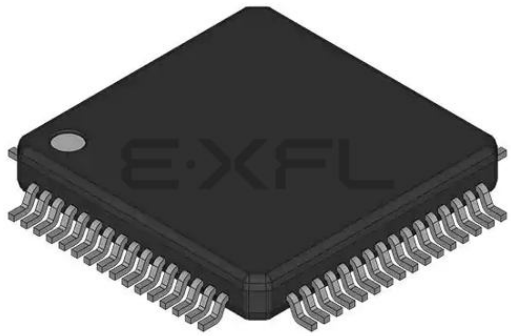

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2.4 Instruction Set

2.4.1 Table of Instructions Classified by Function

The H8/300H CPU has 62 instructions. Tables 2.2 to 2.9 summarize the instructions in each functional category. The notation used in tables 2.2 to 2.9 is defined below.

Table 2.1 Operation Notation

Symbol	Description
Rd	General register (destination)*
Rs	General register (source)*
Rn	General register*
ERn	General register (32-bit register or address register)
(EAd)	Destination operand
(EAs)	Source operand
CCR	Condition-code register
N	N (negative) flag in CCR
Z	Z (zero) flag in CCR
V	V (overflow) flag in CCR
C	C (carry) flag in CCR
PC	Program counter
SP	Stack pointer
#IMM	Immediate data
disp	Displacement
+	Addition
–	Subtraction
×	Multiplication
÷	Division
∧	Logical AND
∨	Logical OR
⊕	Logical XOR
→	Move
¬	NOT (logical complement)
:3/:8/:16/:24	3-, 8-, 16-, or 24-bit length

2.5 Addressing Modes and Effective Address Calculation

The following describes the H8/300H CPU. In this LSI, the upper eight bits are ignored in the generated 24-bit address, so the effective address is 16 bits.

2.5.1 Addressing Modes

The H8/300H CPU supports the eight addressing modes listed in table 2.10. Each instruction uses a subset of these addressing modes. Addressing modes that can be used differ depending on the instruction. For details, refer to appendix A.4, Combinations of Instructions and Addressing Modes.

Arithmetic and logic instructions can use the register direct and immediate modes. Data transfer instructions can use all addressing modes except program-counter relative and memory indirect. Bit-manipulation instructions use register direct, register indirect, or the absolute addressing mode (@aa:8) to specify an operand, and register direct (BSET, BCLR, BNOT, and BTST instructions) or immediate (3-bit) addressing mode to specify a bit number in the operand.

Table 2.10 Addressing Modes

No.	Addressing Mode	Symbol
1	Register direct	Rn
2	Register indirect	@ERn
3	Register indirect with displacement	@(d:16,ERn)/@(d:24,ERn)
4	Register indirect with post-increment Register indirect with pre-decrement	@ERn+ @–ERn
5	Absolute address	@aa:8/@aa:16/@aa:24
6	Immediate	#xx:8/#xx:16/#xx:32
7	Program-counter relative	@(d:8,PC)/@(d:16,PC)
8	Memory indirect	@@aa:8

(1) Register Direct—Rn

The register field of the instruction specifies an 8-, 16-, or 32-bit general register containing the operand. R0H to R7H and R0L to R7L can be specified as 8-bit registers. R0 to R7 and E0 to E7 can be specified as 16-bit registers. ER0 to ER7 can be specified as 32-bit registers.

Bit	Bit Name	Initial Value	R/W	Description
4	TOA1	0	R/W	Output Level Select A1 0: 0 output at the FTIOA1 pin* 1: 1 output at the FTIOA1 pin*
3	TOD0	0	R/W	Output Level Select D0 0: 0 output at the FTIOD0 pin* 1: 1 output at the FTIOD0 pin*
2	TOC0	0	R/W	Output Level Select C0 0: 0 output at the FTIOC0 pin* 1: 1 output at the FTIOC0 pin*
1	TOB0	0	R/W	Output Level Select B0 0: 0 output at the FTIOB0 pin* 1: 1 output at the FTIOB0 pin*
0	TOA0	0	R/W	Output Level Select A0 0: 0 output at the FTIOA0 pin* 1: 1 output at the FTIOA0 pin*

Note: * The change of the setting is immediately reflected in the output value.

12.3.7 Timer Counter (TCNT)

The timer Z has two TCNT counters (TCNT_0 and TCNT_1), one for each channel. The TCNT counters are 16-bit readable/writable registers that increment/decrement according to input clocks. Input clocks can be selected by bits TPSC2 to TPSC0 in TCR. TCNT0 and TCNT 1 increment/decrement in complementary PWM mode, while they only increment in other modes.

The TCNT counters are initialized to H'0000 by compare matches with corresponding GRA, GRB, GRC, or GRD, or input captures to GRA, GRB, GRC, or GRD (counter clearing function). When the TCNT counters overflow, an OVF flag in TSR for the corresponding channel is set to 1. When TCNT_1 underflows, an UDF flag in TSR is set to 1. The TCNT counters cannot be accessed in 8-bit units; they must always be accessed as a 16-bit unit. TCNT is initialized to H'0000.

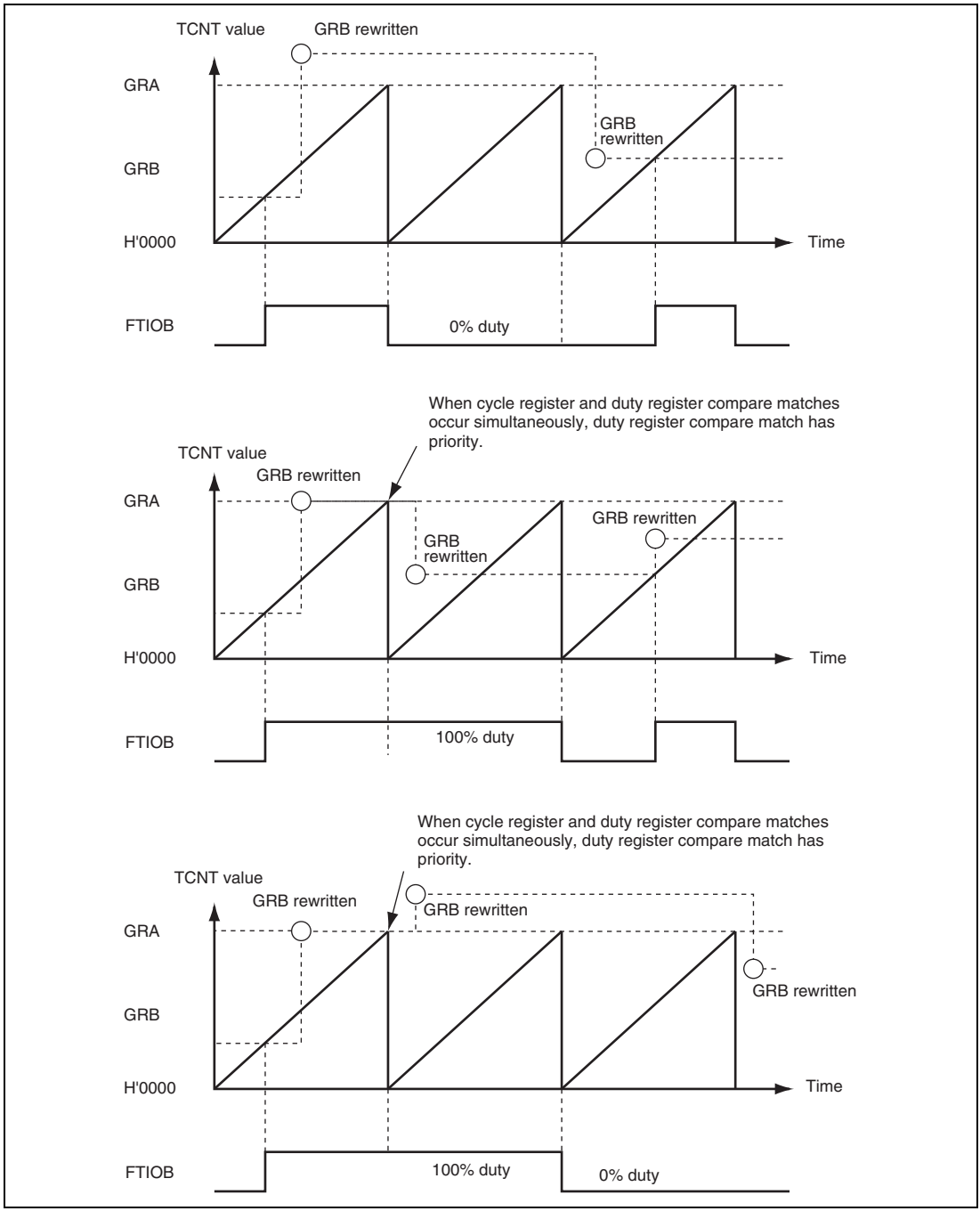


Figure 12.25 Example of PWM Mode Operation (4)

12.4.6 Reset Synchronous PWM Mode

Three normal- and counter-phase PWM waveforms are output by combining channels 0 and 1 that one of changing points of waveforms will be common.

In reset synchronous PWM mode, the FTIOB0 to FTIOD0 and FTIOA1 to FTIOD1 pins become PWM-output pins automatically. TCNT_0 performs an increment operation. Tables 12.4 and 12.5 show the PWM-output pins used and the register settings, respectively.

Figure 12.26 shows the example of reset synchronous PWM mode setting procedure.

Table 12.4 Output Pins in Reset Synchronous PWM Mode

Channel	Pin Name	I/O	Pin Function
0	FTIOC0	Output	Toggle output in synchronous with PWM cycle
0	FTIOB0	Output	PWM output 1
0	FTIOD0	Output	PWM output 1 (counter-phase waveform of PWM output 1)
1	FTIOA1	Output	PWM output 2
1	FTIOC1	Output	PWM output 2 (counter-phase waveform of PWM output 2)
1	FTIOB1	Output	PWM output 3
1	FTIOD1	Output	PWM output 3 (counter-phase waveform of PWM output 3)

Table 12.5 Register Settings in Reset Synchronous PWM Mode

Register	Description
TCNT_0	Initial setting of H'0000
TCNT_1	Not used (independently operates)
GRA_0	Sets counter cycle of TCNT_0
GRB_0	Set a changing point of the PWM waveform output from pins FTIOB0 and FTIOD0.
GRA_1	Set a changing point of the PWM waveform output from pins FTIOA1 and FTIOC1.
GRB_1	Set a changing point of the PWM waveform output from pins FTIOB1 and FTIOD1.

14.5.5 Simultaneous Serial Data Transmission and Reception

Figure 14.14 shows a sample flowchart for simultaneous serial transmit and receive operations. The following procedure should be used for simultaneous serial data transmit and receive operations. To switch from transmit mode to simultaneous transmit and receive mode, after checking that the SCI3 has finished transmission and the TDRE and TEND flags are set to 1, clear TE to 0. Then simultaneously set TE and RE to 1 with a single instruction. To switch from receive mode to simultaneous transmit and receive mode, after checking that the SCI3 has finished reception, clear RE to 0. Then after checking that the RDRF and receive error flags (OER, FER, and PER) are cleared to 0, simultaneously set TE and RE to 1 with a single instruction.

15.3.5 Bit Configuration Registers 0, 1 (BCR0, BCR1)

BCR configures the CAN bit timing parameters and baud rate prescaler for the CDLC.

- BCR0

Bit	Bit Name	Initial Value	R/W	Description
7	SJW1	0	R/W	Re-Synchronization Jump Width
6	SJW0	0	R/W	These bits set the maximum value of synchronization width. 00: 1 time quantum 01: 2 time quanta 10: 3 time quanta 11: 4 time quanta
5	BRP5	0	R/W	Baud Rate Prescaler
4	BRP4	0	R/W	These bits set the clock used for time quanta.
3	BRP3	0	R/W	000000: Setting prohibited
2	BRP2	0	R/W	000001: 2 system clocks
1	BRP1	0	R/W	: : (BRP + 1) system clocks
0	BRP0	0	R/W	111111: 64 system clocks

- BCR1

Bit	Bit Name	Initial Value	R/W	Description
7	—	0	—	Reserved This bit is always read as 0. The write value should always be 0.

15.4.2 Local Acceptance Filter Mask (LAFMHn1, LAFMHn0, LAFMLn1, LAFMLn0 [n = 0 to 3])

LAFM consists of four registers for one Mailbox. LAFM filters mask of bit-unit comparison between the message identifier of RXn (n = 0 to 3) stored in the receive Mailbox and the receive message identifier. Since LAFM is in RAM, initial values are undefined after power-on. Be sure to initialize each bit by writing 0 or 1.

Register Name	Bit	Bit Name	R/W	Description
LAFMLn1 (n = 0 to 3)	7 to 0	LAFMLn7 to LAFMLn0	R/W	Filter mask for bits 7 to 0 of the extended identifier. 0: Receive message is stored in RXn because the RXn message identifier bits match the receive message identifier bits 1: Receive message is stored in RXn regardless of whether the RXn message identifier bits match the receive message identifier bits
LAFMLn0 (n = 0 to 3)	7 to 0	LAFMLn15 to LAFMLn8	R/W	Filter mask for bits 15 to 8 of the extended identifier. 0: Receive message is stored in RXn because the RXn message identifier bits match the receive message identifier bits 1: Receive message is stored in RXn regardless of whether the RXn message identifier bits match the receive message identifier bits
LAFMHn1 (n = 0 to 3)	7 to 5	LAFMHn7 to LAFMHn5	R/W	Filter mask for bits 2 to 0 of the standard identifier. 0: Receive message is stored in RXn because the RXn message identifier bits match the receive message identifier bits 1: Receive message is stored in RXn regardless of whether the RXn message identifier bits match the receive message identifier bits

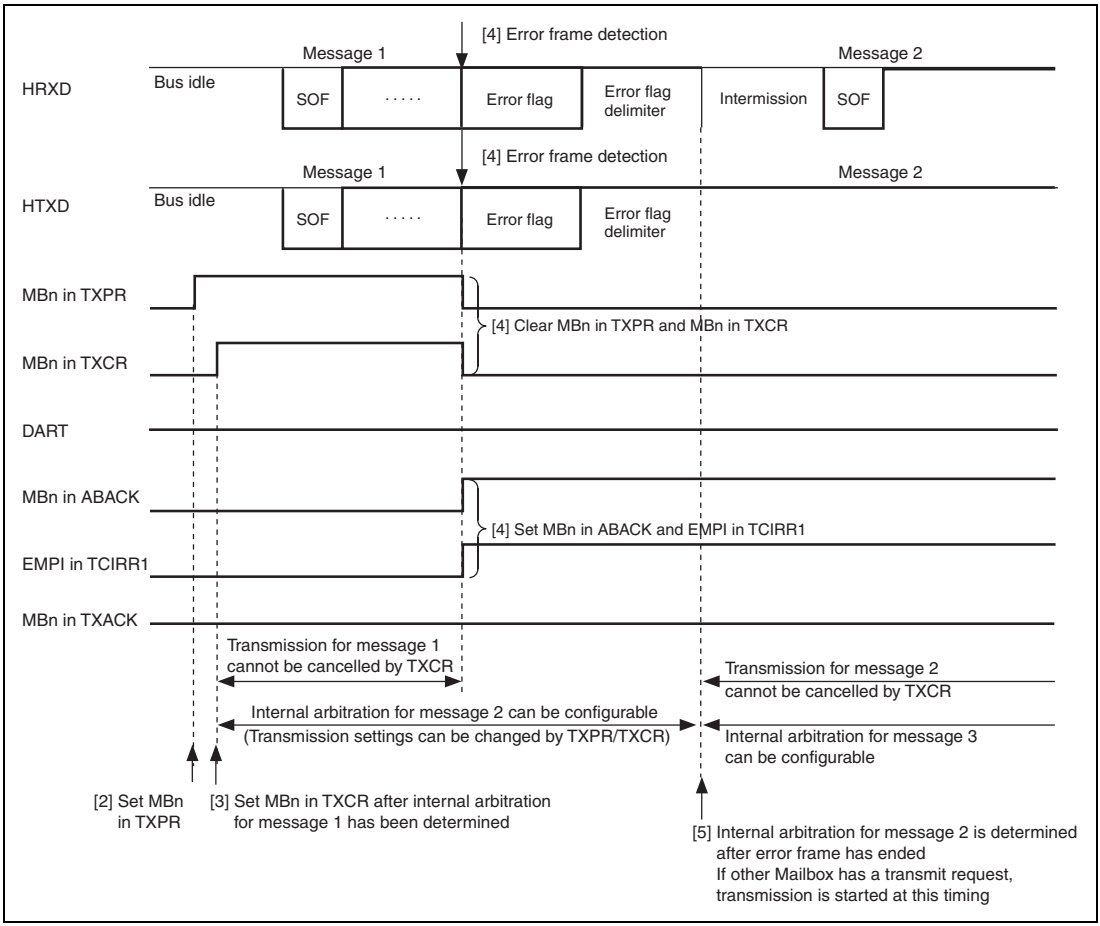


Figure 15.12 Internal Arbitration at Error Detection (MBn in TXCR = 1)

16.3.6 SS Receive Data Register (SSRDR)

SSRDR is an 8-bit register that stores received serial data. When the SSU has received one byte of serial data, it transfers the received serial data from SSTRSR and the data is stored. After this, SSTRSR is receive-enabled. As SSTRSR and SSRDR function as a double buffer in this way, continuous receive operations are possible. SSRDR is a read-only register and cannot be written to by the CPU. SSRDR is initialized to H'00.

16.3.7 SS Transmit Data Register (SSTDR)

SSTDR is an 8-bit register that stores serial data for transmission. SSTDR can be read or written to by the CPU at all times. When the SSU detects that SSTRSR is empty, it transfers the transmit data written in SSTDR to SSTRSR and starts serial transmission. If the next transmit data has already been written to SSTDR during serial transmission, continuous serial transmission is possible. SSTDR is initialized to H′00.

16.3.8 SS Shift Register (SSTRSR)

SSTRSR is a shift register that transmits and receives serial data. When transmit data is transferred from SSTDR to SSTRSR, bit 0 in SSTDR is transferred to bit 0 in SSTRSR while the MLS bit in SSMR is 0 (LSB-first transfer) and bit 7 in SSTDR is transferred to bit 0 in SSTRSR while the MLS bit in SSMR is 1 (MSB-first transfer). SSTRSR cannot be directly accessed by the CPU.

18.3.2 A/D Control/Status Register (ADCSR)

ADCSR consists of the control bits and conversion end status bits of the A/D converter.

Bit	Bit Name	Initial Value	R/W	Description
7	ADF	0	R/W	A/D End Flag [Setting conditions] • When A/D conversion ends in single mode • When A/D conversion ends once on all the channels selected in scan mode [Clearing condition] • When 0 is written after reading ADF = 1
6	ADIE	0	R/W	A/D Interrupt Enable A/D conversion end interrupt request (ADI) is enabled by ADF when this bit is set to 1
5	ADST	0	R/W	A/D Start Setting this bit to 1 starts A/D conversion. In single mode, this bit is cleared to 0 automatically when conversion on the specified channel is complete. In scan mode, conversion continues sequentially on the specified channels until this bit is cleared to 0 by software, a reset, or a transition to standby mode.
4	SCAN	0	R/W	Scan Mode Selects single mode or scan mode as the A/D conversion operating mode. 0: Single mode 1: Scan mode
3	CKS	0	R/W	Clock Select Selects the A/D conversions time. 0: Conversion time = 134 states (max.) 1: Conversion time = 70 states (max.) Clear the ADST bit to 0 before switching the conversion time.

20.2 When Not Using Internal Power Supply Step-Down Circuit

When the internal power supply step-down circuit is not used, connect the external power supply to the V_{CL} pin and V_{CC} pin, as shown in figure 20.2. The external power supply is then input directly to the internal power supply. The permissible range for the power supply voltage is 3.0 V to 3.6 V. Operation cannot be guaranteed if a voltage outside this range (less than 3.0 V or more than 3.6 V) is input.

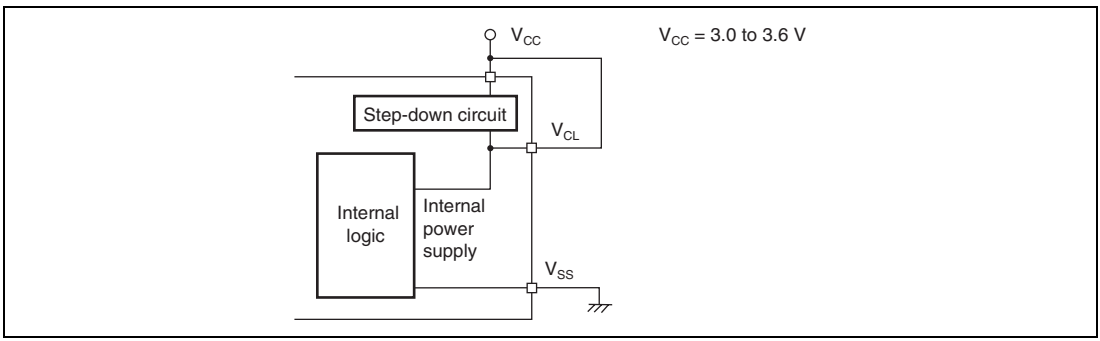


Figure 20.2 Power Supply Connection when Internal Step-Down Circuit is Not Used

22.3.3 AC Characteristics

Table 22.14 AC Characteristics

V_{CC} = 2.7 to 5.5 V, V_{SS} = 0.0 V, T_a = –20 to +75°C (regular specifications) or T_a = –40 to +85°C (wide-range specifications), unless otherwise indicated.

Item	Symbol	Applicable Pins	Test Condition	Values			Unit	Reference Figure
				Min.	Typ.	Max.		
System clock oscillation frequency	f_{OSC}	OSC1, OSC2	VCC = 4.0 to 5.5 V	2.0	—	20.0	MHz	*1
				2.0		10.0		
System clock (ϕ) cycle time	t_{cyc}			1	—	64	t_{OSC}	*2
				—	—	12.8	µs	
Subclock oscillator oscillation frequency	f_{RO}		V_{CC} = 4.0 to 5.5 V	64.0	—	850.0	kHz	
Subclock oscillator (ϕw) cycle time	t_{RO}		V_{CC} = 4.0 to 5.5 V	1.18	—	15.6	µs	
Subclock (ϕsub) cycle time	t_{subcyc}		V_{CC} = 4.0 to 5.5 V	2	—	8	ϕw	
Instruction cycle time				2	—	—	t_{cyc} t_{subcyc}	
Oscillation stabilization time (crystal resonator)	t_{rc}	OSC1, OSC2		—	—	10.0	ms	
Oscillation stabilization time (ceramic resonator)	t_{rc}	OSC1, OSC2		—	—	5.0	ms	
External clock high width	t_{CPH}	OSC1	V_{CC} = 4.0 to 5.5 V	20.0	—	—	ns	Figure 22.1
				40.0	—	—		
External clock low width	t_{CPL}	OSC1	V_{CC} = 4.0 to 5.5 V	20.0	—	—	ns	
				40.0	—	—		
External clock rise time	t_{CPr}	OSC1	V_{CC} = 4.0 to 5.5 V	—	—	10.0	ns	
				—	—	15.0		
External clock fall time	t_{CPf}	OSC1	V_{CC} = 4.0 to 5.5 V	—	—	10.0	ns	
				—	—	15.0		

22.3.6 Power-Supply-Voltage Detection Circuit Characteristics (Optional)

Table 22.20 Power-Supply-Voltage Detection Circuit Characteristics

V_{SS} = 0.0 V, T_a = –20 to +75°C (regular specifications) or T_a = –40 to +85°C (wide-range specifications), unless otherwise indicated.

Item	Symbol	Test Condition	Values			Unit
			Min.	Typ.	Max.	
Power-supply falling detection voltage	Vint (D)	LVDSEL = 0	3.3	3.7	—	V
Power-supply rising detection voltage	Vint (U)	LVDSEL = 0	—	4.0	4.5	V
Reset detection voltage 1*[1]	Vreset1	LVDSEL = 0	—	2.3	2.7	V
Reset detection voltage 2*[2]	Vreset2	LVDSEL = 1	3.0	3.6	4.2	V
Lower-limit voltage of LVDR operation*[3]	$V_{LVDRmin}$		1.0	—	—	V
LVD stabilization time	t_{LVDON}		50	—	—	µs
Supply current in standby mode	I_{STBY}	LVDE = 1, Vcc = 5.0 V, subtimer and WDT not used	—	—	350	µA

Notes: 1. This voltage should be used when the falling and rising voltage detection function is used.
2. Select the low-voltage reset 2 when only the low-voltage detection reset is used.
3. When the power-supply voltage (Vcc) falls below $V_{LVDRmin}$ = 1.0 V and then rises, a reset may not occur. Therefore sufficient evaluation is required.

22.3.7 Power-On Reset Circuit Characteristics (Optional)

Table 22.21 Power-On Reset Circuit Characteristics

V_{SS} = 0.0 V, T_a = –20 to +75°C (regular specifications) or T_a = –40 to +85°C (wide-range specifications), unless otherwise indicated.

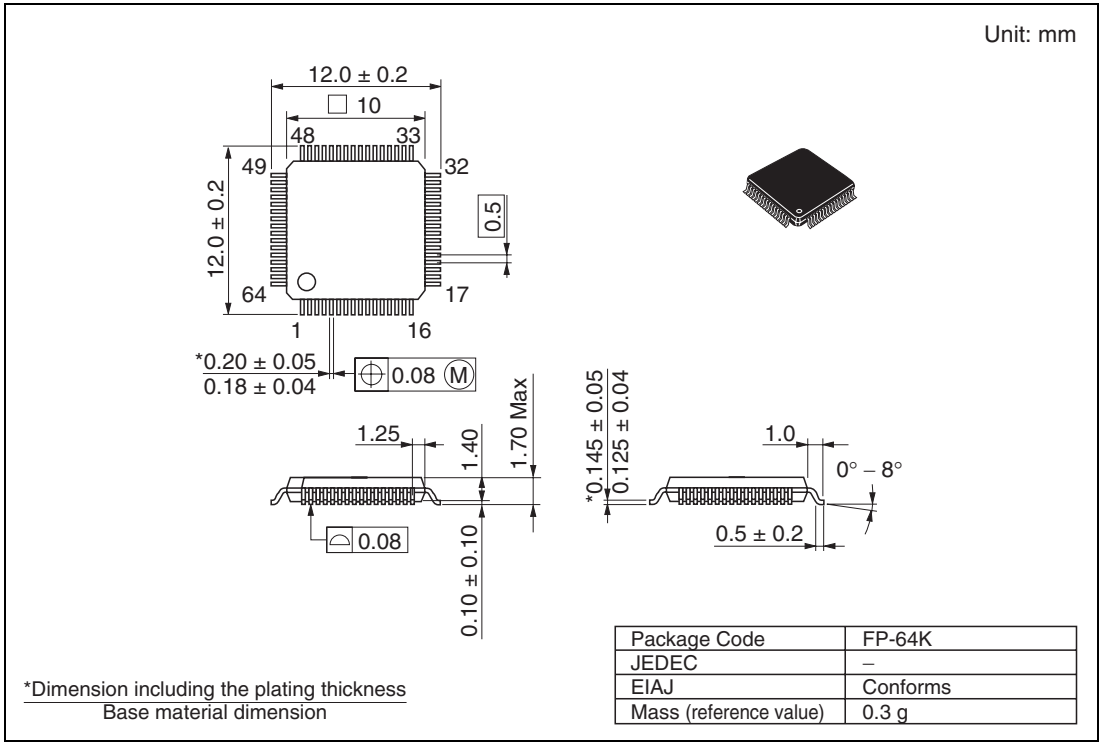
Item	Symbol	Test Condition	Values			Unit
			Min.	Typ.	Max.	
Pull-up resistance of $\overline{RES}$ pin	R_{RES}		100	150	—	kΩ
Power-on reset start voltage*	V_{por}		—	—	100	mV

Note: * The power-supply voltage (Vcc) must fall below Vpor = 100 mV and then rise after charge of the $\overline{RES}$ pin is removed completely. In order to remove charge of the $\overline{RES}$ pin, it is recommended that the diode be placed in the Vcc side. If the power-supply voltage (Vcc) rises from the point over 100 mV, a power-on reset may not occur.

Instruction	Mnemonic	Instruction Fetch I	Branch Addr. Read J	Stack Operation K	Byte Data Access L	Word Data Access M	Internal Operation N
Bcc	BLT d:8	2					
	BGT d:8	2					
	BLE d:8	2					
	BRA d:16(BT d:16)	2					2
	BRN d:16(BF d:16)	2					2
	BHI d:16	2					2
	BLS d:16	2					2
	BCC d:16(BHS d:16)	2					2
	BCS d:16(BLO d:16)	2					2
	BNE d:16	2					2
	BEQ d:16	2					2
	BVC d:16	2					2
	BVS d:16	2					2
	BPL d:16	2					2
	BMI d:16	2					2
	BGE d:16	2					2
	BLT d:16	2					2
	BGT d:16	2					2
	BLE d:16	2					2
BCLR	BCLR #xx:3, Rd	1					
	BCLR #xx:3, @ERd	2			2		
	BCLR #xx:3, @aa:8	2			2		
	BCLR Rn, Rd	1					
	BCLR Rn, @ERd	2			2		
	BCLR Rn, @aa:8	2			2		
BIAND	BIAND #xx:3, Rd	1					
	BIAND #xx:3, @ERd	2			1		
	BIAND #xx:3, @aa:8	2			1		
BILD	BILD #xx:3, Rd	1					
	BILD #xx:3, @ERd	2			1		
	BILD #xx:3, @aa:8	2			1		

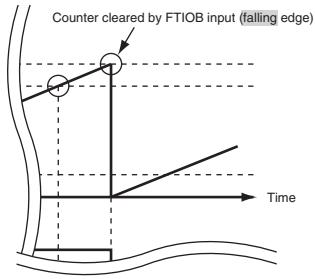
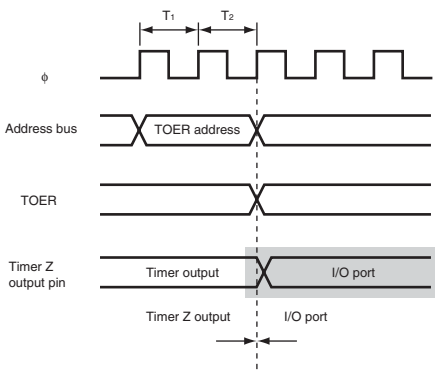
Appendix D Package Dimensions

The package dimensions that are shown in the Renesas Semiconductor Packages Data Book have priority.



Package Code	FP-64K
JEDEC	–
EIAJ	Conforms
Mass (reference value)	0.3 g

Figure D.1 FP-64K Package Dimensions

Item	Page	Revision (See Manual for Details)
12.3.7 Timer Counter (TCNT)	177	Added ….The TCNT counters cannot be accessed in 8-bit units; they must always be accessed as a 16-bit unit. TCNT is initialized to H'0000.
Figure 12.17 Example of Input Capture Operation	196	Amended 
12.4.4 Synchronous Operation	199	Added Figure 12.20 shows an example of synchronous operation. In this example, …. set for the channel 1 counter clearing source. In addition, the same input clock has been set as the counter input clock for channel 0 and channel 1. Two-phase PWM waveforms are….
Figure 12.44 Example of Output Disable Timing of Timer Z by Writing to TOER	229	Amended 

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