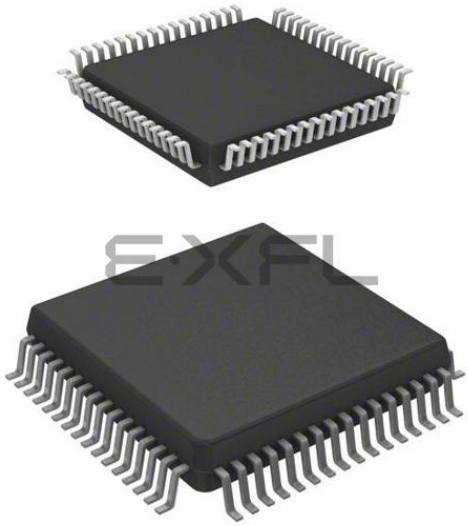


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300H
Core Size	16-Bit
Speed	20MHz
Connectivity	CANbus, SCI, SSU
Peripherals	LVD, POR, PWM, WDT
Number of I/O	45
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	64-BQFP
Supplier Device Package	64-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df36054ghv

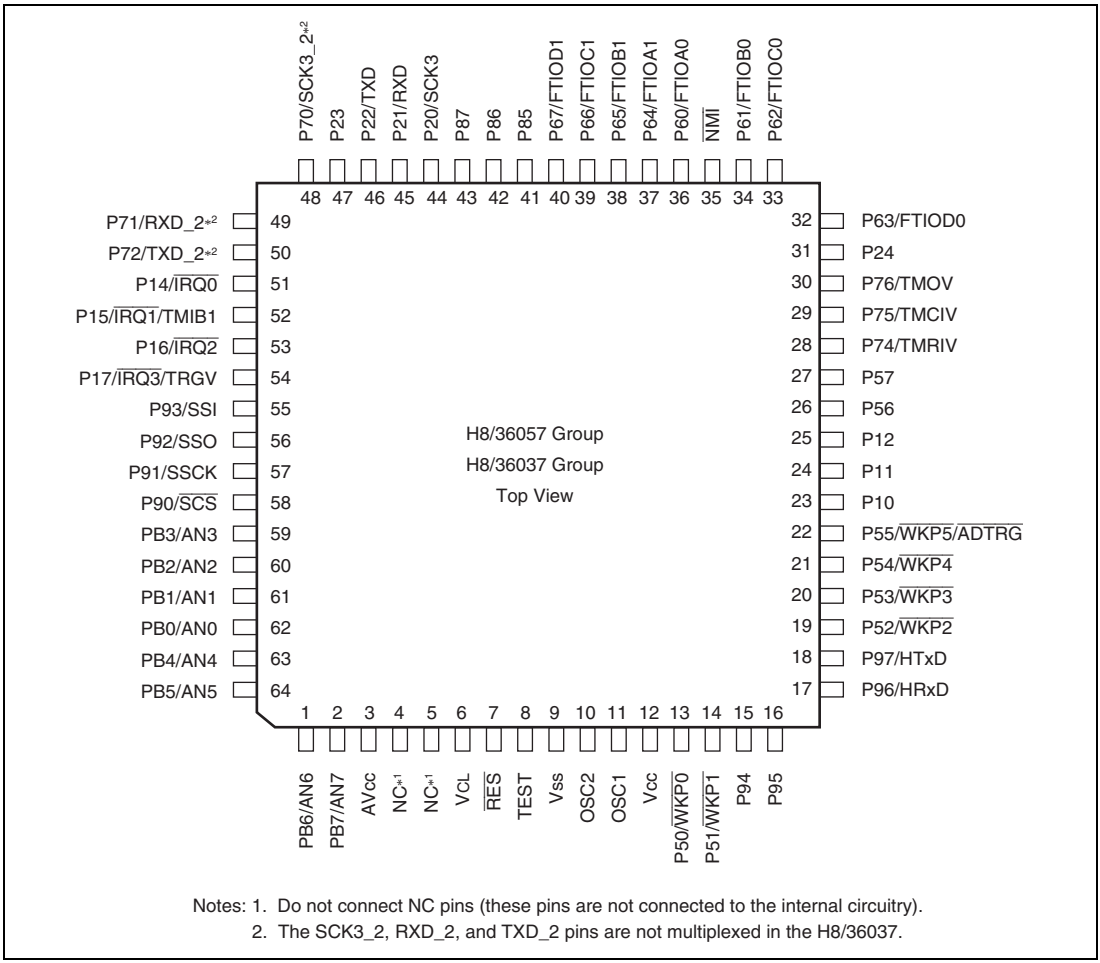
Appendix A Instruction Set

Section 1 Overview

1.1 Features

- High-speed H8/300H central processing unit with an internal 16-bit architecture
  - Upward-compatible with H8/300 CPU on an object level
  - Sixteen 16-bit general registers
  - 62 basic instructions
- Various peripheral functions
  - Timer B1 (8-bit timer)
  - Timer V (8-bit timer)
  - Timer Z (16-bit timer)
  - Watchdog timer
  - SCI3 (asynchronous or clocked synchronous serial communication interface)
  - TinyCAN (controller area network for Tiny)
  - SSU (synchronous serial communication unit)
  - Subsystem timer (subtimer)
  - 10-bit A/D converter

1.3 Pin Arrangement



Notes: 1. Do not connect NC pins (these pins are not connected to the internal circuitry).
2. The SCK3_2, RXD_2, and TXD_2 pins are not multiplexed in the H8/36037.

Figure 1.2 Pin Arrangement of F-ZTAT™ and Masked ROM Versions (FP-64K, FP-64A)

- BCLR instruction executed

```
BCLR    #0,     @PCR5
```

The BCLR instruction is executed for PCR5.

- After executing BCLR instruction

	P57	**P56**	**P55**	**P54**	**P53**	**P52**	**P51**	**P50**
Input/output	Output	Output	Output	Output	Output	Output	Output	Input
Pin state	Low level	High level	Low level	Low level	Low level	Low level	Low level	High level
PCR5	1	1	1	1	1	1	1	0
PDR5	1	0	0	0	0	0	0	0

- Description on operation

1. When the BCLR instruction is executed, first the CPU reads PCR5. Since PCR5 is a write-only register, the CPU reads a value of H'FF, even though the PCR5 value is actually H'3F.
2. Next, the CPU clears bit 0 in the read data to 0, changing the data to H'FE.
3. Finally, H'FE is written to PCR5 and BCLR instruction execution ends.

As a result of this operation, bit 0 in PCR5 becomes 0, making P50 an input port. However, bits 7 and 6 in PCR5 change to 1, so that P57 and P56 change from input pins to output pins. To prevent this problem, store a copy of the PDR5 data in a work area in memory and manipulate data of the bit in the work area, then write this data to PDR5.

- Prior to executing BCLR instruction

```
MOV.B   #3F,  R0L
MOV.B   R0L,  @RAM0
MOV.B   R0L,  @PCR5
```

The PCR5 value (H'3F) is written to a work area in memory (RAM0) as well as to PCR5.

	P57	**P56**	**P55**	**P54**	**P53**	**P52**	**P51**	**P50**
Input/output	Input	Input	Output	Output	Output	Output	Output	Output
Pin state	Low level	High level	Low level	Low level	Low level	Low level	Low level	Low level
PCR5	0	0	1	1	1	1	1	1
PDR5	1	0	0	0	0	0	0	0
RAM0	0	0	1	1	1	1	1	1

Section 6 Power-Down Modes

This LSI has six modes of operation after a reset. These include a normal active mode and four power-down modes, in which power consumption is significantly reduced. Module standby mode reduces power consumption by selectively halting on-chip module functions.

- Active mode

  The CPU and all on-chip peripheral modules are operable on the system clock. The system clock frequency can be selected from ϕosc, ϕosc/8, ϕosc/16, ϕosc/32, and ϕosc/64.
- Subactive mode

  The CPU and all on-chip peripheral modules are operable on the subclock. The subclock frequency can be selected from ϕw/2, ϕw/4, and ϕw/8.
- Sleep mode

  The CPU halts. On-chip peripheral modules are operable on the system clock.
- Subsleep mode

  The CPU halts. On-chip peripheral modules are operable on the subclock.
- Standby mode

  The CPU and all on-chip peripheral modules halt.
- Module standby mode

  Independent of the above modes, power consumption can be reduced by halting on-chip peripheral modules that are not used in module units.

Table 7.3 System Clock Frequencies for which Automatic Adjustment of LSI Bit Rate is Possible

Host Bit Rate	System Clock Frequency Range of LSI
19,200 bps	16 to 20 MHz
9,600 bps	8 to 16 MHz
4,800 bps	4 to 16 MHz
2,400 bps	2 to 16 MHz

7.3.2 Programming/Erasing in User Program Mode

On-board programming/erasing of an individual flash memory block can also be performed in user program mode by branching to a user program/erase control program. The user must set branching conditions and provide on-board means of supplying programming data. The flash memory must contain the user program/erase control program or a program that provides the user program/erase control program from external memory. As the flash memory itself cannot be read during programming/erasing, transfer the user program/erase control program to on-chip RAM, as in boot mode. Figure 7.2 shows a sample procedure for programming/erasing in user program mode. Prepare a user program/erase control program in accordance with the description in section 7.4, Flash Memory Programming/Erasing.

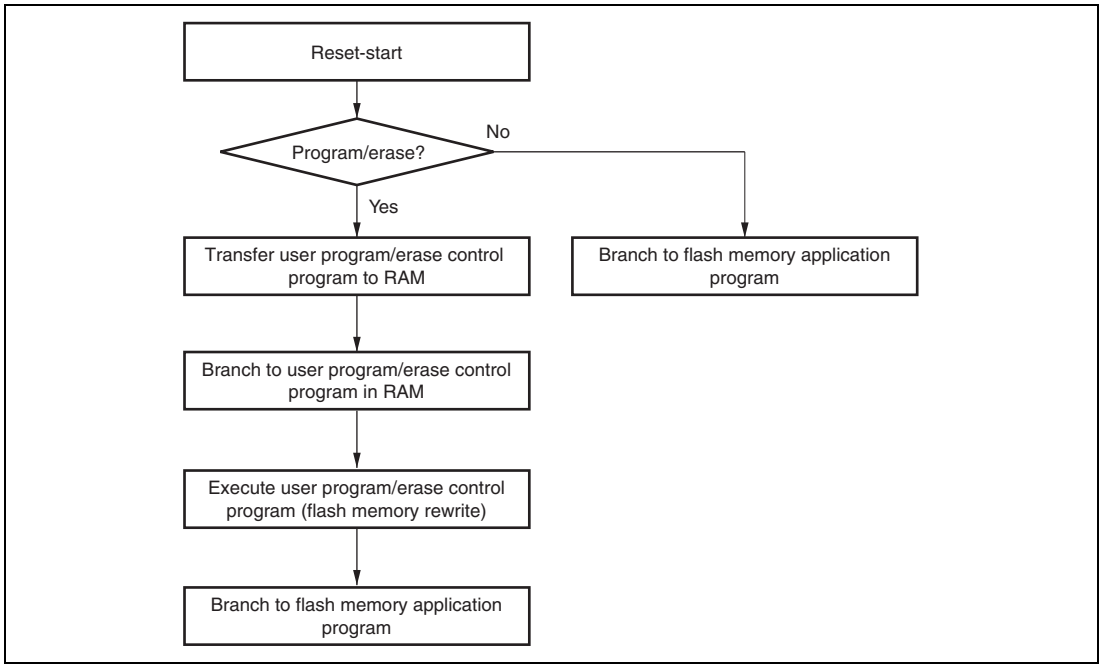


Figure 7.2 Programming/Erasing Flowchart Example in User Program Mode

7.5 Program/Erase Protection

There are three kinds of flash memory program/erase protection; hardware protection, software protection, and error protection.

7.5.1 Hardware Protection

Hardware protection refers to a state in which programming/erasing of flash memory is forcibly disabled or aborted because of a transition to reset, subactive mode, subsleep mode, or standby mode. Flash memory control register 1 (FLMCR1), flash memory control register 2 (FLMCR2), and erase block register 1 (EBR1) are initialized. In a reset via the $\overline{\text{RES}}$ pin, the reset state is not entered unless the $\overline{\text{RES}}$ pin is held low until oscillation stabilizes after powering on. In the case of a reset during operation, hold the $\overline{\text{RES}}$ pin low for the $\overline{\text{RES}}$ pulse width specified in the AC Characteristics section.

7.5.2 Software Protection

Software protection can be implemented against programming/erasing of all flash memory blocks by clearing the SWE bit in FLMCR1. When software protection is in effect, setting the P or E bit in FLMCR1 does not cause a transition to program mode or erase mode. By setting the erase block register 1 (EBR1), erase protection can be set for individual blocks. When EBR1 is set to H'00, erase protection is set for all blocks.

7.5.3 Error Protection

In error protection, an error is detected when CPU runaway occurs during flash memory programming/erasing, or operation is not performed in accordance with the program/erase algorithm, and the program/erase operation is forcibly aborted. Aborting the program/erase operation prevents damage to the flash memory due to overprogramming or overerasing.

When the following errors are detected during programming/erasing of flash memory, the FLER bit in FLMCR2 is set to 1, and the error protection state is entered.

- When the flash memory of the relevant address area is read during programming/erasing (including vector read and instruction fetch)
- Immediately after exception handling excluding a reset during programming/erasing
- When a SLEEP instruction is executed during programming/erasing

Section 11 Timer V

The timer V is an 8-bit timer based on an 8-bit counter. The timer V counts external events. Compare-match signals with two registers can also be used to reset the counter, request an interrupt, or output a pulse signal with an arbitrary duty cycle. Counting can be initiated by a trigger input at the TRGV pin, enabling pulse output control to be synchronized to the trigger, with an arbitrary delay from the trigger input. Figure 11.1 shows a block diagram of the timer V.

11.1 Features

- Choice of seven clock signals is available.
  Choice of six internal clock sources (ϕ/128, ϕ/64, ϕ/32, ϕ/16, ϕ/8, ϕ/4) or an external clock.
- Counter can be cleared by compare match A or B, or by an external reset signal. If the count stop function is selected, the counter can be halted when cleared.
- Timer output is controlled by two independent compare match signals, enabling pulse output with an arbitrary duty cycle, PWM output, and other applications.
- Three interrupt sources: compare match A, compare match B, timer overflow
- Counting can be initiated by trigger input at the TRGV pin. The rising edge, falling edge, or both edges of the TRGV input can be selected.

Bit	Bit Name	Initial Value	R/W	Description
1	CMD1	0	R/W	Combination Mode 1 and 0
0	CMD0	0	R/W	00: Channel 0 and channel 1 operate normally 01: Channel 0 and channel 1 are used together to operate in reset synchronous PWM mode 10: Channel 0 and channel 1 are used together to operate in complementary PWM mode (transferred at the trough) 11: Channel 0 and channel 1 are used together to operate in complementary PWM mode (transferred at the crest) Note: When reset synchronous PWM mode or complementary PWM mode is selected by these bits, this setting has the priority to the settings for PWM mode by each bit in TPMR. Stop TCNT_0 and TCNT_1 before making settings for reset synchronous PWM mode or complementary PWM mode.

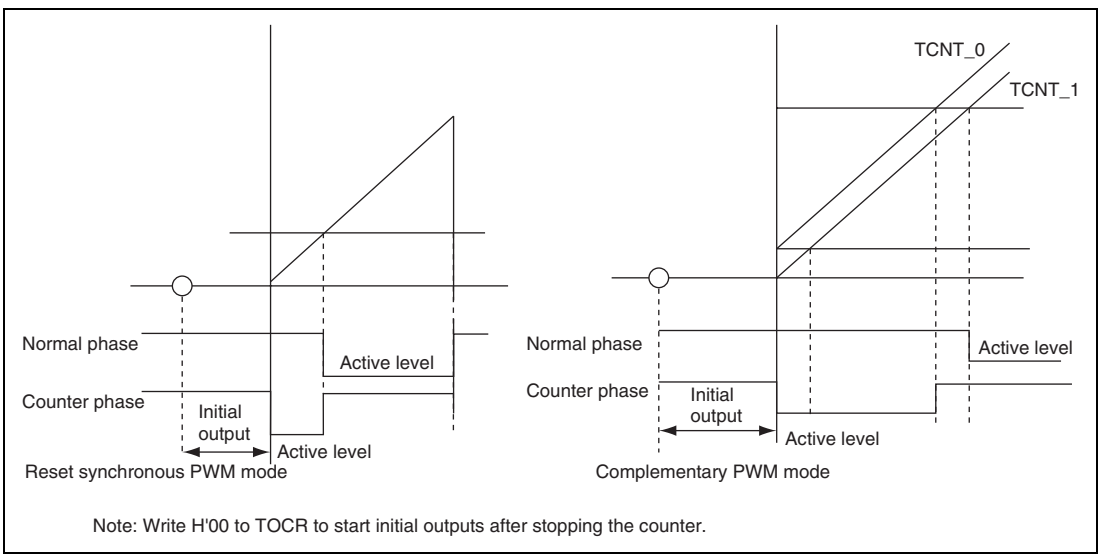


Figure 12.4 Example of Outputs in Reset Synchronous PWM Mode and Complementary PWM Mode

12.4 Operation

12.4.1 Counter Operation

When one of bits STR0 and STR1 in TSTR is set to 1, the TCNT counter for the corresponding channel begins counting. TCNT can operate as a free-running counter, periodic counter, for example. Figure 12.7 shows an example of the counter operation setting procedure.

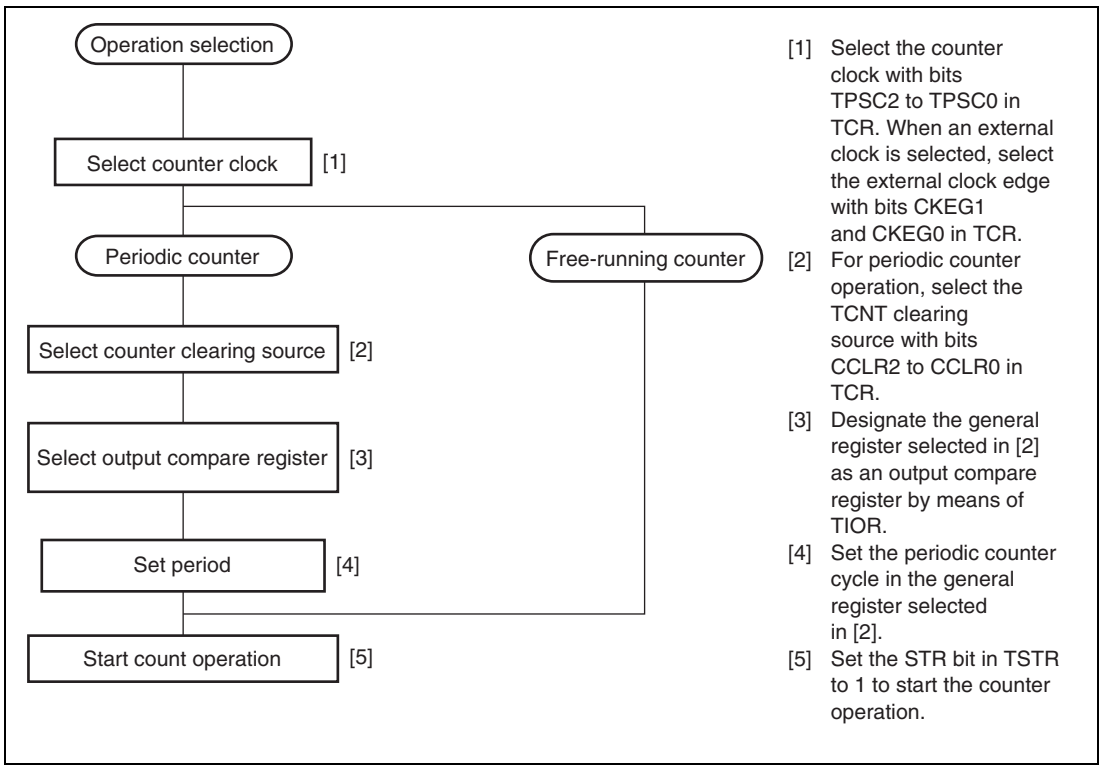


Figure 12.7 Example of Counter Operation Setting Procedure

14.8 Usage Notes

14.8.1 Break Detection and Processing

When framing error detection is performed, a break can be detected by reading the RXD pin value directly. In a break, the input from the RXD pin becomes all 0s, setting the FER flag, and possibly the PER flag. Note that as the SCI3 continues the receive operation after receiving a break, even if the FER flag is cleared to 0, it will be set to 1 again.

14.8.2 Mark State and Break Sending

When TE is 0, the TXD pin is used as an I/O port whose direction (input or output) and level are determined by PCR and PDR. This can be used to set the TXD pin to mark state (high level) or send a break during serial data transmission. To maintain the communication line at mark state until TE is set to 1, set both PCR and PDR to 1. As TE is cleared to 0 at this point, the TXD pin becomes an I/O port, and 1 is output from the TXD pin. To send a break during serial transmission, first set PCR to 1 and clear PDR to 0, and then clear TE to 0. When TE is cleared to 0, the transmitter is initialized regardless of the current transmission state, the TXD pin becomes an I/O port, and 0 is output from the TXD pin.

14.8.3 Receive Error Flags and Transmit Operations (Clocked Synchronous Mode Only)

Transmission cannot be started when a receive error flag (OER, PER, or FER) is set to 1, even if the TDRE flag is cleared to 0. Be sure to clear the receive error flags to 0 before starting transmission. Note also that receive error flags cannot be cleared to 0 even if the RE bit is cleared to 0.

15.5.2 Bit Timing

The bit rate and bit timing are set by the bit configuration register (BCR). The CAN controllers connected to the CAN bus should be set so that all of them have the same baud rate and same bit width. One bit time consists of total settable Time Quantum (TQ).

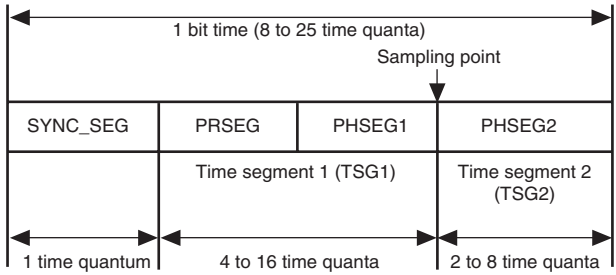


Figure 15.5 CAN Bit Configuration

The SYNC_SEG is a segment for establishing the synchronization of nodes on the CAN bus. Normal bit edge changes in this segment. The PRSEG is a segment for adjusting the physical delay between networks. The PHSEG1 is a buffer segment for adjusting positive phase drift. This segment is extended when re-synchronization is established. The PHSEG2 is a buffer segment for adjusting negative phase drift. This segment is shortened when re-synchronization is established.

The range of settable values in BCR (TSG1, TSG2, BRP, and SJW) is shown in table 15.2.

Table 15.2 Settable Values in BCR

Name	Abbreviation	Min. Value	Max. Value
Time segment 1	TSG1*[1]	3*[3]	15
Time segment 2	TSG2*[1]	1*[4]	7
Baud rate prescaler	BRP	1	63
Re-Synchronization Jump width	SJW*[2]	0	3

Notes: 1. The time quanta values for the TSEG1 and TSEG2 are as follows: TSG value + 1
2. In the CAN specifications, the Re-Synchronization Jump Width is stipulated as $4 \geq SJW \geq 1$. The value of SJW is given by adding 1 to the setting value of the bits SJW0 to SJW1 in BCR.
3. The minimum value of TSG1 is stipulated in the CAN specifications: TSG1 > TSG2
4. The minimum value of TSG2 is stipulated in the CAN specifications: $TSG2 \geq SJW$

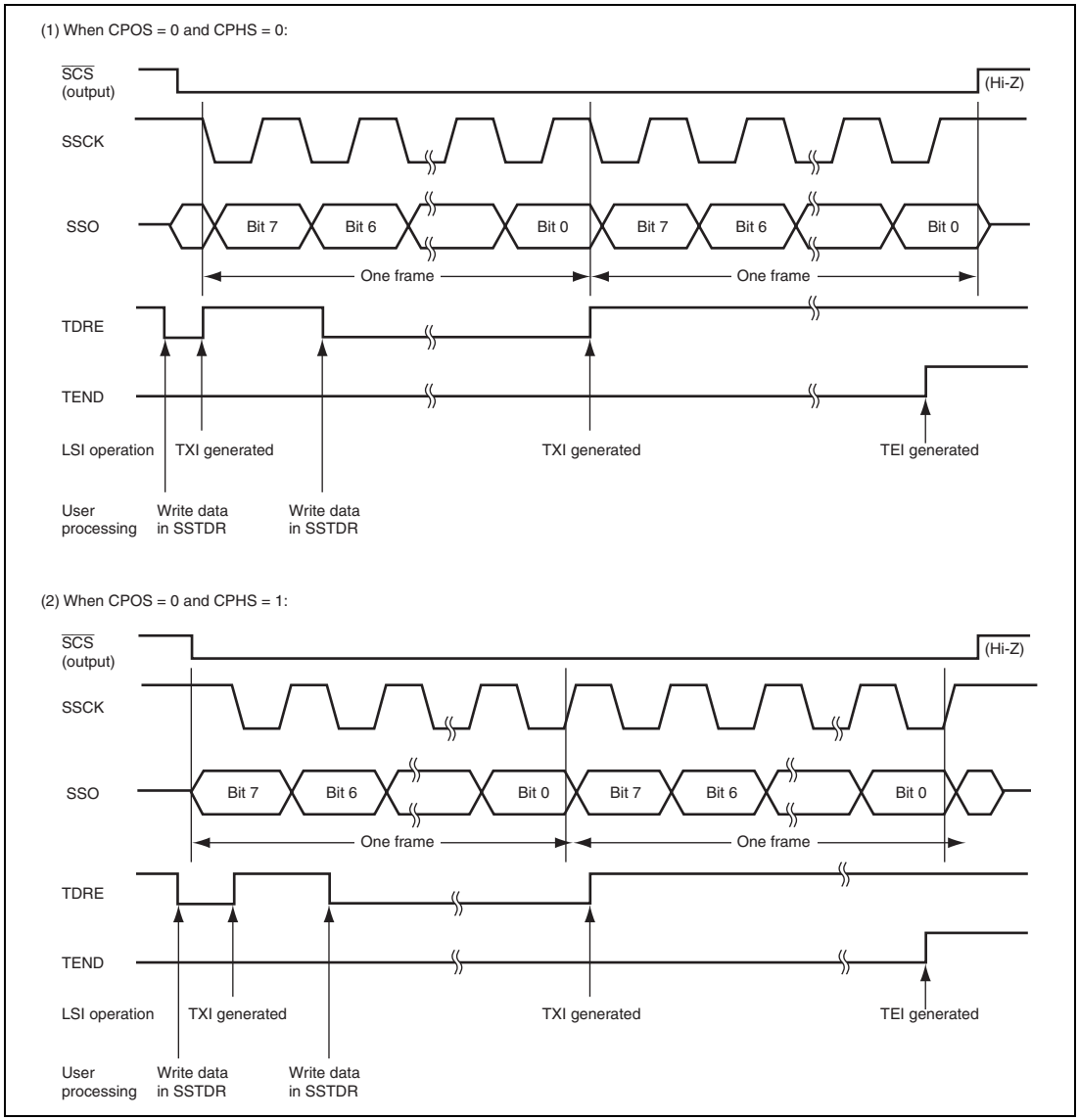


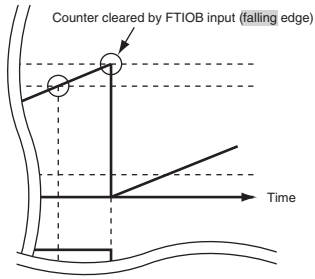
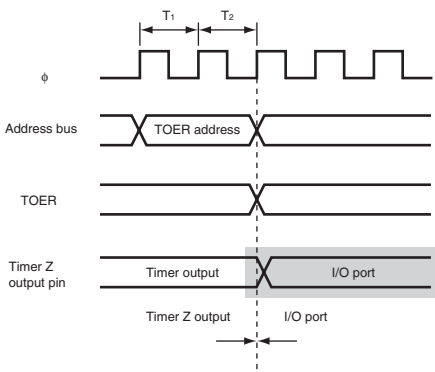
Figure 16.11 Example of Operation in Data Transmission (MSS = 1)

18.3.2 A/D Control/Status Register (ADCSR)

ADCSR consists of the control bits and conversion end status bits of the A/D converter.

Bit	Bit Name	Initial Value	R/W	Description
7	ADF	0	R/W	A/D End Flag [Setting conditions] • When A/D conversion ends in single mode • When A/D conversion ends once on all the channels selected in scan mode [Clearing condition] • When 0 is written after reading ADF = 1
6	ADIE	0	R/W	A/D Interrupt Enable A/D conversion end interrupt request (ADI) is enabled by ADF when this bit is set to 1
5	ADST	0	R/W	A/D Start Setting this bit to 1 starts A/D conversion. In single mode, this bit is cleared to 0 automatically when conversion on the specified channel is complete. In scan mode, conversion continues sequentially on the specified channels until this bit is cleared to 0 by software, a reset, or a transition to standby mode.
4	SCAN	0	R/W	Scan Mode Selects single mode or scan mode as the A/D conversion operating mode. 0: Single mode 1: Scan mode
3	CKS	0	R/W	Clock Select Selects the A/D conversions time. 0: Conversion time = 134 states (max.) 1: Conversion time = 70 states (max.) Clear the ADST bit to 0 before switching the conversion time.

Register Abbreviation	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name
SSCRH	MSS	BIDE	SOOS	SOL	SOLP	SCKS	CSS1	CSS0	SSU
SSCRL	MSTSSU	SSUMS	SRES	SCKOS	CSOS	—	—	—	
SSMR	MLS	CPOS	CPHS	—	—	CKS2	CKS1	CKS0	
SSER	TE	RE	RSSTP	—	TEIE	TIE	RIE	CEIE	
SSSR	—	ORER	—	—	TEND	TDRE	RDRF	CE	
SSRDR	SSRDR7	SSRDR6	SSRDR5	SSRDR4	SSRDR3	SSRDR2	SSRDR1	SSRDR0	
SSTDR	SSTDR7	SSTDR6	SSTDR5	SSTDR4	SSTDR3	SSTDR2	SSTDR1	SSTDR0	
SBTCTL	PCEF	—	—	START	OSCEB	SYSCKS	SBTIB	SBTUF	Subtimer
SBTDCNT	SBTDCNT7	SBTDCNT6	SBTDCNT5	SBTDCNT4	SBTDCNT3	SBTDCNT2	SBTDCNT1	SBTDCNT0	
ROPCR	ROPCR7	ROPCR6	ROPCR5	ROPCR4	ROPCR3	ROPCR2	ROPCR1	ROPCR0	
TCR_0	CCLR2	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0	Timer Z
TIORA_0	—	IOB2	IOB1	IOB0	—	IOA2	IOA1	IOA0	
TIORC_0	—	IOD2	IOD1	IOD0	—	IOC2	IOC1	IOC0	
TSR_0	—	—	—	OVF	IMFD	IMFC	IMFB	IMFA	
TIER_0	—	—	—	OVIE	IMIED	IMIEC	IMIEB	IMIEA	
POCR_0	—	—	—	—	—	POLD	POLC	POLB	
TCNT_0	TCNT0H7	TCNT0H6	TCNT0H5	TCNT0H4	TCNT0H3	TCNT0H2	TCNT0H1	TCNT0H0	
	TCNT0L7	TCNT0L6	TCNT0L5	TCNT0L4	TCNT0L3	TCNT0L2	TCNT0L1	TCNT0L0	
GRA_0	GRA0H7	GRA0H6	GRA0H5	GRA0H4	GRA0H3	GRA0H2	GRA0H1	GRA0H0	
	GRA0L7	GRA0L6	GRA0L5	GRA0L4	GRA0L3	GRA0L2	GRA0L1	GRA0L0	
GRB_0	GRB0H7	GRB0H6	GRB0H5	GRB0H4	GRB0H3	GRB0H2	GRB0H1	GRB0H0	
	GRB0L7	GRB0L6	GRB0L5	GRB0L4	GRB0L3	GRB0L2	GRB0L1	GRB0L0	
GRC_0	GRC0H7	GRC0H6	GRC0H5	GRC0H4	GRC0H3	GRC0H2	GRC0H1	GRC0H0	
	GRC0L7	GRC0L6	GRC0L5	GRC0L4	GRC0L3	GRC0L2	GRC0L1	GRC0L0	
GRD_0	GRD0H7	GRD0H6	GRD0H5	GRD0H4	GRD0H3	GRD0H2	GRD0H1	GRD0H0	
	GRD0L7	GRD0L6	GRD0L5	GRD0L4	GRD0L3	GRD0L2	GRD0L1	GRD0L0	
TCR_1	CCLR2	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0	
TIORA_1	—	IOB2	IOB1	IOB0	—	IOA2	IOA1	IOA0	
TIORC_1	—	IOD2	IOD1	IOD0	—	IOC2	IOC1	IOC0	
TSR_1	—	—	UDF	OVF	IMFD	IMFC	IMFB	IMFA	
TIER_1	—	—	—	OVIE	IMIED	IMIEC	IMIEB	IMIEA	
POCR_1	—	—	—	—	—	POLD	POLC	POLB	

Item	Page	Revision (See Manual for Details)
12.3.7 Timer Counter (TCNT)	177	Added ….The TCNT counters cannot be accessed in 8-bit units; they must always be accessed as a 16-bit unit. TCNT is initialized to H'0000.
Figure 12.17 Example of Input Capture Operation	196	Amended 
12.4.4 Synchronous Operation	199	Added Figure 12.20 shows an example of synchronous operation. In this example, …. set for the channel 1 counter clearing source. In addition, the same input clock has been set as the counter input clock for channel 0 and channel 1. Two-phase PWM waveforms are….
Figure 12.44 Example of Output Disable Timing of Timer Z by Writing to TOER	229	Amended 

Index