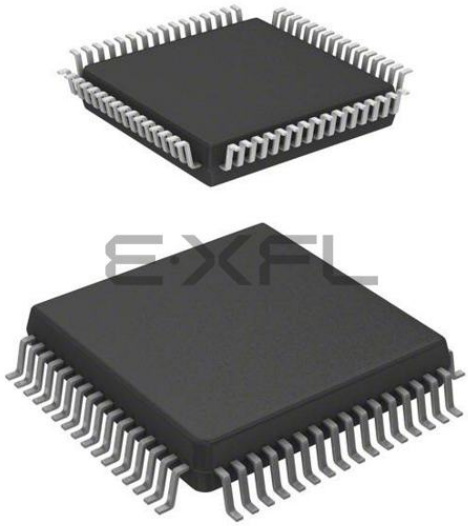

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300H
Core Size	16-Bit
Speed	20MHz
Connectivity	CANbus, SCI, SSU
Peripherals	PWM, WDT
Number of I/O	45
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	64-BQFP
Supplier Device Package	64-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df36054hv

User's Manual

16

The revision list can be viewed directly by clicking the title page.

The revision list summarizes the locations of revisions and additions. Details should always be checked by referring to the relevant text.

16 H8/36057Group, H8/36037Group

Hardware Manual

Renesas 16-Bit Single-Chip Microcomputer H8 Family/H8/300H Tiny Series

H8/36057	HD64F36057, HD64F36057G
	HD64336057, HD64336057G
H8/36054	HD64F36054, HD64F36054G
	HD64336054, HD64336054G
H8/36037	HD64F36037, HD64F36037G
	HD64336037, HD64336037G
H8/36036	HD64336036, HD64336036G
H8/36035	HD64336035, HD64336035G
H8/36034	HD64F36034, HD64F36034G
	HD64336034, HD64336034G
H8/36033	HD64336033, HD64336033G
H8/36032	HD64336032, HD64336032G

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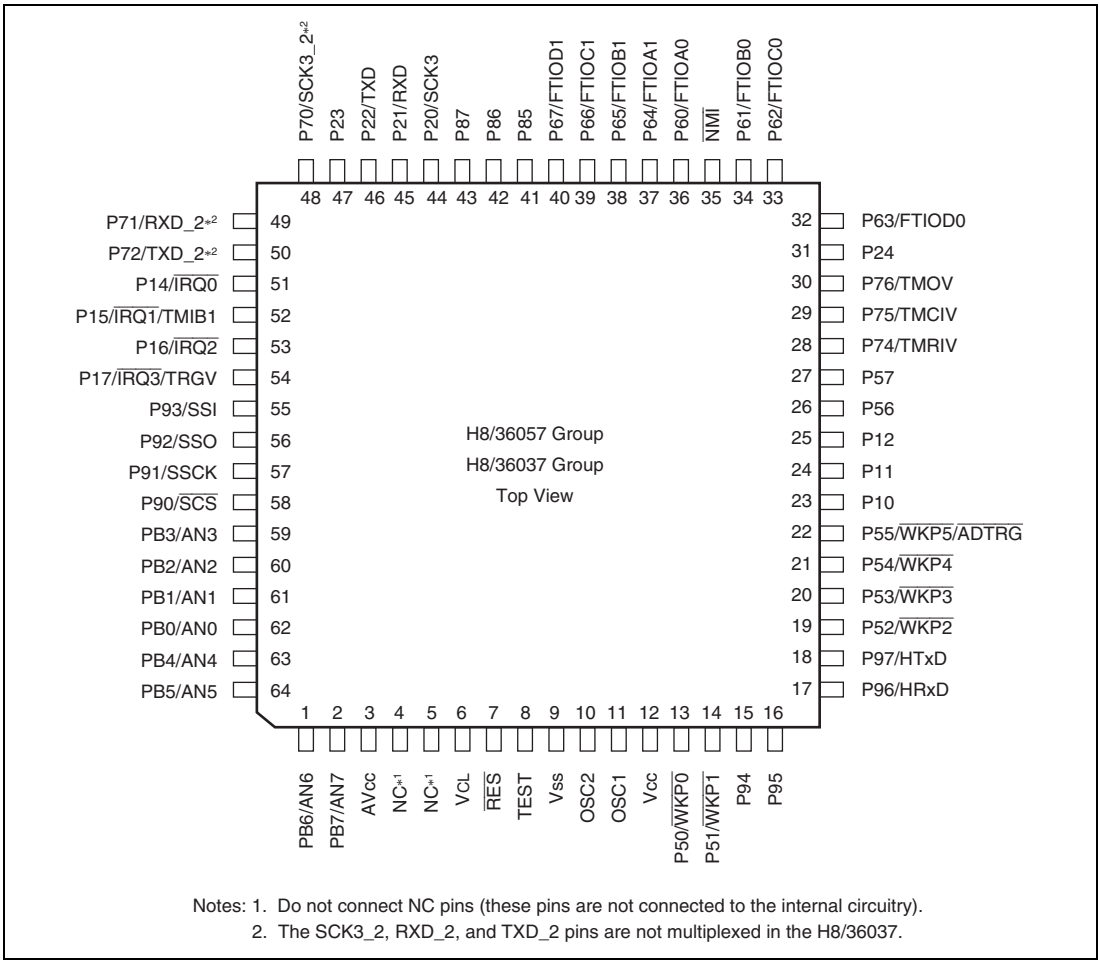
Rev.4.00 2006.05

1.3 Pin Arrangement



Notes: 1. Do not connect NC pins (these pins are not connected to the internal circuitry).
2. The SCK3_2, RXD_2, and TXD_2 pins are not multiplexed in the H8/36037.

Figure 1.2 Pin Arrangement of F-ZTAT™ and Masked ROM Versions (FP-64K, FP-64A)

The timer is counting, so the value read is not necessarily the same as the value in the timer load register. As a result, bits other than the intended bit in the timer counter may be modified and the modified value may be written to the timer load register.

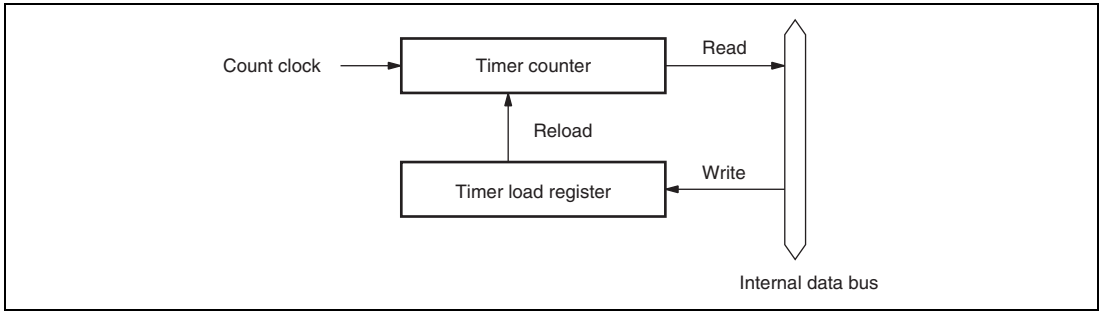


Figure 2.13 Example of Timer Configuration with Two Registers Allocated to Same Address

Example 2: The BSET instruction is executed for port 5.

P57 and P56 are input pins, with a low-level signal input at P57 and a high-level signal input at P56. P55 to P50 are output pins and output low-level signals. An example to output a high-level signal at P50 with a BSET instruction is shown below.

- Prior to executing BSET instruction

	P57	P56	P55	P54	P53	P52	P51	P50
Input/output	Input	Input	Output	Output	Output	Output	Output	Output
Pin state	Low level	High level	Low level	Low level	Low level	Low level	Low level	Low level
PCR5	0	0	1	1	1	1	1	1
PDR5	1	0	0	0	0	0	0	0

- BSET instruction executed instruction

```
BSET    #0,     @PDR5
```

The BSET instruction is executed for port 5.

6.1.4 Module Standby Control Register 2 (MSTCR2)

MSTCR2 allows the on-chip peripheral modules to enter a standby state in module units.

Bit	Bit Name	Initial Value	R/W	Description
7	MSTS3_2	0	R/W	SCI3_2 Module Standby The SCI3_2 enters standby mode when this bit is set to 1. Note: This bit is reserved in the H8/36037 Group. This bit is always read as 0.
6, 5	—	All 0	—	Reserved These bits are always read as 0.
4	MSTTB1	0	R/W	Timer B1 Module Standby The timer B1 enters standby mode when this bit is set to 1.
3, 2	—	All 0	—	Reserved These bits are always read as 0.
1	MSTTZ	0	R/W	Timer Z Module Standby The timer Z enters standby mode when this bit is set to 1.
0	—	0	—	Reserved This bit is always read as 0.

- P72/TXD_2* pin

Register	PMR1*	PCR7	
Bit Name	**TXD2***	**PCR72**	**Pin Function**
Setting Value	0	0	P72 input pin
		1	P72 output pin
	1	X	TXD_2 output pin*

[Legend]
X: Don't care.
Note: * The H8/36037 Group does not have this pin.

- P71/RXD_2* pin

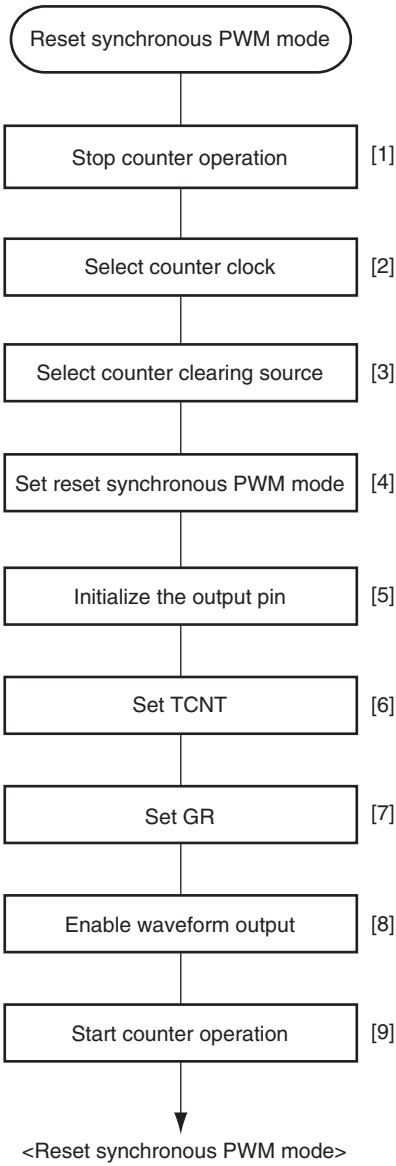
Register	SCR3_2*	PCR7	
Bit Name	**RE***	**PCR71**	**Pin Function**
Setting Value	0	0	P71 input pin
		1	P71 output pin
	1	X	RXD_2 input pin*

[Legend]
X: Don't care.
Note: * The H8/36037 Group does not have this pin.

- P70/SCK3_2* pin

Register	SCR3_2*		SMR2*	PCR7	
Bit Name	**CKE1***	**CKE0***	**COM***	**PCR70**	**Pin Function**
Setting Value	0	0	0	0	P70 input pin
				1	P70 output pin
	0	0	1	X	SCK3_2 output pin*
	0	1	X	X	SCK3_2 output pin*
	1	X	X	X	SCK3_2 input pin*

[Legend]
X: Don't care.
Note: * The H8/36037 Group does not have these pins.



[1] Clear bit STR0 in TSTR to 0 and stop the counter operation of TCNT_0. Set reset synchronous PWM mode after TCNT_0 stops.
[2] Select the counter clock with bits TPSC2 to TOSC0 in TCR. When an external clock is selected, select the external clock edge with bits CKEG1 and CKEG0 in TCR.
[3] Use bits CCLR1 and CCLR0 in TCR to select counter clearing source GRA_0.
[4] Select the reset synchronous PWM mode with bits CMD1 and CMD0 in TFCR. FTIOB0 to FTIOD0 and FTIOA1 to FTIOD1 become PWM output pins automatically.
[5] Set H'00 to TOCR.
[6] Set TCNT_0 as H'0000. TCNT1 does not need to be set.
[7] GRA_0 is a cycle register. Set a cycle for GRA_0. Set the changing point timing of the PWM output waveform for GRB_0, GRA_1, and GRB_1.
[8] Enable or disable the timer output by TOER.
[9] Set the STR bit in TSTR to 1 and start the counter operation.

Figure 12.26 Example of Reset Synchronous PWM Mode Setting Procedure

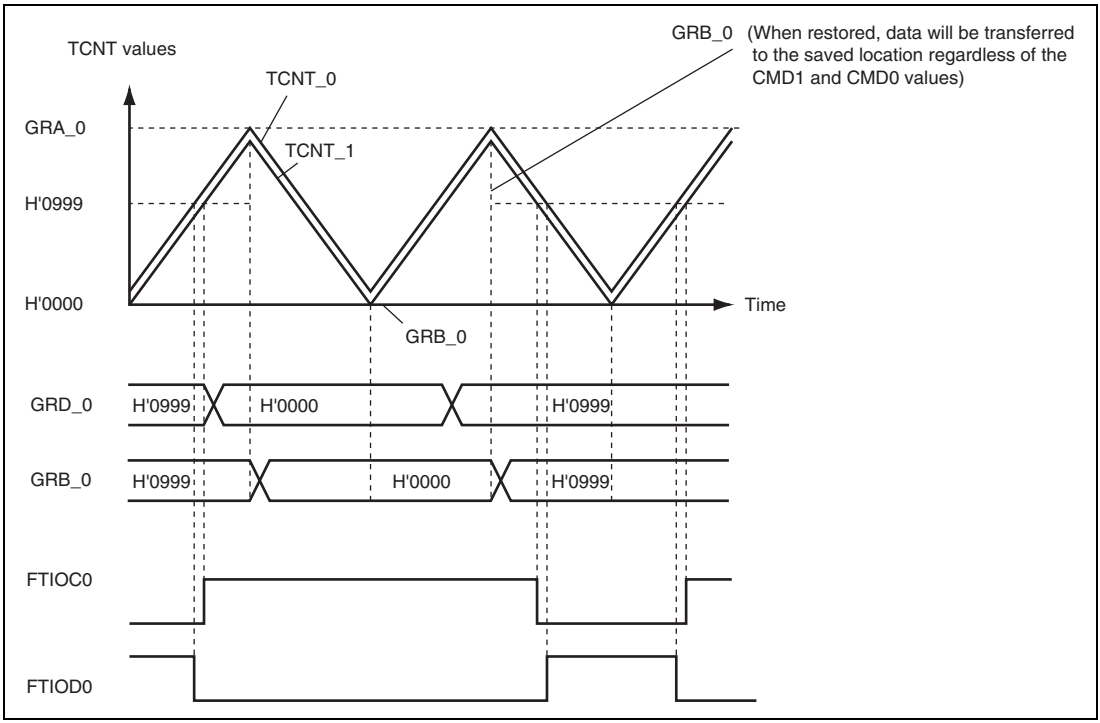


Figure 12.43 Buffer Operation (4)
(Buffer Operation in Complementary PWM Mode CMD1 = CMD0 = 1)

	Operating Frequency ϕ (MHz)					
	18			20		
Bit Rate (bit/s)	n	N	Error (%)	n	N	Error (%)
110	3	79	–0.12	3	88	–0.25
150	2	233	0.14	3	64	0.14
300	2	114	0.14	2	129	0.14
600	1	233	0.14	2	64	0.14
1200	1	114	0.14	1	129	0.14
2400	0	233	0.14	1	64	0.14
4800	0	114	0.14	0	129	0.14
9600	0	58	–0.96	0	64	0.14
19200	0	28	1.02	0	32	–1.36
31250	0	17	0.00	0	19	0.00
38400	0	14	–2.34	0	15	1.73

[Legend]

—: A setting is available but error occurs.

Table 14.4 Maximum Bit Rate for Each Frequency (Asynchronous Mode)

ϕ (MHz)	Maximum Bit Rate (bit/s)	n	N	ϕ (MHz)	Maximum Bit Rate (bit/s)	n	N
2	62500	0	0	8	250000	0	0
2.097152	65536	0	0	9.8304	307200	0	0
2.4576	76800	0	0	10	312500	0	0
3	93750	0	0	12	375000	0	0
3.6864	115200	0	0	12.288	384000	0	0
4	125000	0	0	14	437500	0	0
4.9152	153600	0	0	14.7456	460800	0	0
5	156250	0	0	14	500000	0	0
6	187500	0	0	17.2032	537600	0	0
6.144	192000	0	0	18	562500	0	0
7.3728	230400	0	0	20	625000	0	0

Table 14.5 Examples of BRR Settings for Various Bit Rates (Clocked Synchronous Mode) (2)

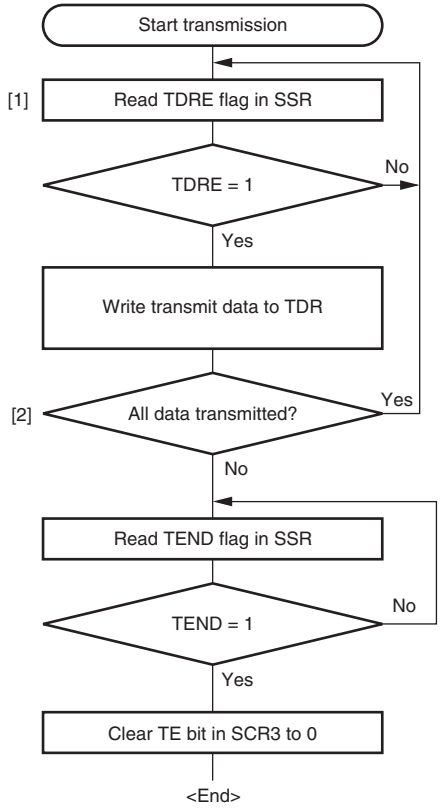
Bit Rate (bit/s)	Operating Frequency ϕ (MHz)			
	18		20	
	n	N	n	N
110	—	—	—	—
250	—	—	—	—
500	3	140	3	155
1k	3	69	3	77
2.5k	2	112	2	124
5k	1	224	1	249
10k	1	112	1	124
25k	0	179	0	199
50k	0	89	0	99
100k	0	44	0	49
250k	0	17	0	19
500k	0	8	0	9
1M	0	4	0	4
2M	—	—	—	—
2.5M	—	—	0	1
4M	—	—	—	—

[Legend]

Blank: No setting is available.

—: A setting is available but error occurs.

*: Continuous transfer is not possible.



[1] Read SSR and check that the TDRE flag is set to 1, then write transmit data to TDR. When data is written to TDR, the TDRE flag is automatically cleared to 0 and clocks are output to start the data transmission.

[2] To continue serial transmission, be sure to read 1 from the TDRE flag to confirm that writing is possible, then write data to TDR. When data is written to TDR, the TDRE flag is automatically cleared to 0.

Figure 14.11 Sample Serial Transmission Flowchart (Clocked Synchronous Mode)

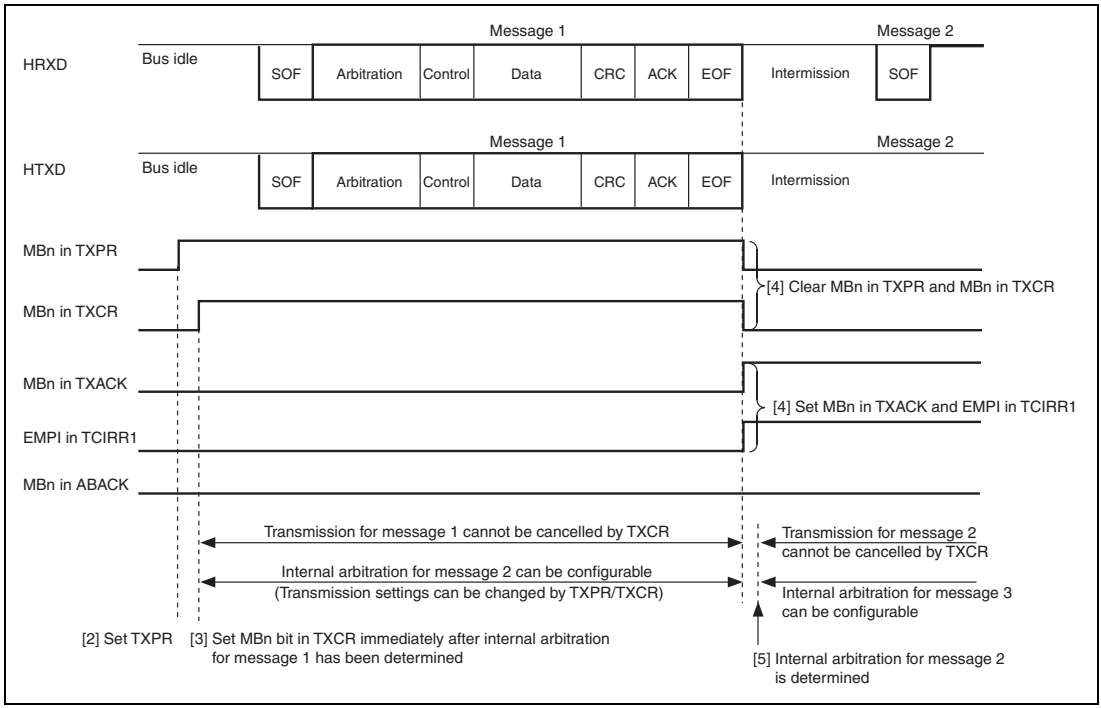


Figure 15.7 Internal Arbitration at Transmission Caused by TXCR/TXPR Setting

Arbitration Lost during Message Transmission: If an arbitration loss on the CAN bus occurs, the TinyCAN halts transmission, and starts message reception. If the DART bit for the transmission-requested message is cleared to 0, on the completion of reception, the transmission-requested message is retransmitted. However, if the DART bit is set to 1, it is not transmitted in frame 2. Figures 15.8 to 15.10 show the timings of the arbitration loss on the CAN bus. Procedure and operation are as follows.

1. Write data of a transmit message to MCn0, MCn4 to MCn7, and MDn0 to MDn7 [n = 1 to 3] before clearing the MBn bit in MBCR corresponding to the Mailbox of the transmit message to 0 (initial setting).
2. Set the corresponding MBn bit in TXPR to 1 (start condition issuance). Then, the start condition is generated.
3. The internal arbitration for message 1 is determined and the transmit message is transferred to the temporary buffer. After that, even if a transmit request cancellation is issued to the message being transmitted by the DART or MBn bit in TXCR, message 1 is transmitted continuously unless the TinyCAN detects an arbitration loss or error on the CAN bus.

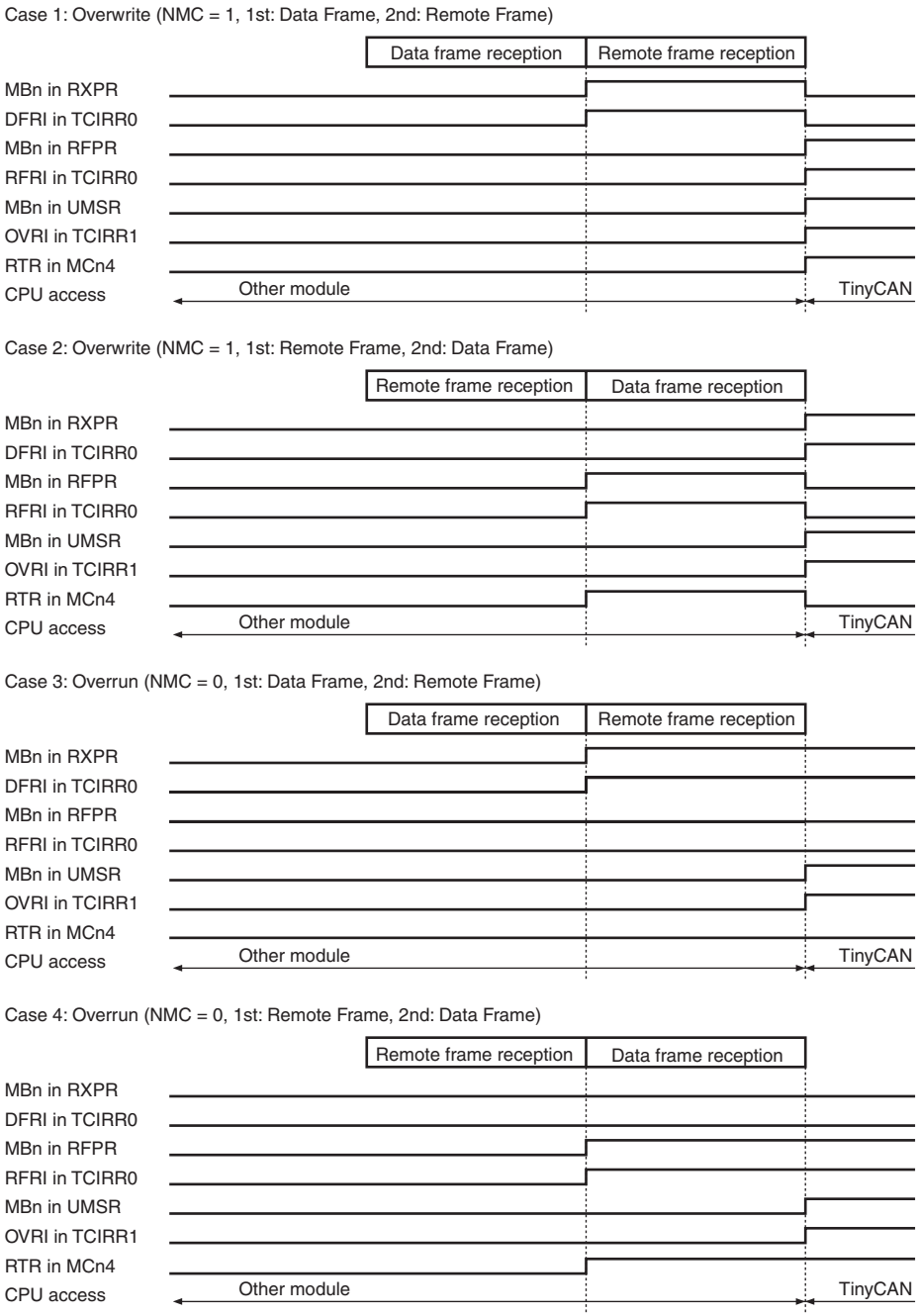


Figure 15.16 RXPR/RFPR Set/Clear Timing when Overrun/Overwrite Occurs

16.3.6 SS Receive Data Register (SSRDR)

SSRDR is an 8-bit register that stores received serial data. When the SSU has received one byte of serial data, it transfers the received serial data from SSTRSR and the data is stored. After this, SSTRSR is receive-enabled. As SSTRSR and SSRDR function as a double buffer in this way, continuous receive operations are possible. SSRDR is a read-only register and cannot be written to by the CPU. SSRDR is initialized to H'00.

16.3.7 SS Transmit Data Register (SSTDR)

SSTDR is an 8-bit register that stores serial data for transmission. SSTDR can be read or written to by the CPU at all times. When the SSU detects that SSTRSR is empty, it transfers the transmit data written in SSTDR to SSTRSR and starts serial transmission. If the next transmit data has already been written to SSTDR during serial transmission, continuous serial transmission is possible. SSTDR is initialized to H′00.

16.3.8 SS Shift Register (SSTRSR)

SSTRSR is a shift register that transmits and receives serial data. When transmit data is transferred from SSTDR to SSTRSR, bit 0 in SSTDR is transferred to bit 0 in SSTRSR while the MLS bit in SSMR is 0 (LSB-first transfer) and bit 7 in SSTDR is transferred to bit 0 in SSTRSR while the MLS bit in SSMR is 1 (MSB-first transfer). SSTRSR cannot be directly accessed by the CPU.

Table A.2 Operation Code Map (2)

Instruction code:

1st byte	2nd byte
AH AL	BH BL

AH AL \ BH	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
01	MOV				LDC/STC				SLEEP				Table A.2 (3)	Table A.2 (3)		Table A.2 (3)
0A	INC												ADD			
0B	ADDS					INC		INC	ADDS					INC		INC
0F	DAA												MOV			
10	SHLL			SHLL					SHAL			SHAL				
11	SHLR			SHLR					SHAR			SHAR				
12	ROTXL			ROTXL					ROTL			ROTL				
13	ROTXR			ROTXR					ROTR			ROTR				
17	NOT			NOT		EXTU		EXTU	NEG			NEG		EXTS		EXTS
1A	DEC												SUB			
1B	SUBS					DEC		DEC	SUB					DEC		DEC
1F	DAS												CMP			
58	BRA	BRN	BHI	BLS	BCC	BCS	BNE	BEQ	BVC	BVS	BPL	BMI	BGE	BLT	BGT	BLE
79	MOV	ADD	CMP	SUB	OR	XOR	AND									
7A	MOV	ADD	CMP	SUB	OR	XOR	AND									

Instruction	Mnemonic	Instruction Fetch I	Branch Addr. Read J	Stack Operation K	Byte Data Access L	Word Data Access M	Internal Operation N
BIOR	BIOR #xx:8, Rd	1					
	BIOR #xx:8, @ERd	2			1		
	BIOR #xx:8, @aa:8	2			1		
BIST	BIST #xx:3, Rd	1					
	BIST #xx:3, @ERd	2			2		
	BIST #xx:3, @aa:8	2			2		
BIXOR	BIXOR #xx:3, Rd	1					
	BIXOR #xx:3, @ERd	2			1		
	BIXOR #xx:3, @aa:8	2			1		
BLD	BLD #xx:3, Rd	1					
	BLD #xx:3, @ERd	2			1		
	BLD #xx:3, @aa:8	2			1		
BNOT	BNOT #xx:3, Rd	1					
	BNOT #xx:3, @ERd	2			2		
	BNOT #xx:3, @aa:8	2			2		
	BNOT Rn, Rd	1					
	BNOT Rn, @ERd	2			2		
	BNOT Rn, @aa:8	2			2		
BOR	BOR #xx:3, Rd	1					
	BOR #xx:3, @ERd	2			1		
	BOR #xx:3, @aa:8	2			1		
BSET	BSET #xx:3, Rd	1					
	BSET #xx:3, @ERd	2			2		
	BSET #xx:3, @aa:8	2			2		
	BSET Rn, Rd	1					
	BSET Rn, @ERd	2			2		
	BSET Rn, @aa:8	2			2		
BSR	BSR d:8	2		1			
	BSR d:16	2		1			2
BST	BST #xx:3, Rd	1					
	BST #xx:3, @ERd	2			2		
	BST #xx:3, @aa:8	2			2		

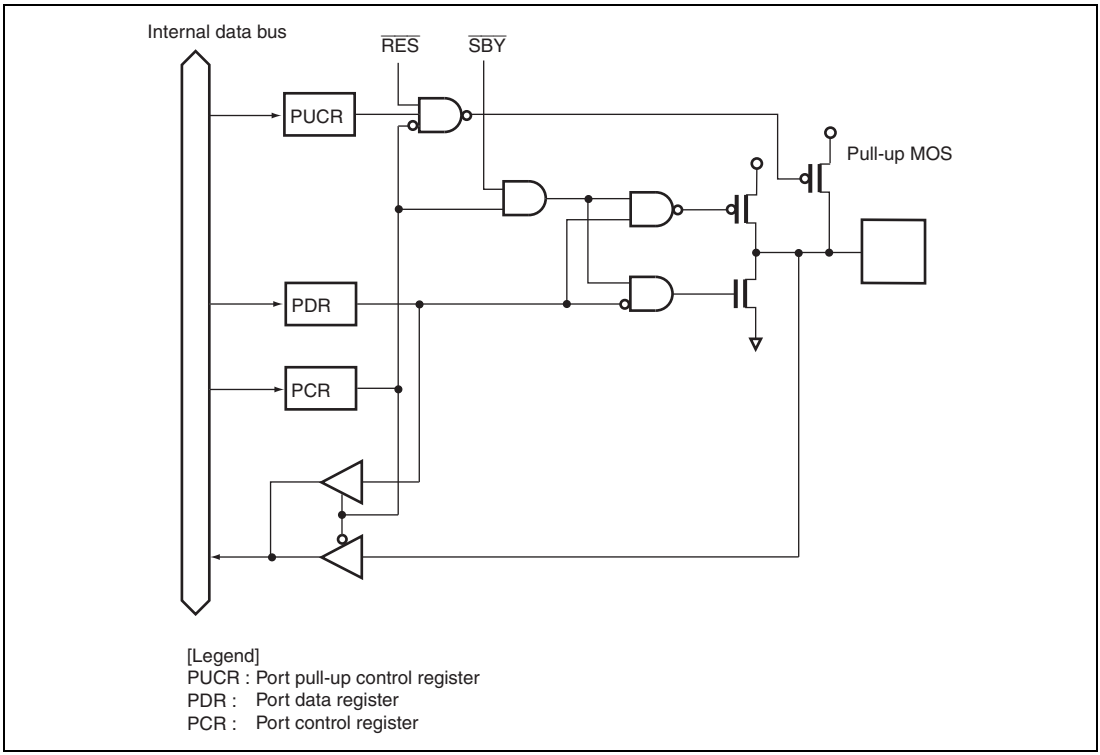
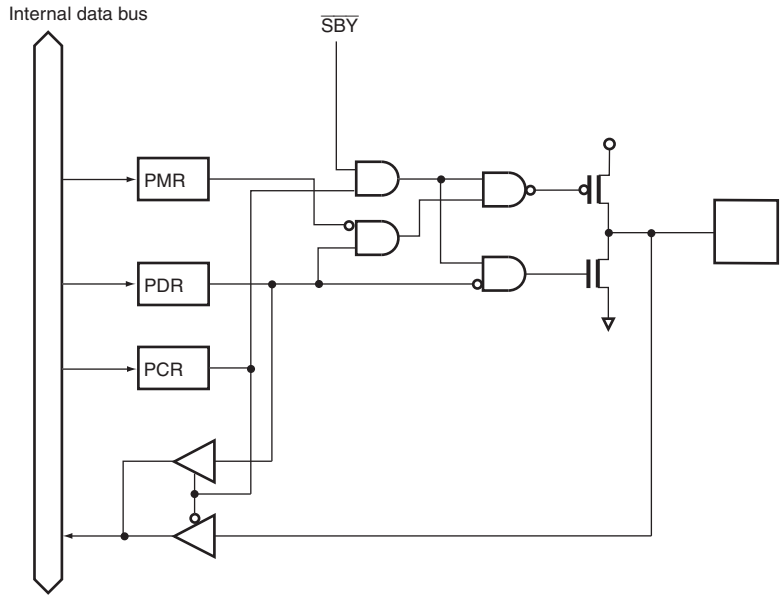


Figure B.4 Port 1 Block Diagram (P12, P11, P10)



[Legend]
PMR : Port mode register
PDR : Port data register
PCR : Port control register

Figure B.5 Port 2 Block Diagram (P24, P23)

Item	Page	Revision (See Manual for Details)
Table 22.2 DC Characteristics (1)	449	Amended
Table 22.12 DC Characteristics (1)	468	Note: 3. Pin states during current consumption measurement are given below (excluding current in the pull-up MOS transistors and output buffers).

Mode	$\overline{RES}$ Pin	Internal State
Active mode 1	V_{CC}	Operates
Active mode 2		Operates (ϕ_{OSC}/64)
Sleep mode 1	V_{CC}	Only timers operate
Sleep mode 2		Only timers operate(ϕ_{OSC}/64)

Figure 22.8 SSU Input/Output Timing (Four-Line Bus Communication Mode, Master, CPHS = 1) to Figure 22.11 SSU Input/Output Timing (Four-Line Bus Communication Mode, Slave, CPHS = 0)	481 to 484	t_{OH} deleted								
Table A.1 Instruction Set 2. Arithmetic Instructions	491	Amended								

Mnemonic		Operand Size	Condition Code						No. of States*1	
			I	H	N	Z	V	C	Normal	Advanced
DAA	DAA Rd	B	—	*	↕	↕	*	↕	2	