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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300H
Core Size	16-Bit
Speed	20MHz
Connectivity	CANbus, SCI, SSU
Peripherals	PWM, WDT
Number of I/O	45
Program Memory Size	56KB (56K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df36057fpjv

7.2.4 Flash Memory Power Control Register (FLPWCR)

FLPWCR enables or disables a transition to the flash memory power-down mode when the LSI switches to subactive mode. There are two modes: mode in which operation of the power supply circuit of flash memory is partly halted in power-down mode and flash memory can be read, and mode in which even if a transition is made to subactive mode, operation of the power supply circuit of flash memory is retained and flash memory can be read.

Bit	Bit Name	Initial Value	R/W	Description
7	PDWND	0	R/W	Power-Down Disable When this bit is 0 and a transition is made to subactive mode, the flash memory enters the power-down mode. When this bit is 1, the flash memory remains in the normal mode even after a transition is made to subactive mode.
6 to 0	—	All 0	—	Reserved These bits are always read as 0.

7.2.5 Flash Memory Enable Register (FENR)

Bit 7 (FLSHE) in FENR enables or disables the CPU access to the flash memory control registers, FLMCR1, FLMCR2, EBR1, and FLPWCR.

Bit	Bit Name	Initial Value	R/W	Description
7	FLSHE	0	R/W	Flash Memory Control Register Enable Flash memory control registers can be accessed when this bit is set to 1. Flash memory control registers cannot be accessed when this bit is set to 0.
6 to 0	—	All 0	—	Reserved These bits are always read as 0.

7.3.1 Boot Mode

Table 7.2 shows the boot mode operations between reset end and branching to the programming control program.

1. When boot mode is used, the flash memory programming control program must be prepared in the host beforehand. Prepare a programming control program in accordance with the description in section 7.4, Flash Memory Programming/Erasing.
2. SCI3 should be set to asynchronous mode, and the transfer format as follows: 8-bit data, 1 stop bit, and no parity.
3. When the boot program is initiated, the chip measures the low-level period of asynchronous SCI communication data (H'00) transmitted continuously from the host. The chip then calculates the bit rate of transmission from the host, and adjusts the SCI3 bit rate to match that of the host. The reset should end with the RXD pin high. The RXD and TXD pins should be pulled up on the board if necessary. After the reset is complete, it takes approximately 100 states before the chip is ready to measure the low-level period.
4. After matching the bit rates, the chip transmits one H'00 byte to the host to indicate the completion of bit rate adjustment. The host should confirm that this adjustment end indication (H'00) has been received normally, and transmit one H'55 byte to the chip. If reception could not be performed normally, initiate boot mode again by a reset. Depending on the host's transfer bit rate and system clock frequency of this LSI, there will be a discrepancy between the bit rates of the host and the chip. To operate the SCI properly, set the host's transfer bit rate and system clock frequency of this LSI within the ranges listed in table 7.3.
5. In boot mode, a part of the on-chip RAM area is used by the boot program. The area H'F780 to H'FEEF is the area to which the programming control program is transferred from the host. The boot program area cannot be used until the execution state in boot mode switches to the programming control program.
6. Before branching to the programming control program, the chip terminates transfer operations by the SCI3 (by clearing the RE and TE bits in SCR to 0), however the adjusted bit rate value remains set in BRR. Therefore, the programming control program can still use it for transfer of program data or verify data with the host. The TXD pin is high (PCR22 = 1, P22 = 1). The contents of the CPU general registers are undefined immediately after branching to the programming control program. These registers must be initialized at the beginning of the programming control program, as the stack pointer (SP), in particular, is used implicitly in subroutine calls, etc.
7. Boot mode can be cleared by a reset. End the reset after driving the reset pin low, waiting at least 20 states, and then setting the $\overline{\text{NMI}}$ pin. Boot mode is also cleared when a WDT overflow occurs.
8. Do not change the TEST pin and $\overline{\text{NMI}}$ pin input levels in boot mode.

Section 9 I/O Ports

This LSI has forty-five general I/O ports and eight general input-only ports. Port 6 is a large current port, which can drive 20 mA ($@V_{OL}$ = 1.5 V) when a low level signal is output. Any of these ports can become an input port immediately after a reset. They can also be used as I/O pins of the on-chip peripheral modules or external interrupt input pins, and these functions can be switched depending on the register settings. The registers for selecting these functions can be divided into two types: those included in I/O ports and those included in each on-chip peripheral module. General I/O ports are comprised of the port control register for controlling inputs/outputs and the port data register for storing output data and can select inputs/outputs in bit units.

For functions in each port, see appendix B.1, I/O Port Block Diagrams. For the execution of bit-manipulation instructions to the port control register and port data register, see section 2.8.3, Bit Manipulation Instruction.

9.1 Port 1

Port 1 is a general I/O port also functioning as IRQ interrupt input pins, a timer B1 input pin, and a timer V input pin. Figure 9.1 shows its pin configuration.

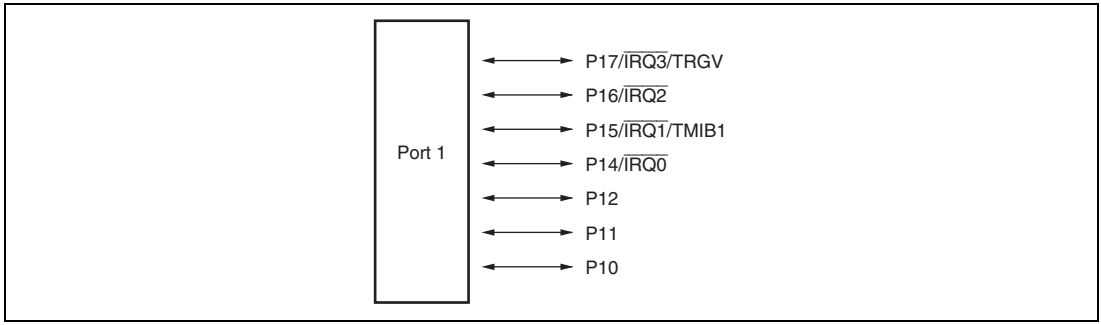


Figure 9.1 Port 1 Pin Configuration

Port 1 has the following registers.

- Port mode register 1 (PMR1)
- Port control register 1 (PCR1)
- Port data register 1 (PDR1)
- Port pull-up control register 1 (PUCR1)

12.3 Register Descriptions

The timer Z has the following registers.

Common

- Timer start register (TSTR)
- Timer mode register (TMDR)
- Timer PWM mode register (TPMR)
- Timer function control register (TFCR)
- Timer output master enable register (TOER)
- Timer output control register (TOCR)

Channel 0

- Timer control register_0 (TCR_0)
- Timer I/O control register A_0 (TIORA_0)
- Timer I/O control register C_0 (TIORC_0)
- Timer status register_0 (TSR_0)
- Timer interrupt enable register_0 (TIER_0)
- PWM mode output level control register_0 (POCR_0)
- Timer counter_0 (TCNT_0)
- General register A_0 (GRA_0)
- General register B_0 (GRB_0)
- General register C_0 (GRC_0)
- General register D_0 (GRD_0)

Channel 1

- Timer control register_1 (TCR_1)
- Timer I/O control register A_1 (TIORA_1)
- Timer I/O control register C_1 (TIORC_1)
- Timer status register_1 (TSR_1)
- Timer interrupt enable register_1 (TIER_1)
- PWM mode output level control register_1 (POCR_1)
- Timer counter_1 (TCNT_1)
- General register A_1 (GRA_1)
- General register B_1 (GRB_1)

- General register C_1 (GRC_1)
- General register D_1 (GRD_1)

12.3.1 Timer Start Register (TSTR)

TSTR selects the operation/stop for the TCNT counter.

Bit	Bit Name	Initial Value	R/W	Description
7 to 2	—	All 1	—	Reserved These bits are always read as 1 and cannot be modified.
1	STR1	0	R/W	Channel 1 Counter Start 0: TCNT_1 halts counting 1: TCNT_1 starts counting
0	STR0	0	R/W	Channel 0 Counter Start 0: TCNT_0 halts counting 1: TCNT_0 starts counting

Figure 12.14 shows an example of toggle output.

In this example, TCNT has been designated as a periodic counter (with counter clearing on compare match B), and settings have been made such that the output is toggled by both compare match A and compare match B.

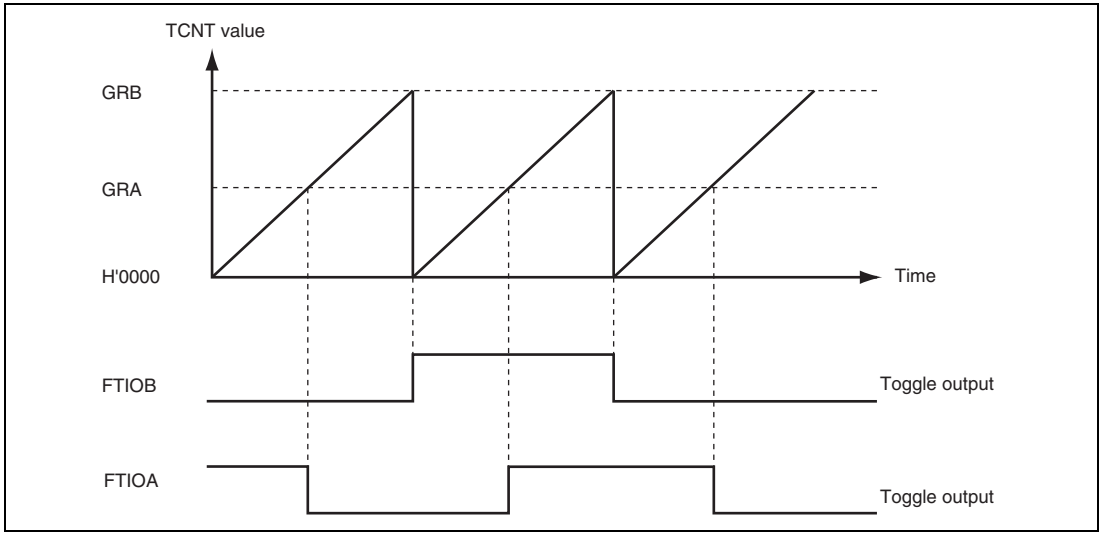


Figure 12.14 Example of Toggle Output Operation

14.4.2 SCI3 Initialization

Before transmitting and receiving data, you should first clear the TE and RE bits in SCR3 to 0, then initialize the SCI3 as described below. When the operating mode, or transfer format, is changed for example, the TE and RE bits must be cleared to 0 before making the change using the following procedure. When the TE bit is cleared to 0, the TDRE flag is set to 1. Note that clearing the RE bit to 0 does not initialize the contents of the RDRF, PER, FER, and OER flags, or the contents of RDR. When the external clock is used in asynchronous mode, the clock must be supplied even during initialization.

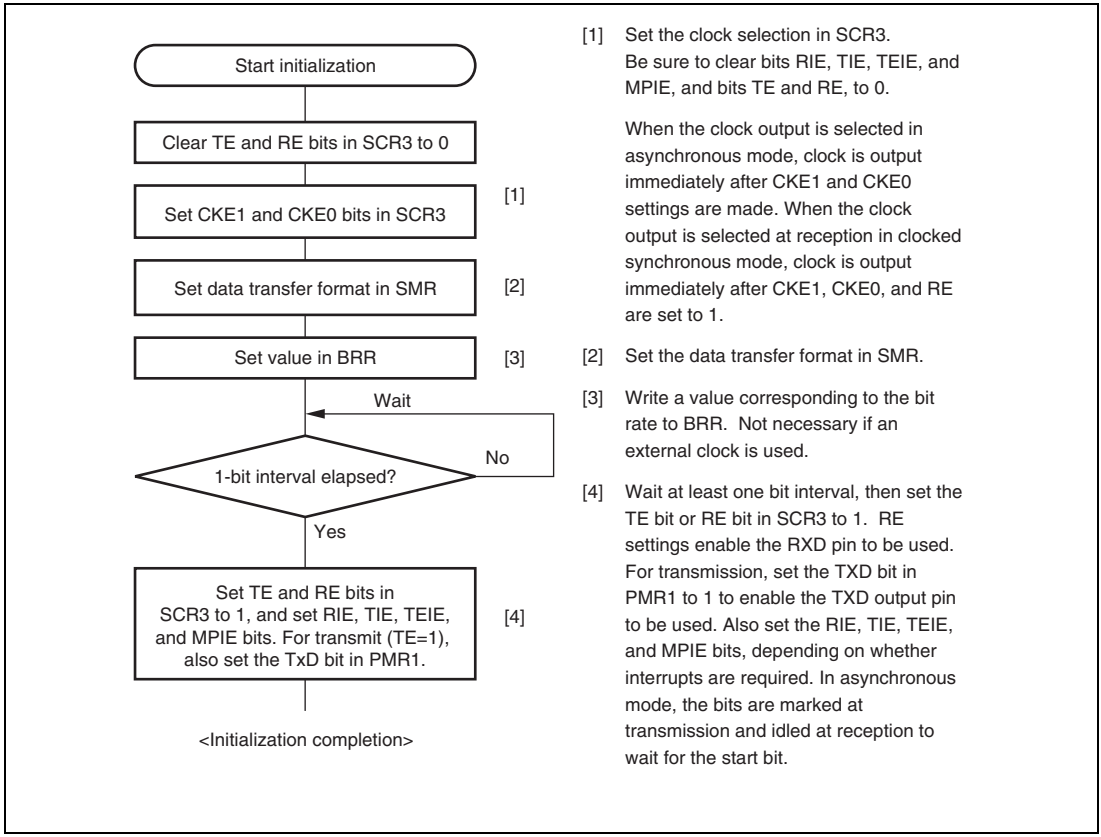


Figure 14.4 Sample SCI3 Initialization Flowchart

Bit	Bit Name	Initial Value	R/W	Description
3	DEC	0	R/W	Error Count Disable Bit Enables or disables the TEC and REC to be functional. 0: TEC and REC function according to CAN specification 1: TEC and REC is disabled to function (count value is retained, enabled only in test mode)
2	DRXIN	0	R/W	HRXD Pin Input Enable Enables or disables the HRXD pin to be supplied into the CDLC. 0: Input from the CAN bus to the HRXD pin is enabled 1: Input from the CAN bus to the HRXD pin is disabled (enabled only in test mode) • When INTLE = 0, the HRXD pin always holds recessive data. • When INTLE = 1, data is input from the internal HTXD to the HRXD pin.
1	DTXOT	0	R/W	HTXD Pin Output Enable Enables or disables the HTXD pin to output the CAN bus. 0: Output from the HTXD pin to the CAN bus is enabled 1: Output from the HTXD pin to the CAN bus is disabled (enabled only in test mode) • When INTLE = 0, the HTXD pin always outputs recessive data to the CAN bus. • When INTLE = 1, the internal HTXD outputs data to the internal HRXD.
0	INTLE	0	R/W	Internal Loop Enable Enables or disables connection between the internal HTXD and internal HRXD. 0: Internal HRXD is supplied from the HRXD pin 1: Internal HRXD is supplied from the internal HTXD (enabled only in test mode)

15.3.13 Unread Message Status Register (UMSR)

UMSR is a status flag that indicates that an unread message in each Mailbox has been overwritten by a new receive message or a new receive message has been discarded.

Bit	Bit Name	Initial Value	R/W	Description
7 to 4	—	All 0	—	Reserved These bits are always read as 0.
3	MB3	0	R/(W)*	Status flags indicating that a new receive message has overwritten/overrun an unread message. [Setting condition] When a new message is received before the corresponding bit in RXPR or RFPR is cleared to 0 [Clearing condition] When 1 is written to these bits
2	MB2	0	R/(W)*	
1	MB1	0	R/(W)*	
0	MB0	0	R/(W)*	

Note: * Only 1 can be written to clear the flag.

Serial Data Reception: Figure 16.7 shows an example of the SSU operation for reception. In serial reception, the SSU operates as described below.

When the SSU is set as a master device, it outputs a synchronous clock and inputs data. When the SSU is set as a slave device, it inputs data in synchronized with the input clock. When the SSU is set as a master device, it outputs a receive clock and starts reception by performing dummy read on SSRDR.

After eight bits of data is received, the RDRF bit in SSSR is set to 1 and received data is stored in SSRDR. If the RIE bit in SSER is set to 1 at this time, a RXI is generated. If SSRDR is read, the RDRF bit is automatically cleared to 0.

When the SSU is set as a master device and reception is ended, received data is read after setting the RSSTP bit in SSER to 1. Then the SSU outputs eight bits of clocks and operation is stopped. After that, the RE and RSSTP bits are cleared to 0 and the last received data is read. Note that if SSRDR is read while the RE bit is set to 1, received clock is output again.

When the eighth clock rises while the RDRF bit is 1, the ORER bit in SSSR is set. Then an overrun error (OEI) is generated and operation is stopped. When the ORER bit in SSSR is set to 1, reception cannot be performed. Therefore confirm that the ORER bit is cleared to 0 before reception.

Figure 16.8 shows a sample flowchart for serial data reception.

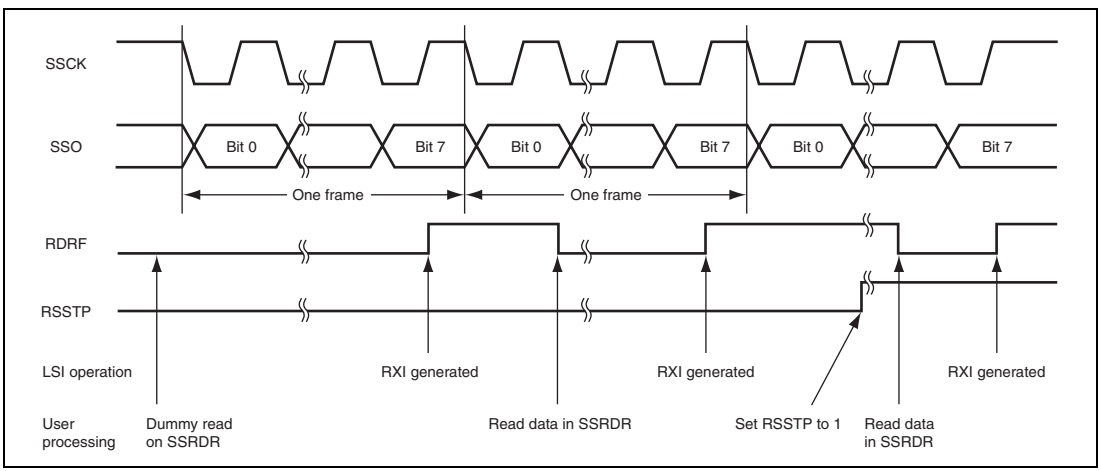


Figure 16.7 Example of Operation in Data Reception (MSS = 1)

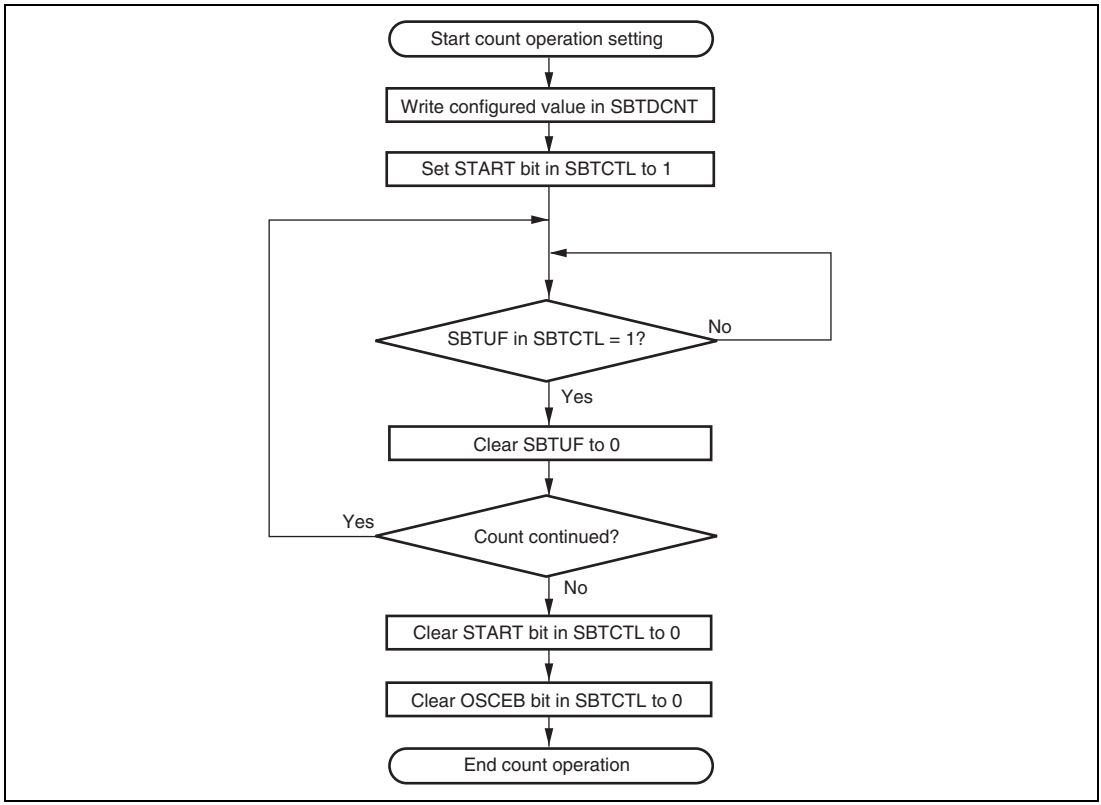


Figure 17.5 Count Operation Flowchart

Bit	Bit Name	Initial Value	R/W	Description
0	LVDUE	0	R/W	Voltage-Rise-Interrupt Enable 0: Interrupt on the power-supply voltage rising above the selected detection level disabled 1: Interrupt on the power-supply voltage rising above the selected detection level enabled

Note: * Not initialized by LVDR but initialized by a power-on reset or WDT reset.

Table 19.1 LVDCR Settings and Select Functions

LVDCR Settings					Select Functions			
LVDE	LVDSEL	LVDRE	LVDDE	LVDUE	Power-On Reset	LVDR	Low-Voltage-Detection Falling Interrupt	Low-Voltage-Detection Rising Interrupt
0	*	*	*	*	O	—	—	—
1	1	1	0	0	O	O	—	—
1	0	0	1	0	O	—	O	—
1	0	0	1	1	O	—	O	O
1	0	1	1	1	O	O	O	O

Note: * means invalid.

19.3 Operation

19.3.1 Power-On Reset Circuit

Figure 19.2 shows the timing of the operation of the power-on reset circuit. As the power-supply voltage rises, the capacitor which is externally connected to the $\overline{\text{RES}}$ pin is gradually charged via the on-chip pull-up resistor (typ. 150 kΩ). Since the state of the $\overline{\text{RES}}$ pin is transmitted within the chip, the prescaler S and the entire chip are in their reset states. When the level on the $\overline{\text{RES}}$ pin reaches the specified value, the prescaler S is released from its reset state and it starts counting. The OVF signal is generated to release the internal reset signal after the prescaler S has counted 131,072 clock (ϕ) cycles. The noise canceler of approximately 500 ns is incorporated to prevent the incorrect operation of the chip by noise on the $\overline{\text{RES}}$ pin.

To achieve stable operation of this LSI, the power supply needs to rise to its full level and settles within the specified time. The maximum time required for the power supply to rise and settle after power has been supplied (t_{PWON}) is determined by the oscillation frequency (f_{OSC}) and capacitance which is connected to $\overline{\text{RES}}$ pin ($C_{\overline{\text{RES}}}$). If t_{PWON} means the time required to reach 90 % of power supply voltage, the power supply circuit should be designed to satisfy the following formula.

$$t_{PWON}\ (\text{ms}) \leq 90 \times C_{\overline{\text{RES}}}\ (\mu\text{F}) + 162/f_{OSC}\ (\text{MHz})$$

($t_{PWON} \leq 3000$ ms, $C_{\overline{\text{RES}}} \geq 0.22$ μF, and $f_{OSC} = 10$ in 2-MHz to 10-MHz operation)

Note that the power supply voltage (Vcc) must fall below Vpor = 100 mV and rise after charge on the $\overline{\text{RES}}$ pin is removed. To remove charge on the $\overline{\text{RES}}$ pin, it is recommended that the diode should be placed near Vcc. If the power supply voltage (Vcc) rises from the point above Vpor, a power-on reset may not occur.

Section 20 Power Supply Circuit

This LSI incorporates an internal power supply step-down circuit. Use of this circuit enables the internal power supply to be fixed at a constant level of approximately 3.0 V, independently of the voltage of the power supply connected to the external V_{CC} pin. As a result, the current consumed when an external power supply is used at 3.0 V or above can be held down to virtually the same low level as when used at approximately 3.0 V. If the external power supply is 3.0 V or below, the internal voltage will be practically the same as the external voltage. It is, of course, also possible to use the same level of external power supply voltage and internal power supply voltage without using the internal power supply step-down circuit.

20.1 When Using Internal Power Supply Step-Down Circuit

Connect the external power supply to the V_{CC} pin, and connect a capacitance of approximately 0.1 µF between V_{CL} and V_{SS}, as shown in figure 20.1. The internal step-down circuit is made effective simply by adding this external circuit. In the external circuit interface, the external power supply voltage connected to V_{CC} and the GND potential connected to V_{SS} are the reference levels. For example, for port input/output levels, the V_{CC} level is the reference for the high level, and the V_{SS} level is that for the low level. The A/D converter analog power supply is not affected by the internal step-down circuit.

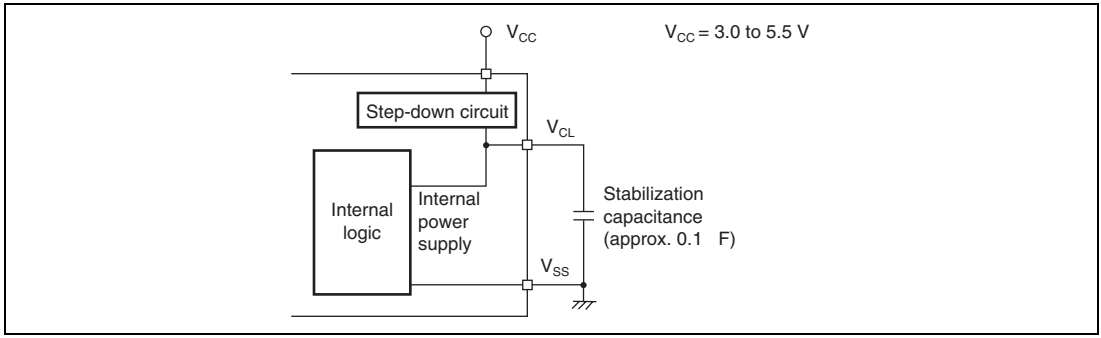
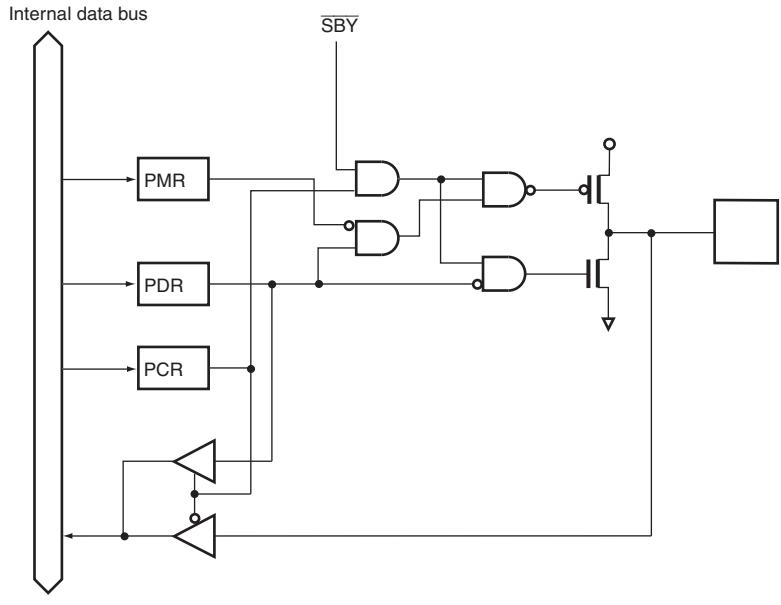


Figure 20.1 Power Supply Connection when Internal Step-Down Circuit is Used

Instruction	Mnemonic	Instruction Fetch I	Branch Addr. Read J	Stack Operation K	Byte Data Access L	Word Data Access M	Internal Operation N
Bcc	BLT d:8	2					
	BGT d:8	2					
	BLE d:8	2					
	BRA d:16(BT d:16)	2					2
	BRN d:16(BF d:16)	2					2
	BHI d:16	2					2
	BLS d:16	2					2
	BCC d:16(BHS d:16)	2					2
	BCS d:16(BLO d:16)	2					2
	BNE d:16	2					2
	BEQ d:16	2					2
	BVC d:16	2					2
	BVS d:16	2					2
	BPL d:16	2					2
	BMI d:16	2					2
	BGE d:16	2					2
	BLT d:16	2					2
	BGT d:16	2					2
	BLE d:16	2					2
BCLR	BCLR #xx:3, Rd	1					
	BCLR #xx:3, @ERd	2			2		
	BCLR #xx:3, @aa:8	2			2		
	BCLR Rn, Rd	1					
	BCLR Rn, @ERd	2			2		
	BCLR Rn, @aa:8	2			2		
BIAND	BIAND #xx:3, Rd	1					
	BIAND #xx:3, @ERd	2			1		
	BIAND #xx:3, @aa:8	2			1		
BILD	BILD #xx:3, Rd	1					
	BILD #xx:3, @ERd	2			1		
	BILD #xx:3, @aa:8	2			1		



[Legend]
PMR : Port mode register
PDR : Port data register
PCR : Port control register

Figure B.5 Port 2 Block Diagram (P24, P23)

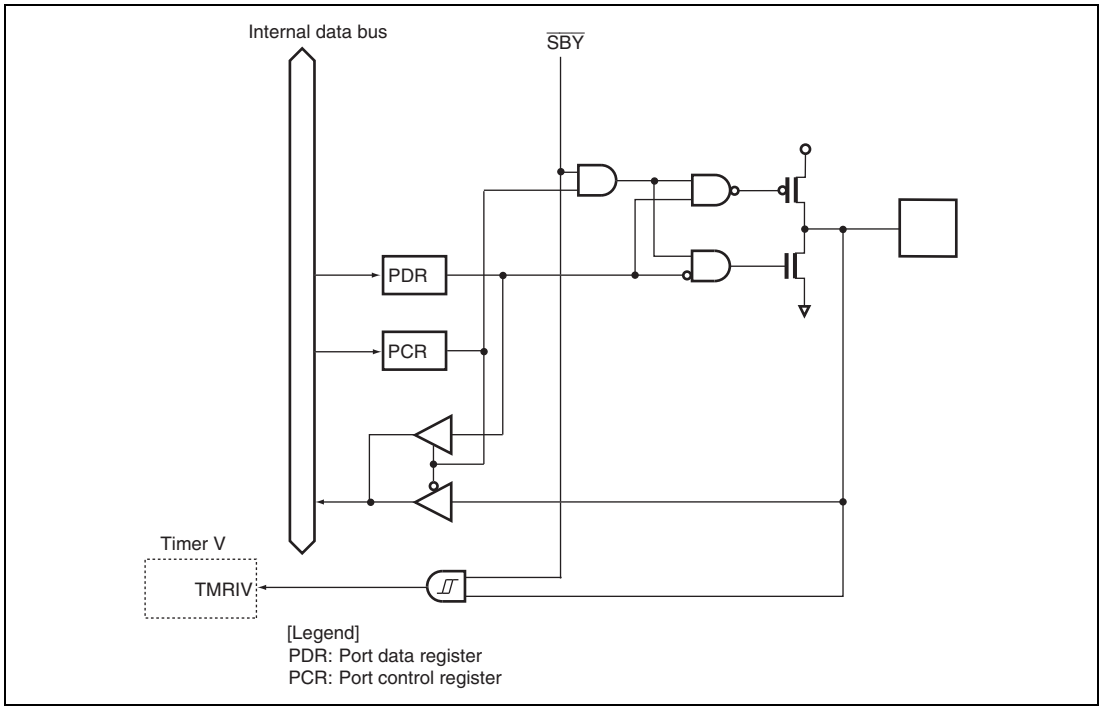


Figure B.15 Port 7 Block Diagram (P74)

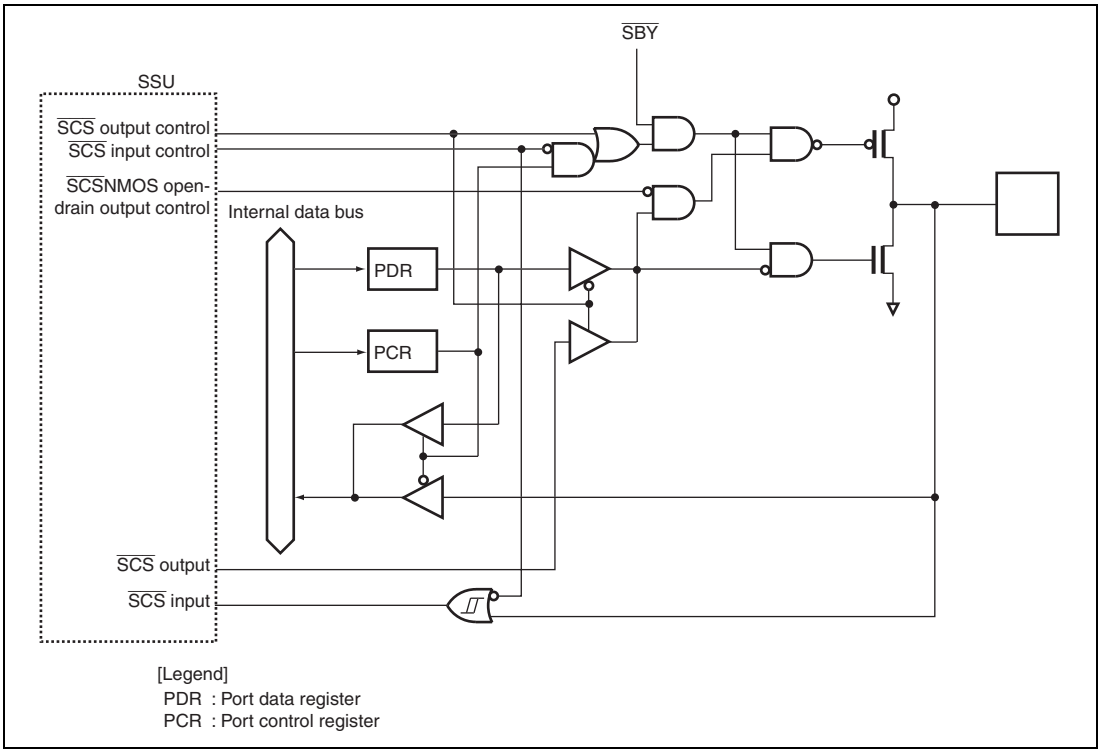


Figure B.26 Port 9 Block Diagram (P90)