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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300H
Core Size	16-Bit
Speed	20MHz
Connectivity	CANbus, SCI, SSU
Peripherals	PWM, WDT
Number of I/O	45
Program Memory Size	56KB (56K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df36057fpv

2.7 CPU States

There are four CPU states: the reset state, program execution state, program halt state, and exception-handling state. The program execution state includes active mode and subactive mode. For the program halt state, there are a sleep mode, standby mode, and sub-sleep mode. These states are shown in figure 2.11. Figure 2.12 shows the state transitions. For details on program execution state and program halt state, refer to section 6, Power-Down Modes. For details on exception processing, refer to section 3, Exception Handling.

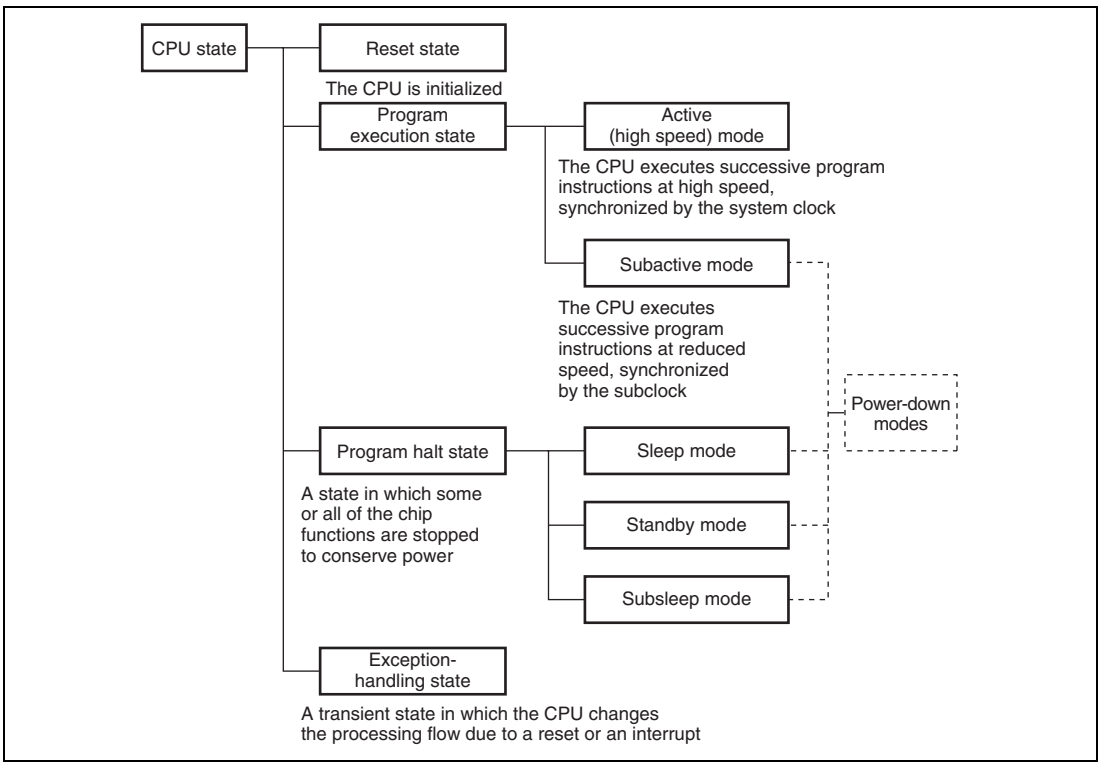

Figure 2.11 CPU Operation States

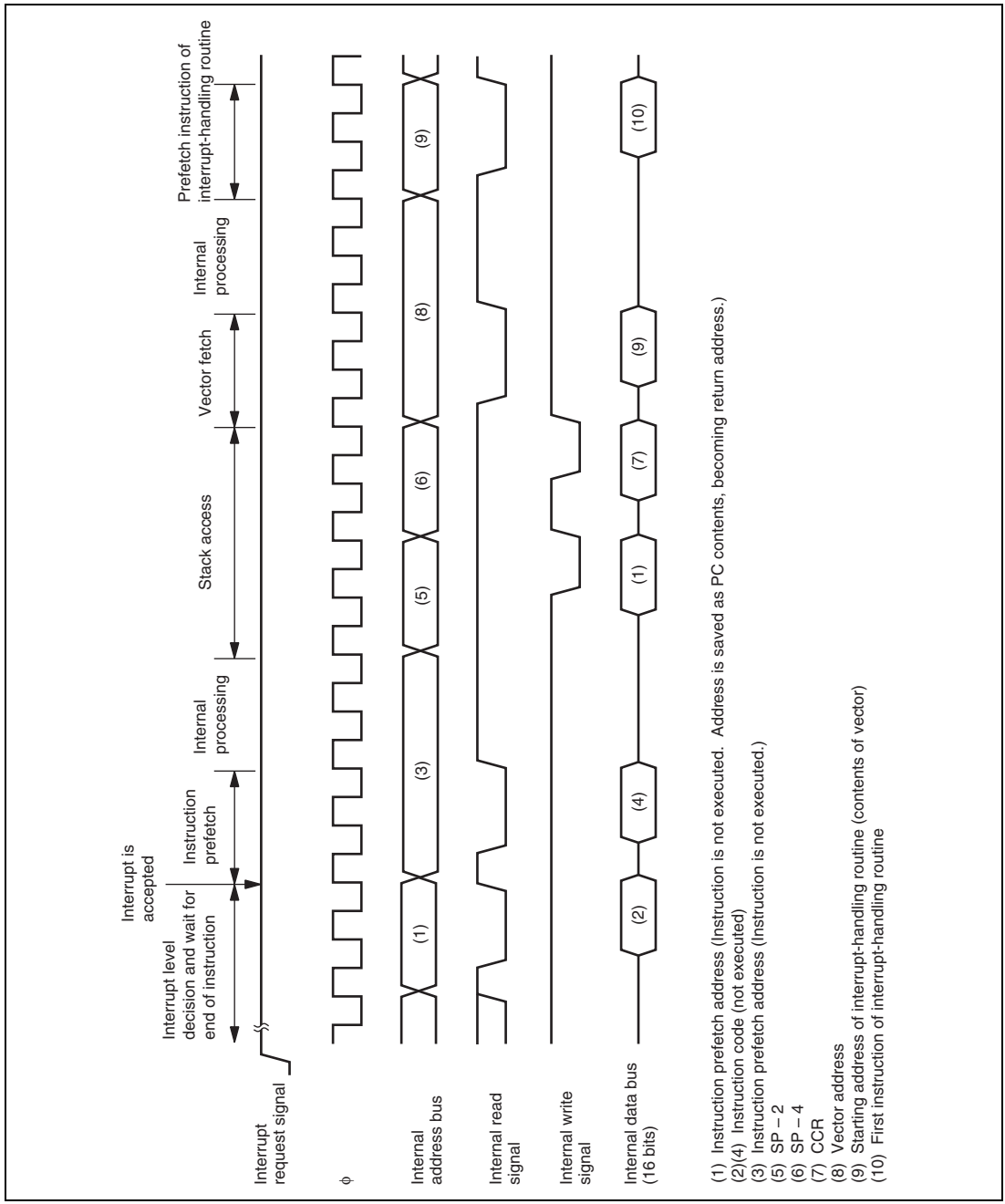

Figure 3.3 Interrupt Sequence

9.3 Port 5

Port 5 is a general I/O port also functioning as an A/D trigger input pin and a wakeup interrupt input pin. Each pin of the port 5 is shown in figure 9.3. The register setting of the I^2C bus interface register has priority for functions of the pins P57/SCL and P56/SDA. Since the output buffer for pins P56 and P57 has the NMOS push-pull structure, it differs from an output buffer with the CMOS structure in the high-level output characteristics (see section 22, Electrical Characteristics).

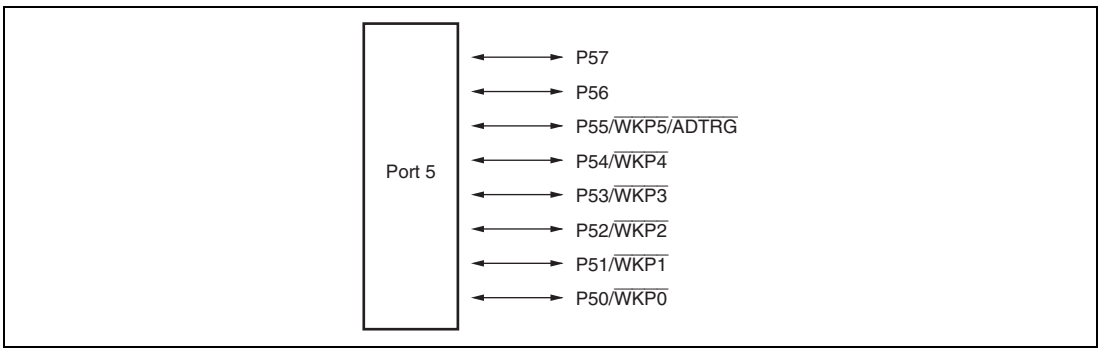

Figure 9.3 Port 5 Pin Configuration

Port 5 has the following registers.

- Port mode register 5 (PMR5)
- Port control register 5 (PCR5)
- Port data register 5 (PDR5)
- Port pull-up control register 5 (PUCR5)

9.4.2 Port Data Register 6 (PDR6)

PDR6 is a general I/O port data register of port 6.

Bit	Bit Name	Initial Value	R/W	Description
7	P67	0	R/W	Stores output data for port 6 pins.
6	P66	0	R/W	If PDR6 is read while PCR6 bits are set to 1, the value stored in PDR6 are read. If PDR6 is read while PCR6 bits are cleared to 0, the pin states are read regardless of the value stored in PDR6.
5	P65	0	R/W	
4	P64	0	R/W	
3	P63	0	R/W	
2	P62	0	R/W	
1	P61	0	R/W	
0	P60	0	R/W	

9.4.3 Pin Functions

The correspondence between the register specification and the port functions is shown below.

- P67/FTIOD1 pin

Register	TOER	TFCR	TPMR	TIORC1	PCR6	
Bit Name	ED1	CMD1, CMD0	PWMD1	IOD2 to IOD0	PCR67	Pin Function
Setting Value	1	00	0	000 or 1XX	0	P67 input/FTIOD1 input pin
					1	P67 output pin
	0	00	0	001 or 01X	X	FTIOD1 output pin
			1	XXX		
		Other than 00	X	XXX		

[Legend]

X: Don't care.

12.3.5 Timer Output Master Enable Register (TOER)

TOER enables/disables the outputs for channel 0 and channel 1. When $\overline{\text{WKP4}}$ is selected for inputs, if a low level signal is input to $\overline{\text{WKP4}}$, the bits in TOER are set to 1 to disable the output for timer Z.

Bit	Bit Name	Initial Value	R/W	Description
7	ED1	1	R/W	Master Enable D1 0: FTIOD1 pin output is enabled according to the TPMR, TFCR, and TIORC_1 settings 1: FTIOD1 pin output is disabled regardless of the TPMR, TFCR, and TIORC_1 settings (FTIOD1 pin is operated as an I/O port).
6	EC1	1	R/W	Master Enable C1 0: FTIOC1 pin output is enabled according to the TPMR, TFCR, and TIORC_1 settings 1: FTIOC1 pin output is disabled regardless of the TPMR, TFCR, and TIORC_1 settings (FTIOC1 pin is operated as an I/O port).
5	EB1	1	R/W	Master Enable B1 0: FTIOB1 pin output is enabled according to the TPMR, TFCR, and TIORA_1 settings 1: FTIOB1 pin output is disabled regardless of the TPMR, TFCR, and TIORA_1 settings (FTIOB1 pin is operated as an I/O port).
4	EA1	1	R/W	Master Enable A1 0: FTIOA1 pin output is enabled according to the TPMR, TFCR, and TIORA_1 settings 1: FTIOA1 pin output is disabled regardless of the TPMR, TFCR, and TIORA_1 settings (FTIOA1 pin is operated as an I/O port).
3	ED0	1	R/W	Master Enable D0 0: FTIOD0 pin output is enabled according to the TPMR, TFCR, and TIORC_0 settings 1: FTIOD0 pin output is disabled regardless of the TPMR, TFCR, and TIORC_0 settings (FTIOD0 pin is operated as an I/O port).

Canceling Procedure of Complementary PWM Mode: Figure 12.30 shows the complementary PWM mode canceling procedure.

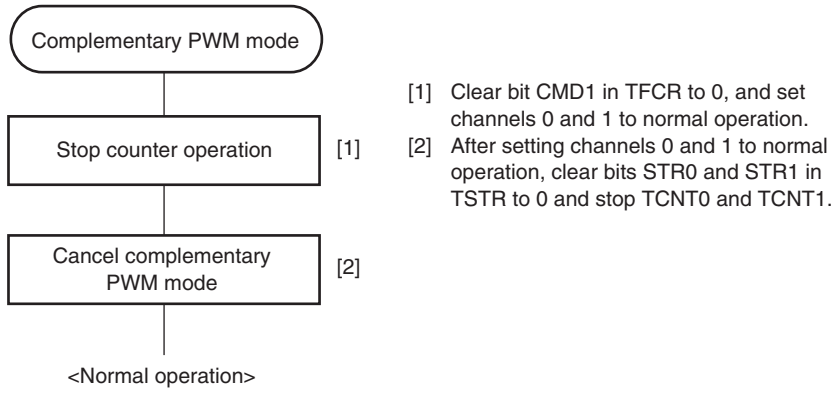

Figure 12.30 Canceling Procedure of Complementary PWM Mode

- To output a 100%-duty cycle waveform, write H'0000 while previous GR value < TCNT_0 ≤ GRA_0.
- To change duty cycles while a waveform with a duty cycle of 0% or 100% is being output, make sure the following procedure.
- To change duty cycles while a 0%-duty cycle waveform is being output, write to GR while H'0000 ≤TCNT_1 < previous GR value.
- To change duty cycles while a 100%-duty cycle waveform is being output, write to GR while previous GR value< TCNT_0 ≤ GRA_0.

  Note that changing from a 0%-duty cycle waveform to a 100%-duty cycle waveform

B. When buffer operation is used and TPSC2 = TPSC1 = TPSC0 = 0.

   Write H'0000 or a value equal to or more than the GRA_0 value to the buffer register.

   - To output a 0%-duty cycle waveform, write a value equal to or more than the GRA_0value to the buffer register.
   - To output a 100%-duty cycle waveform, write H'0000 to the buffer register.

     For details on buffer operation, see section 12.4.8, Buffer Operation.

C. When buffer operation is not used and other than TPSC2 = TPSC1 = TPSC0 = 0.

   Write a value which satisfies GRA_0 + 1 < GR < H'FFFF to GR directly at the timing shown below.

   - To output a 0%-duty cycle waveform, write the value while H'0000 is TCNT_1 < previous GR value
   - To output a 100%-duty cycle waveform, write the value while previous GR value < TCNT_0 ≤ GRA_0.

To change duty cycles while a waveform with a duty cycle of 0% and 100% is being output, the following procedure must be followed.

- To change duty cycles while a 0%-duty cycle waveform is being output, write to GR while H'0000 ≤ TCNT_1 < previous GR value.
- To change duty cycles while a 100%-duty cycle waveform is being output, write to GR while previous GR value< TCNT_0 ≤ GRA_0.

  Note that changing from a 0%-duty cycle waveform to a 100%-duty cycle waveform and vice versa is not possible.

D. Buffer operation is used and other than TPSC2 = TPSC1 = TPSC0 = 0

   Write a value which satisfies GRA_0 + 1 < GR < H'FFFF to the buffer register. A waveform with a duty cycle of 0% can be output. However, a waveform with a duty cycle of 100% cannot be output using the buffer operation. Also, the buffer operation cannot be used to change duty cycles while a waveform with a duty cycle of 100% is being output. For details on buffer operation, see section 12.4.8, Buffer Operation.

12.4.8 Buffer Operation

Buffer operation differs depending on whether GR has been designated for an input capture register or an output compare register, or in reset synchronous PWM mode or complementary PWM mode.

Table 12.8 shows the register combinations used in buffer operation.

Table 12.8 Register Combinations in Buffer Operation

General Register	Buffer Register
GRA	GRC
GRB	GRD

When GR is Output Compare Register: When a compare match occurs, the value in the buffer register of the corresponding channel is transferred to the general register.

This operation is illustrated in figure 12.35.

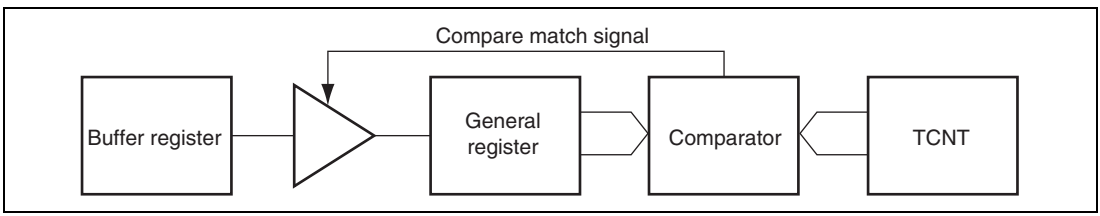

Figure 12.35 Compare Match Buffer Operation

When GR is Input Capture Register: When an input capture occurs, the value in TCNT is transferred to the general register and the value previously stored in the general register is transferred to the buffer register.

This operation is illustrated in figure 12.36.

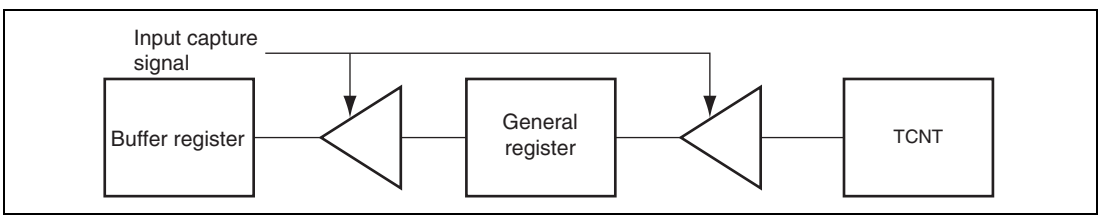

Figure 12.36 Input Capture Buffer Operation

Note on Clearing TSR Flag: When a specific flag in TSR is cleared, a combination of the BCLR or MOV instructions is used to read 1 from the flag and then write 0 to the flag. However, if another bit is set during this processing, the bit may also be cleared simultaneously. To avoid this, the following processing that does not use the BCLR instruction must be executed. Note that this note is only applied to the F-ZTAT version. This problem has already been solved in the mask ROM version.

```
Example: When clearing bit 4 (OVF) in TSR
MOV.B @TSR,R0L
MOV.B #B'11101111, R0L <..... Only the bit to be cleared is 0 and
                              the other bits are all set to 1.
MOV.B R0L,@TSR
```

Note on Writing to the TOA0 to TOD0 Bits and the TOA1 to TOD1 Bits in TOCR:
The TOA0 to TOD0 bits and the TOA1 to TOD1 bits in TOCR decide the value of the FTIO pin, which is output until the first compare match occurs. Once a compare match occurs and this compare match changes the values of FTIOA0 to FTIOD0 and FTIOA1 to FTIOD1 output, the values of the FTIOA0 to FTIOD0 and FTIOA1 to FTIOD1 pin output and the values read from the TOA0 to TOD0 and TOA1 to TOD1 bits may differ. Moreover, when the writing to TOCR and the generation of the compare match A0 to D0 and A1 to D1 occur at the same timing, the writing to TOCR has the priority. Thus, output change due to the compare match is not reflected to the FTIOA0 to FTIOD0 and FTIOA1 to FTIOD1 pins. Therefore, when bit manipulation instruction is used to write to TOCR, the values of the FTIOA0 to FTIOD0 and FTIOA1 to FTIOD1 pin output may result in an unexpected result. When TOCR is to be written to while compare match is operating, stop the counter once before accessing to TOCR, read the port 6 state to reflect the values of FTIOA0 to FTIOD0 and FTIOA1 to FTIOD1 output, to TOA0 to TOD0 and TOA1 to TOD1, and then restart the counter. Figure 12.59 shows an example when the compare match and the bit manipulation instruction to TOCR occur at the same timing.

Section 13 Watchdog Timer

The watchdog timer is an 8-bit timer that can generate an internal reset signal for this LSI if a system crash prevents the CPU from writing to the timer counter, thus allowing it to overflow.

The block diagram of the watchdog timer is shown in figure 13.1.

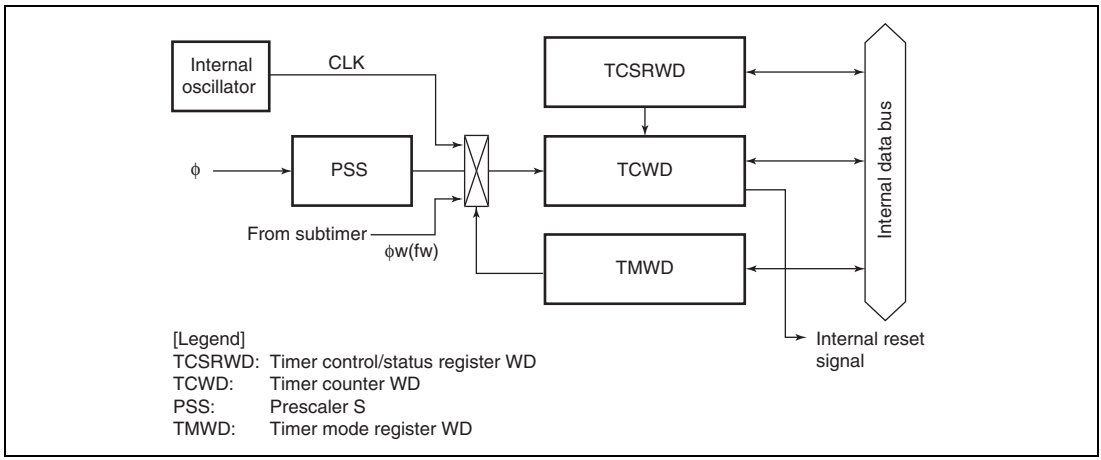

Figure 13.1 Block Diagram of Watchdog Timer

13.1 Features

- Selectable from nine counter input clocks.

  Eight internal clock sources (/64, /128, /256, /512, /1024, /2048, /4096, and /8192) or the internal oscillator (WDT and SBT) can be selected as the timer-counter clock. When the internal oscillator is selected, it can operate as the watchdog timer in any operating mode.
- Reset signal generated on counter overflow

  An overflow period of 1 to 256 times the selected clock can be set.

[Legend]
WDT: Watchdog timer
SBT: Subtimer

14.3.5 Serial Mode Register (SMR)

SMR is used to set the SCI3 s serial transfer format and select the baud rate generator clock source.

Bit	Bit Name	Initial Value	R/W	Description
7	COM	0	R/W	Communication Mode 0: Asynchronous mode 1: Clocked synchronous mode
6	CHR	0	R/W	Character Length (enabled only in asynchronous mode) 0: Selects 8 bits as the data length. 1: Selects 7 bits as the data length.
5	PE	0	R/W	Parity Enable (enabled only in asynchronous mode) When this bit is set to 1, the parity bit is added to transmit data before transmission, and the parity bit is checked in reception.
4	PM	0	R/W	Parity Mode (enabled only when the PE bit is 1 in asynchronous mode) 0: Selects even parity. 1: Selects odd parity.
3	STOP	0	R/W	Stop Bit Length (enabled only in asynchronous mode) Selects the stop bit length in transmission. 0: 1 stop bit 1: 2 stop bits For reception, only the first stop bit is checked, regardless of the value in the bit. If the second stop bit is 0, it is treated as the start bit of the next transmit character.
2	MP	0	R/W	Multiprocessor Mode When this bit is set to 1, the multiprocessor communication function is enabled. The PE bit and PM bit settings are invalid in multiprocessor mode. In clocked synchronous mode, clear this bit to 0.

Bit	Bit Name	Initial Value	R/W	Description
0	—	0	—	Reserved This bit is always read as 0. This bit is relevant to the receive-only Mailbox, and its value cannot be changed.

Note: * Only 1 can be written to clear the flag.

15.3.10 Abort Acknowledge Register (ABACK)

ABACK is a status flag that indicates successful cancellation of the Max transmit messages. If the transmit request cancellation is completed, bit in ABACK corresponding to the transmit message is set to 1.

Bit	Bit Name	Initial Value	R/W	Description
7 to 4	—	All 0	—	Reserved These bits are always read as 0.
3	MB3	0	R/(W)*	[Setting condition]
2	MB2	0	R/(W)*	When cancellation of the transmit message in the corresponding Mailbox has completed
1	MB1	0	R/(W)*	[Clearing condition] When 1 is written to these bits
0	—	0	—	Reserved This bit is always read as 0. This bit is relevant to the receive-only Mailbox, and its value cannot be changed.

Note: * Only 1 can be written to clear the flag.

15.5.2 Bit Timing

The bit rate and bit timing are set by the bit configuration register (BCR). The CAN controllers connected to the CAN bus should be set so that all of them have the same baud rate and same width. One bit time consists of a total settable Time Quantum (TQ).

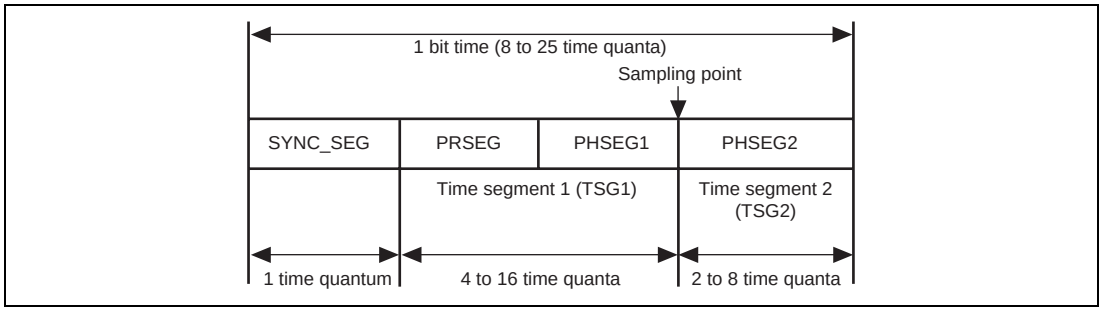

Figure 15.5 CAN Bit Configuration

The SYNC_SEG is a segment for establishing the synchronization of nodes on the CAN bus. Normal bit edge changes in this segment. The PRSEG is a segment for adjusting the physical delay between networks. The PHSEG1 is a buffer segment for adjusting positive phase drift. This segment is extended when re-synchronization is established. The PHSEG2 is a buffer segment for adjusting negative phase drift. This segment is shortened when re-synchronization is established.

The range of settable values in BCR (TSG1, TSG2, BRP, and SJW) is shown in table 15.2.

Table 15.2 Settable Values in BCR

Name	Abbreviation	Min. Value	Max. Value
Time segment 1	TSG1*[1]	3*[3]	15
Time segment 2	TSG2*[1]	1*[4]	7
Baud rate prescaler	BRP	1	63
Re-Synchronization Jump width	SJW*[2]	0	3

Notes: 1. The time quanta values for the TSEG1 and TSEG2 are as follows: TSG value + 1
2. In the CAN specifications, the Re-Synchronization Jump Width is stipulated as $4 \geq SJW \geq 1$. The value of SJW is given by adding 1 to the setting value of the bits SJW0 to SJW1 in BCR.
3. The minimum value of TSG1 is stipulated in the CAN specifications: TSG1 > TSG2
4. The minimum value of TSG2 is stipulated in the CAN specifications: TSG2 ≥ SJW