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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300H
Core Size	16-Bit
Speed	20MHz
Connectivity	CANbus, SCI, SSU
Peripherals	PWM, WDT
Number of I/O	45
Program Memory Size	56KB (56K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df36057fzjv

Table 7.3 System Clock Frequencies for which Automatic Adjustment of LSI Bit Rate is Possible

Host Bit Rate	System Clock Frequency Range of LSI
19,200 bps	16 to 20 MHz
9,600 bps	8 to 16 MHz
4,800 bps	4 to 16 MHz
2,400 bps	2 to 16 MHz

7.3.2 Programming/Erasing in User Program Mode

On-board programming/erasing of an individual flash memory block can also be performed in user program mode by branching to a user program/erase control program. The user must set branching conditions and provide on-board means of supplying programming data. The flash memory must contain the user program/erase control program or a program that provides the user program/erase control program from external memory. As the flash memory itself cannot be read during programming/erasing, transfer the user program/erase control program to on-chip RAM, as in boot mode. Figure 7.2 shows a sample procedure for programming/erasing in user program mode. Prepare a user program/erase control program in accordance with the description in section 7.4, Flash Memory Programming/Erasing.

9.4 Port 6

Port 6 is a general I/O port also functioning as a timer Z I/O pin. Each pin of the port 6 is shown in figure 9.4. The register setting of the timer Z has priority for functions of the pins for both uses.

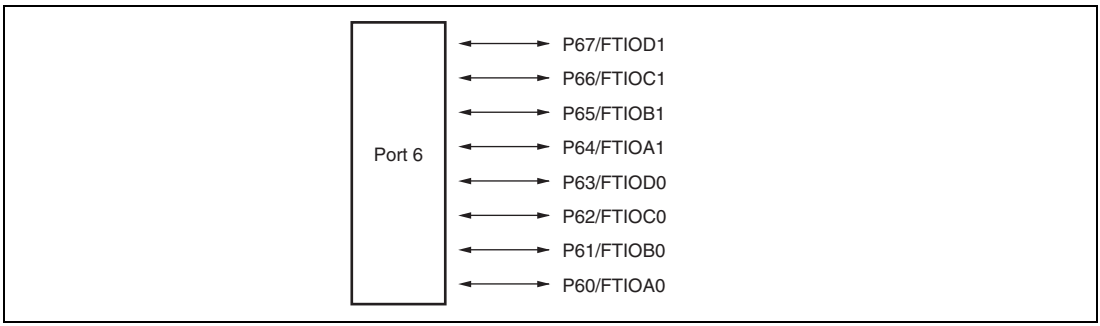


Figure 9.4 Port 6 Pin Configuration

Port 6 has the following registers.

- Port control register 6 (PCR6)
- Port data register 6 (PDR6)

9.4.1 Port Control Register 6 (PCR6)

PCR6 selects inputs/outputs in bit units for pins to be used as general I/O ports of port 6.

Bit	Bit Name	Initial Value	R/W	Description
7	PCR67	0	W	When each of the port 6 pins P67 to P60 functions as a general I/O port, setting a PCR6 bit to 1 makes the corresponding pin an output port, while clearing the bit to 0 makes the pin an input port.
6	PCR66	0	W	
5	PCR65	0	W	
4	PCR64	0	W	
3	PCR63	0	W	
2	PCR62	0	W	
1	PCR61	0	W	
0	PCR60	0	W	

9.7 Port 9

Port 9 is a general I/O port also functioning as a TinyCAN I/O pin and an SSU I/O pin. Each pin of the port 9 is shown in figure 9.7.

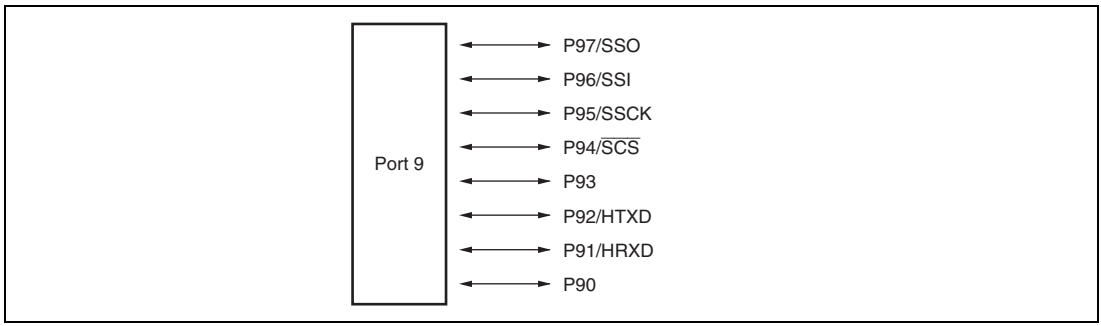


Figure 9.7 Port 9 Pin Configuration

Port 9 has the following registers.

- Port control register 9 (PCR9)
- Port data register 9 (PDR9)

9.7.1 Port Control Register 9 (PCR9)

PCR9 selects inputs/outputs in bit units for pins to be used as general I/O ports of port 9.

Bit	Bit Name	Initial Value	R/W	Description
7	PCR97	0	W	When each of the port 9 pins P97 to P90 functions as a general I/O port, setting a PCR9 bit to 1 makes the corresponding pin an output port, while clearing the bit to 0 makes the pin an input port.
6	PCR96	0	W	
5	PCR95	0	W	
4	PCR94	0	W	
3	PCR93	0	W	
2	PCR92	0	W	
1	PCR91	0	W	
0	PCR90	0	W	

Bit	Bit Name	Initial Value	R/W	Description
0	IMIEA	0	R/W	Input Capture/Compare Match Interrupt Enable A 0: Interrupt requests (IMIA) by IMFA flag are disabled 1: Interrupt requests (IMIA) by IMFA flag are enabled

12.3.13 PWM Mode Output Level Control Register (POCR)

POCR control the active level in PWM mode. Timer Z has two POCR registers, one for each channel.

Bit	Bit Name	Initial value	R/W	Description
7 to 3	—	All 1	—	Reserved These bits are always read as 1.
2	POLD	0	R/W	PWM Mode Output Level Control D 0: The output level of FTIOD is low-active 1: The output level of FTIOD is high-active
1	POLC	0	R/W	PWM Mode Output Level Control C 0: The output level of FTIOC is low-active 1: The output level of FTIOC is high-active
0	POLB	0	R/W	PWM Mode Output Level Control B 0: The output level of FTIOB is low-active 1: The output level of FTIOB is high-active

12.3.14 Interface with CPU

16-Bit Register: TCNT and GR are 16-bit registers. Reading/writing in a 16-bit unit is enabled but disabled in an 8-bit unit since the data bus with the CPU is 16-bit width. These registers must always be accessed in a 16-bit unit. Figure 12.5 shows an example of accessing the 16-bit registers.

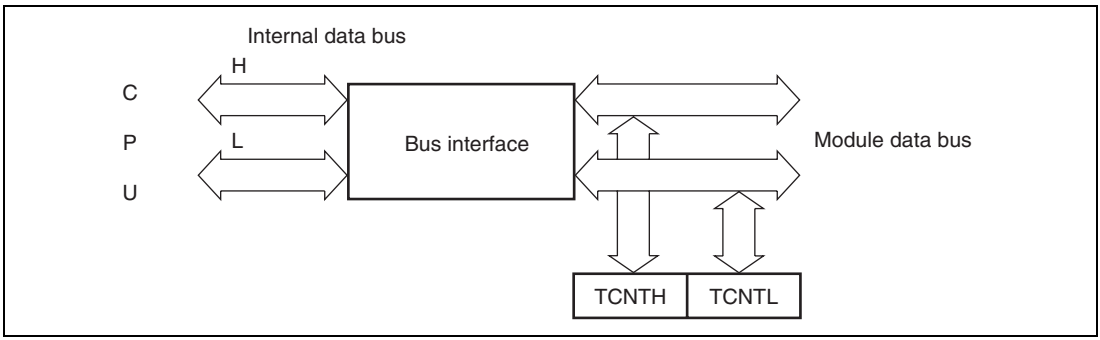


Figure 12.5 Accessing Operation of 16-Bit Register (between CPU and TCNT (16 Bits))

8-Bit Register: Registers other than TCNT and GR are 8-bit registers that are connected internally with the CPU in an 8-bit width. Figure 12.6 shows an example of accessing the 8-bit registers.

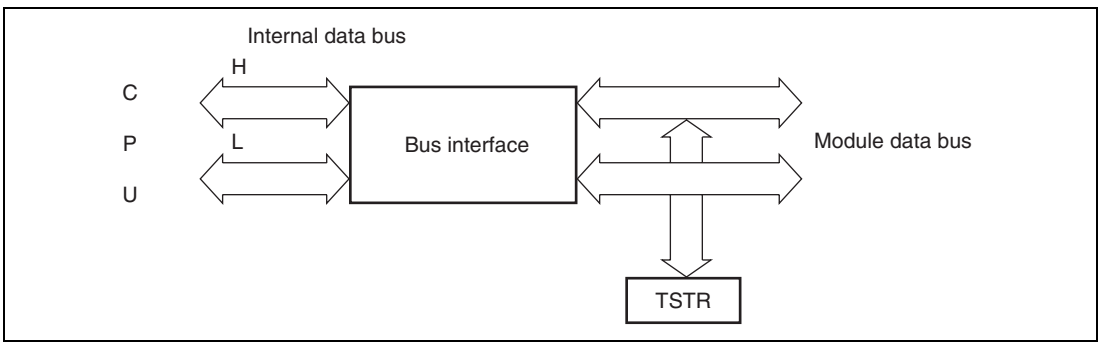
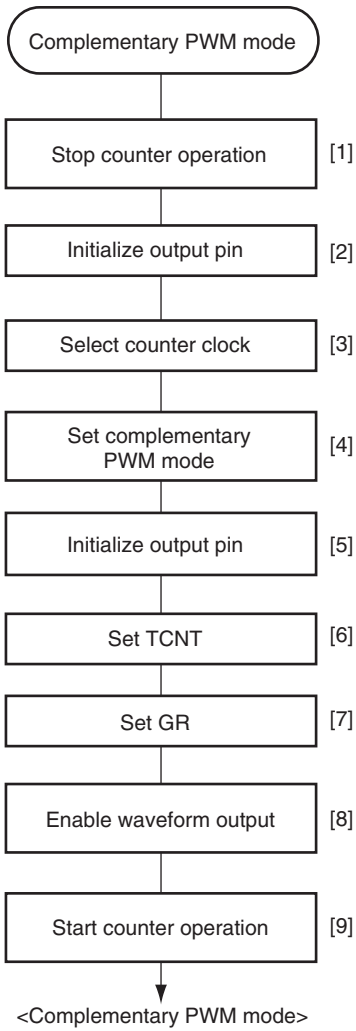


Figure 12.6 Accessing Operation of 8-Bit Register (between CPU and TSTR (8 Bits))

Table 12.7 Register Settings in Complementary PWM Mode

Register	Description
TCNT_0	Initial setting of non-overlapped periods (non-overlapped periods are differences with TCNT_1)
TCNT_1	Initial setting of H'0000
GRA_0	Sets (upper limit value – 1) of TCNT_0
GRB_0	Set a changing point of the PWM waveform output from pins FTIOB0 and FTIOD0.
GRA_1	Set a changing point of the PWM waveform output from pins FTIOA1 and FTIOC1.
GRB_1	Set a changing point of the PWM waveform output from pins FTIOB1 and FTIOD1.



[1] Clear bits STR0 and STR1 in TSTR to 0, and stop the counter operation of TCNT_0. Stop TCNT_0 and TCNT_1 and set complementary PWM mode.
[2] Write H'00 to TOCR.
[3] Use bits TPSC2 to TPSC0 in TCR to select the same counter clock for channels 0 and 1. When an external clock is selected, select the edge of the external clock by bits CKEG1 and CKEG0 in TCR. Do not use bits CCLR1 and CCLR0 in TCR to clear the counter.
[4] Use bits CMD1 and CMD0 in TFCR to set complementary PWM mode. FTIOB0 to FTIOD0 and FTIOA1 to FTIOD1 automatically become PWM output pins.
[5] Set H'00 to TOCR.
[6] TCNT_1 must be H'0000. Set a non-overlapped period to TCNT_0.
[7] GRA_0 is a cycle register. Set the cycle to GRA_0. Set the timing to change the PWM output waveform to GRB_0, GRA_1, and GRB_1. Note that the timing must be set within the range of compare match carried out for TCNT_0 and TCNT_1. For GR settings, see Setting GR Value in Complementary PWM Mode in section 12.4.7, Complementary PWM Mode.
[8] Use TOER to enable or disable the timer output.
[9] Set the STR0 and STR1 bits in TSTR to 1 to start the count operation.

Note: To re-enter complementary PWM mode, first, enter a mode other than the complementary PWM mode. After that, repeat the setting procedures from step [1].
For settings of waveform outputs with a duty cycle of 0% and 100%, see Examples of Complementary PWM Mode Operation and Setting GR Value in Complementary PWM Mode in section 12.4.7, Complementary PWM Mode.

Figure 12.29 Example of Complementary PWM Mode Setting Procedure

Table 14.5 Examples of BRR Settings for Various Bit Rates (Clocked Synchronous Mode) (1)

Bit Rate (bit/s)	Operating Frequency φ (MHz)									
	2		4		8		10		16	
	n	N	n	N	n	N	n	N	n	N
110	3	70	—	—	—	—	—	—		
250	2	124	2	249	3	124	—	—	3	249
500	1	249	2	124	2	249	—	—	3	124
1k	1	124	1	249	2	124	—	—	2	249
2.5k	0	199	1	99	1	199	1	249	2	99
5k	0	99	0	199	1	99	1	124	1	199
10k	0	49	0	99	0	199	0	249	1	99
25k	0	19	0	39	0	79	0	99	0	159
50k	0	9	0	19	0	39	0	49	0	79
100k	0	4	0	9	0	19	0	24	0	39
250k	0	1	0	3	0	7	0	9	0	15
500k	0	0*	0	1	0	3	0	4	0	7
1M			0	0*	0	1	—	—	0	3
2M					0	0*	—	—	0	1
2.5M							0	0*	—	—
4M									0	0*

[Legend]

Blank: No setting is available.

—: A setting is available but error occurs.

*: Continuous transfer is not possible.

14.4.4 Serial Data Reception

Figure 14.7 shows an example of operation for reception in asynchronous mode. In serial reception, the SCI3 operates as described below.

1. The SCI3 monitors the communication line. If a start bit is detected, the SCI3 performs internal synchronization, receives receive data in RSR, and checks the parity bit and stop bit.
2. If an overrun error occurs (when reception of the next data is completed while the RDRF flag is still set to 1), the OER bit in SSR is set to 1. If the RIE bit in SCR3 is set to 1 at this time, an ERI interrupt request is generated. Receive data is not transferred to RDR.
3. If a parity error is detected, the PER bit in SSR is set to 1 and receive data is transferred to RDR. If the RIE bit in SCR3 is set to 1 at this time, an ERI interrupt request is generated.
4. If a framing error is detected (when the stop bit is 0), the FER bit in SSR is set to 1 and receive data is transferred to RDR. If the RIE bit in SCR3 is set to 1 at this time, an ERI interrupt request is generated.
5. If reception is completed successfully, the RDRF bit in SSR is set to 1, and receive data is transferred to RDR. If the RIE bit in SCR3 is set to 1 at this time, an RXI interrupt request is generated. Continuous reception is possible because the RXI interrupt routine reads the receive data transferred to RDR before reception of the next receive data has been completed.

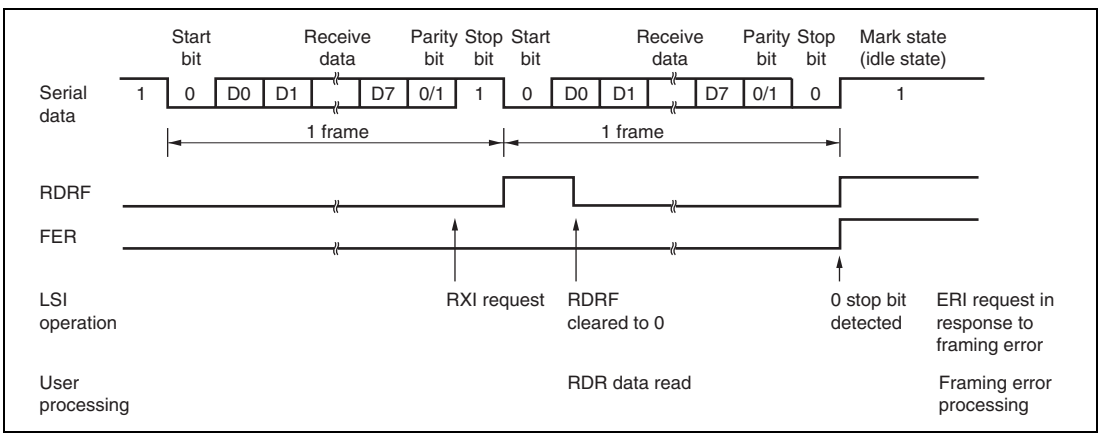


Figure 14.7 Example of SCI3 Reception in Asynchronous Mode (8-Bit Data, Parity, One Stop Bit)

Bit	Bit Name	Initial Value	R/W	Description
6	BOFIM	1	R/W	Bus Off Interrupt Mask Enables or disables a bus-off interrupt request. 0: The bus-off interrupt request is enabled 1: The bus-off interrupt request is disabled
5	EPIM	1	R/W	Error Passive Interrupt Mask Enables or disables an error passive interrupt request. 0: The error passive interrupt request is enabled 1: The error passive interrupt request is disabled
4	ROWIM	1	R/W	Receive Overload Warning Interrupt Mask Enables or disables an interrupt request for a receive overload warning. 0: The interrupt request for the receive overload warning is enabled 1: The interrupt request for the receive overload warning is disabled
3	TOWIM	1	R/W	Transmit Overload Warning Interrupt Mask Enables or disables an interrupt request for a transmit overload warning. 0: The interrupt request for the transmit overload warning is enabled 1: The interrupt request for the transmit overload warning is disabled
2	RFRIM	1	R/W	Remote Frame Request Interrupt Mask Enables or disables an interrupt request for a remote frame request. 0: The interrupt request for the remote frame request is enabled 1: The interrupt request for the remote frame request is disabled
1	DFRIM	1	R/W	Data Frame Receive Message Interrupt Mask Enables or disables an interrupt request for a data frame receive message. 0: The interrupt request for the data frame receive message is enabled 1: The interrupt request for the data frame receive message is disabled

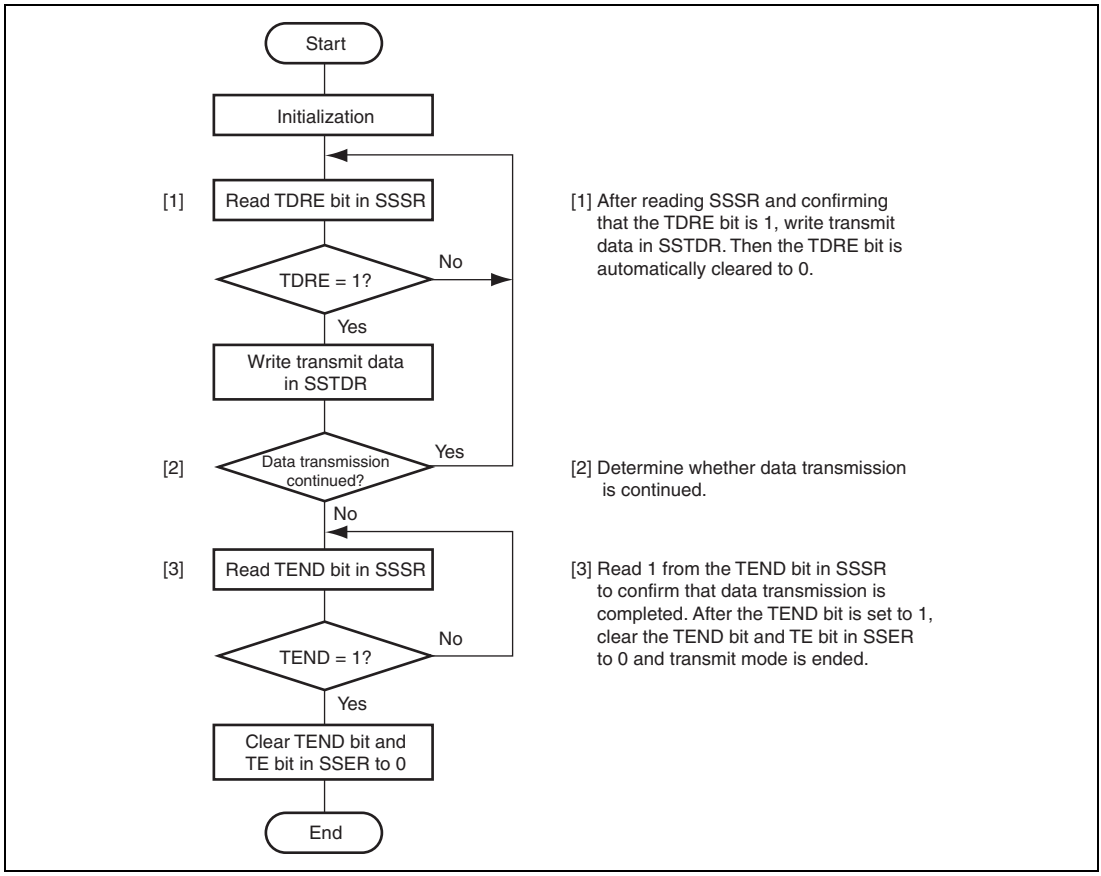


Figure 16.6 Sample Serial Transmission Flowchart

Table 22.13 DC Characteristics (2)

V_{CC} = 2.7 to 5.5 V, V_{SS} = 0.0 V, T_a = –20 to +75°C (regular specifications) or T_a = –40 to +85°C (wide-range specifications), unless otherwise indicated.

				Values			
Item	**Symbol**	**Applicable Pins**	**Test Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
Allowable output low current (per pin)	I_{OL}	Output pins except port 6	V_{CC} = 4.0 to 5.5 V	—	—	2.0	mA
		Port 6		—	—	20.0	
		Output pins except port 6		—	—	0.5	
		Port 6		—	—	10.0	
Allowable output low current (total)	ΣI_{OL}	Output pins except port 6	V_{CC} = 4.0 to 5.5 V	—	—	40.0	mA
		Port 6		—	—	80.0	
		Output pins except port 6		—	—	20.0	
		Port 6		—	—	40.0	
Allowable output high current (per pin)	$\lvert -I_{OH} \rvert$	All output pins	V_{CC} = 4.0 to 5.5 V	—	—	2.0	mA
				—	—	0.2	
Allowable output high current (total)	$\Sigma \lvert -I_{OH} \rvert$	All output pins	V_{CC} = 4.0 to 5.5 V	—	—	30.0	mA
				—	—	8.0	

22.4 Operation Timing

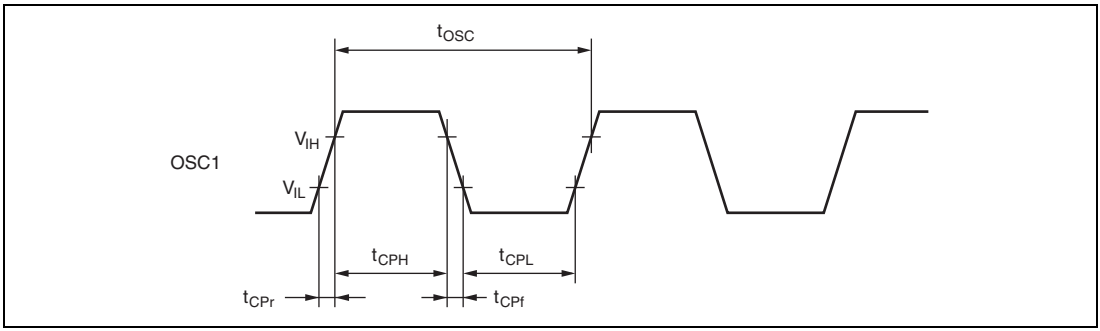


Figure 22.1 System Clock Input Timing

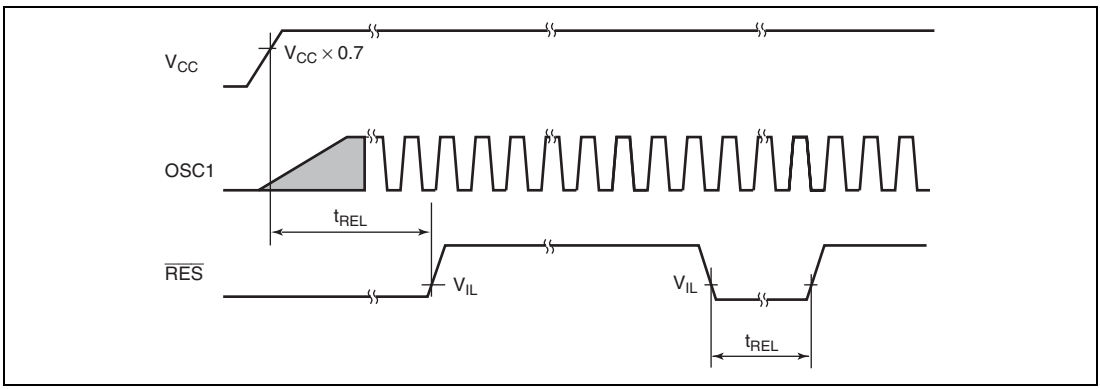


Figure 22.2 $\overline{\text{RES}}$ Low Width Timing

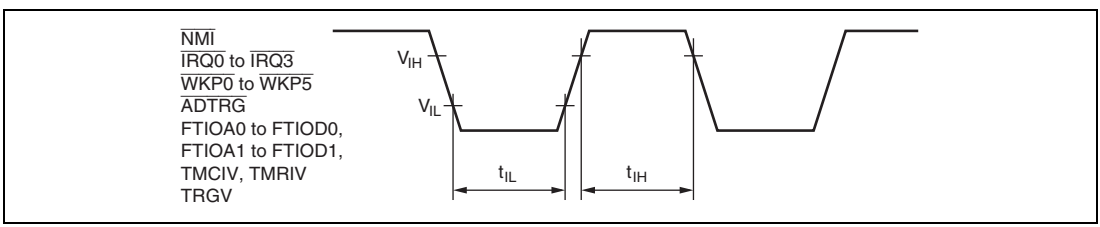


Figure 22.3 Input Timing

22.5 Output Load Condition

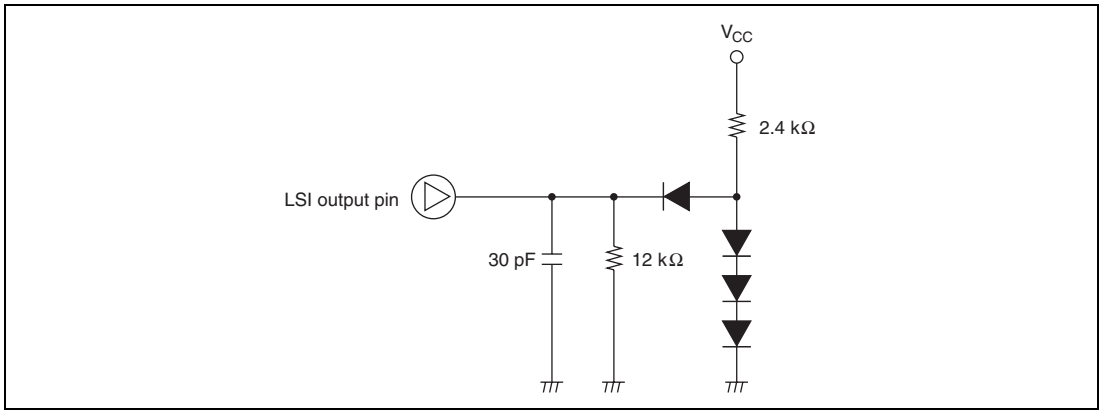


Figure 22.12 Output Load Circuit

Mnemonic		Operand Size	Addressing Mode and Instruction Length (bytes)									Operation	Condition Code						No. of States*1	
			#xx	Rn	@ERn	@(d, ERn)	@–ERn/@ERn+	@aa	@(d, PC)	@@aa	—		I	H	N	Z	V	C	Normal	Advanced
DEC	DEC.L #1, ERd	L		2								ERd32–1 → ERd32	—	—	↕	↕	↕	—	2	
	DEC.L #2, ERd	L		2								ERd32–2 → ERd32	—	—	↕	↕	↕	—	2	
DAS	DAS.Rd	B		2								Rd8 decimal adjust → Rd8	—	*	↕	↕	*	—	2	
MULXU	MULXU. B Rs, Rd	B		2								Rd8 × Rs8 → Rd16 (unsigned multiplication)	—	—	—	—	—	—	14	
	MULXU. W Rs, ERd	W		2								Rd16 × Rs16 → ERd32 (unsigned multiplication)	—	—	—	—	—	—	22	
MULXS	MULXS. B Rs, Rd	B		4								Rd8 × Rs8 → Rd16 (signed multiplication)	—	—	↕	↕	—	—	16	
	MULXS. W Rs, ERd	W		4								Rd16 × Rs16 → ERd32 (signed multiplication)	—	—	↕	↕	—	—	24	
DIVXU	DIVXU. B Rs, Rd	B		2								Rd16 ÷ Rs8 → Rd16 (RdH: remainder, RdL: quotient) (unsigned division)	—	—	(6)	(7)	—	—	14	
	DIVXU. W Rs, ERd	W		2								ERd32 ÷ Rs16 → ERd32 (Ed: remainder, Rd: quotient) (unsigned division)	—	—	(6)	(7)	—	—	22	
DIVXS	DIVXS. B Rs, Rd	B		4								Rd16 ÷ Rs8 → Rd16 (RdH: remainder, RdL: quotient) (signed division)	—	—	(8)	(7)	—	—	16	
	DIVXS. W Rs, ERd	W		4								ERd32 ÷ Rs16 → ERd32 (Ed: remainder, Rd: quotient) (signed division)	—	—	(8)	(7)	—	—	24	
CMP	CMP.B #xx:8, Rd	B	2									Rd8–#xx:8	—	↕	↕	↕	↕	↕	2	
	CMP.B Rs, Rd	B		2								Rd8–Rs8	—	↕	↕	↕	↕	↕	2	
	CMP.W #xx:16, Rd	W	4									Rd16–#xx:16	—	(1)	↕	↕	↕	↕	4	
	CMP.W Rs, Rd	W		2								Rd16–Rs16	—	(1)	↕	↕	↕	↕	2	
	CMP.L #xx:32, ERd	L	6									ERd32–#xx:32	—	(2)	↕	↕	↕	↕	4	
	CMP.L ERs, ERd	L		2								ERd32–ERs32	—	(2)	↕	↕	↕	↕	2	

Table A.2 Operation Code Map (2)

Instruction code:

1st byte	2nd byte
AH AL	BH BL

AH AL \ BH	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
01	MOV				LDC/STC				SLEEP				Table A.2 (3)	Table A.2 (3)		Table A.2 (3)
0A	INC												ADD			
0B	ADDS					INC		INC	ADDS					INC		INC
0F	DAA												MOV			
10	SHLL			SHLL					SHAL			SHAL				
11	SHLR			SHLR					SHAR			SHAR				
12	ROTXL			ROTXL					ROTL			ROTL				
13	ROTXR			ROTXR					ROTR			ROTR				
17	NOT			NOT		EXTU		EXTU	NEG			NEG		EXTS		EXTS
1A	DEC												SUB			
1B	SUBS					DEC		DEC	SUB					DEC		DEC
1F	DAS												CMP			
58	BRA	BRN	BHI	BLS	BCC	BCS	BNE	BEQ	BVC	BVS	BPL	BMI	BGE	BLT	BGT	BLE
79	MOV	ADD	CMP	SUB	OR	XOR	AND									
7A	MOV	ADD	CMP	SUB	OR	XOR	AND									

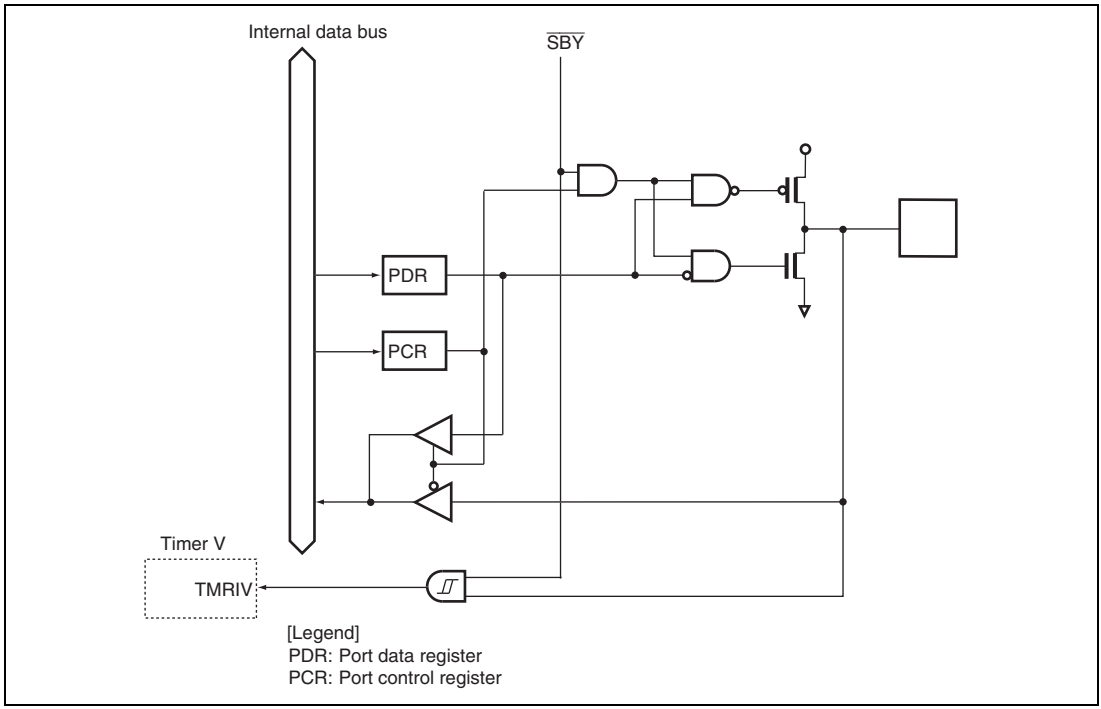


Figure B.15 Port 7 Block Diagram (P74)

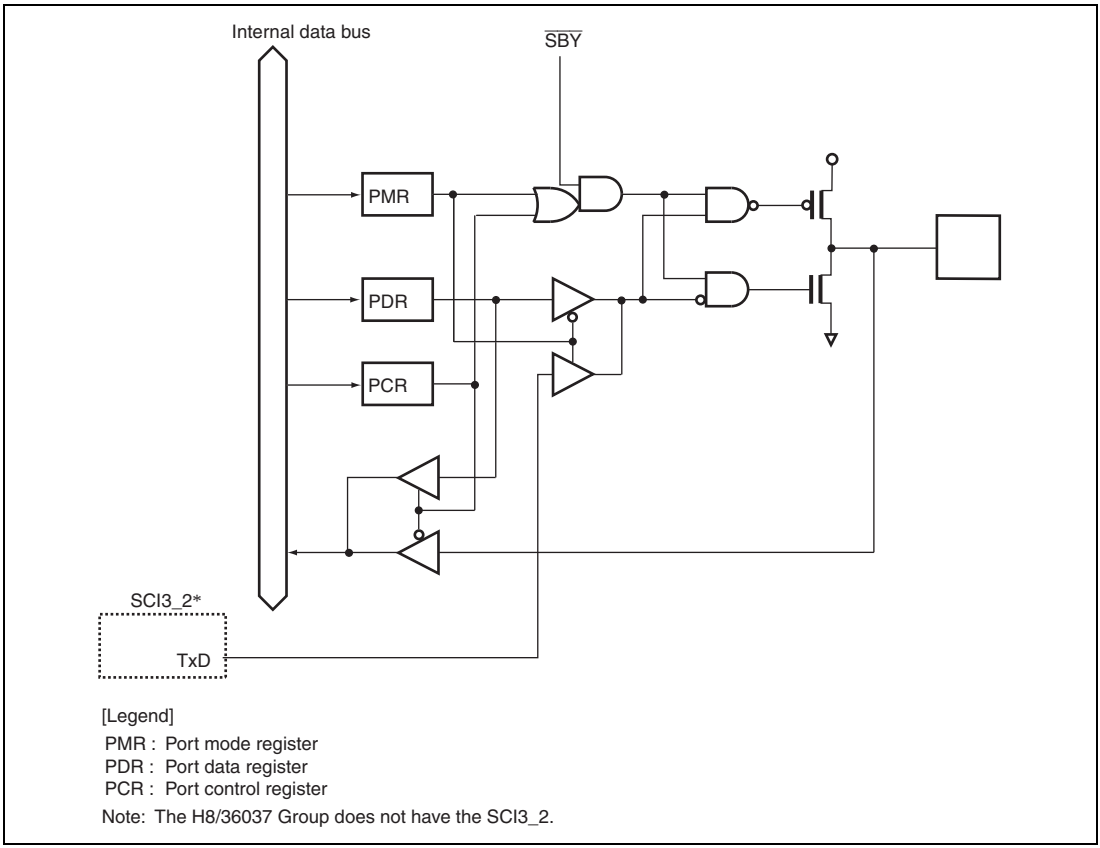


Figure B.16 Port 7 Block Diagram (P72)

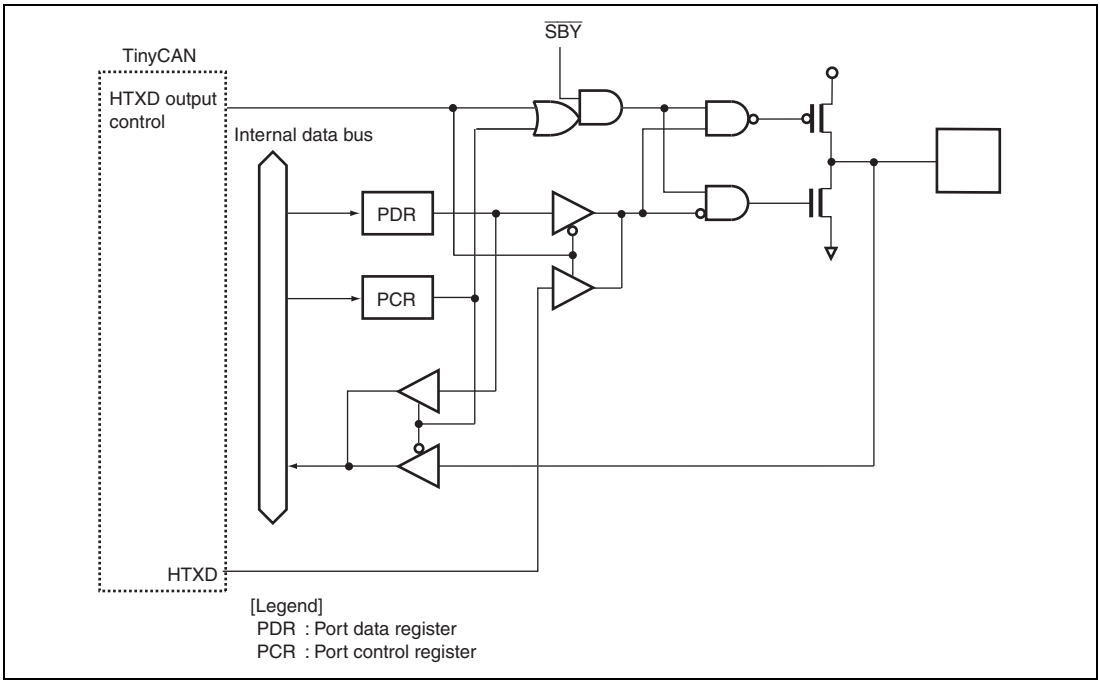


Figure B.20 Port 9 Block Diagram (P97)