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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300H
Core Size	16-Bit
Speed	20MHz
Connectivity	CANbus, SCI, SSU
Peripherals	LVD, POR, PWM, WDT
Number of I/O	45
Program Memory Size	56KB (56K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x10b SAR; D/A 1x10b
Oscillator Type	External, Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df36057fzv

Type	Symbol	Pin No. FP-64K FP-64A	I/O	Functions
Timer Z	FTIOA0	36	I/O	Output compare output/input capture input/external clock input pin.
	FTIOB0	34	I/O	Output compare output/input capture input/PWM output pin.
	FTIOC0	33	I/O	Output compare output/input capture input/PWM sync output pin (at a reset, complementary PWM mode).
	FTIOD0	32	I/O	Output compare output/input capture input/PWM output pin.
	FTIOA1	37	I/O	Output compare output/input capture input/PWM output pin (at a reset, complementary PWM mode).
	FTIOB1 to FTIOD1	38 to 40	I/O	Output compare output/input capture input/PWM output pins.
Serial communication interface (SCI)	TXD, TXD_2*	46, 50	Output	Transmit data output pins.
	RXD, RXD_2*	45, 49	Input	Receive data input pins.
	SCK3, SCK3_2*	44, 48	I/O	Clock I/O pins.
Controller area network for Tiny (TinyCAN)	HRXD	17	Input	Receive data input pin.
	HTXD	18	Output	Transmit data output pin.
Synchronous serial communication unit (SSU)	$\overline{\text{SCS}}$	58	I/O	Chip select I/O pin.
	SSCK	57	I/O	Clock I/O pin.
	SSI	55	I/O	Transmit/receive data I/O pin.
	SSO	56	I/O	Transmit/receive data I/O pin.
A/D converter	AN7 to AN0	2, 1, 59 to 64	Input	Analog input pins.
	$\overline{\text{ADTRG}}$	22	Input	Conversion start trigger input pin.

2.4.2 Basic Instruction Formats

H8/300H CPU instructions consist of 2-byte (1-word) units. An instruction consists of an operation field (op), a register field (r), an effective address extension (EA), and a condition field (cc).

Figure 2.7 shows examples of instruction formats.

- Operation Field

  Indicates the function of the instruction, the addressing mode, and the operation to be carried out on the operand. The operation field always includes the first four bits of the instruction. Some instructions have two operation fields.
- Register Field

  Specifies a general register. Address registers are specified by 3 bits, and data registers by 3 bits or 4 bits. Some instructions have two register fields. Some have no register field.
- Effective Address Extension

  8, 16, or 32 bits specifying immediate data, an absolute address, or a displacement. A24-bit address or displacement is treated as a 32-bit data in which the first 8 bits are 0 (H'00).
- Condition Field

  Specifies the branching condition of Bcc instructions.

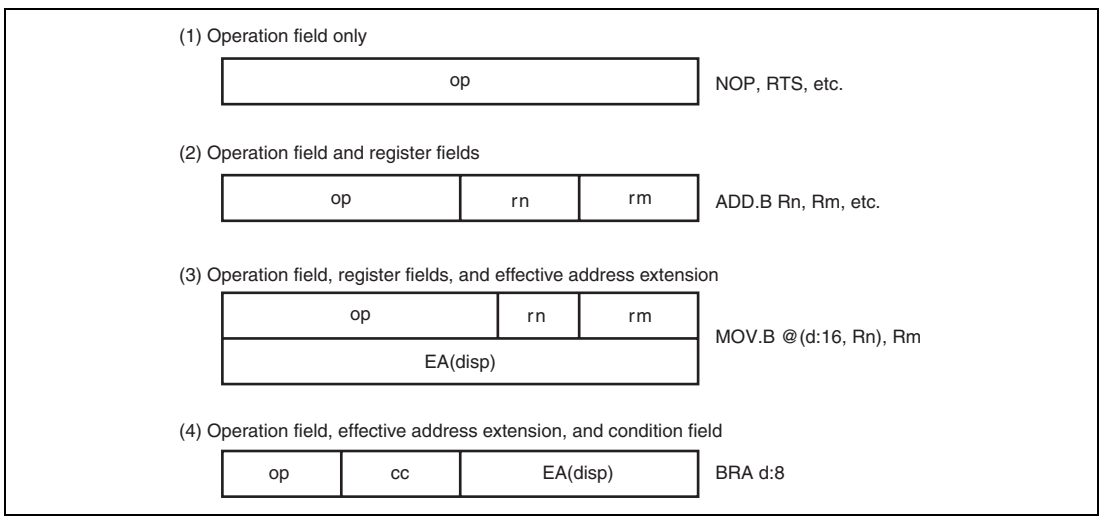


Figure 2.7 Instruction Formats

2.7 CPU States

There are four CPU states: the reset state, program execution state, program halt state, and exception-handling state. The program execution state includes active mode and subactive mode. For the program halt state, there are a sleep mode, standby mode, and sub-sleep mode. These states are shown in figure 2.11. Figure 2.12 shows the state transitions. For details on program execution state and program halt state, refer to section 6, Power-Down Modes. For details on exception processing, refer to section 3, Exception Handling.

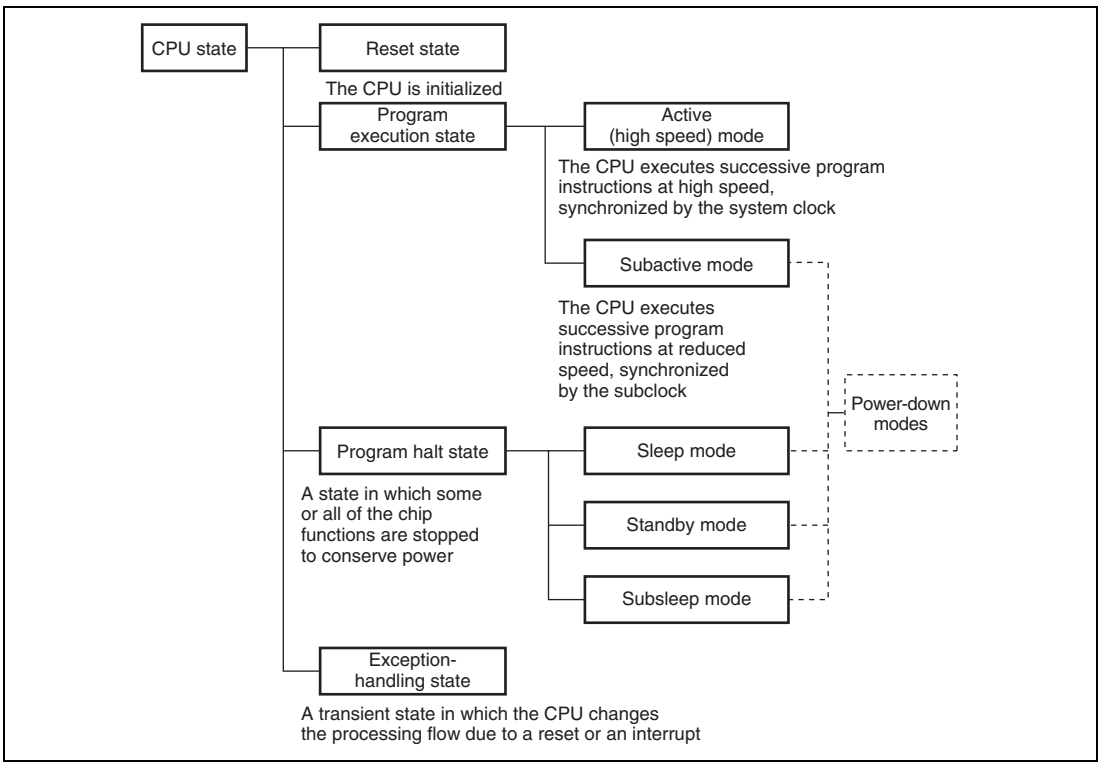


Figure 2.11 CPU Operation States

6.4.2 Direct Transition from Subactive Mode to Active Mode

The time from the start of SLEEP instruction execution to the end of interrupt exception handling (the direct transition time) is calculated by equation (2).

Direct transition time = {(number of SLEEP instruction execution states) + (number of internal processing states)} × (tsubcyc before transition) + {(waiting time set in bits STS2 to STS0) + (number of interrupt exception handling states)} × (tcyc after transition) (2)

Example:
Direct transition time = (2 + 1) × 8tw + (8192 + 14) × tosc = 24tw + 8206tosc
(when the CPU operating clock of $\phi_w/8 \rightarrow \phi_{osc}$ and a waiting time of 8192 states are selected)

[Legend]
tosc: OSC clock cycle time
tw: Watch clock cycle time
tcyc: System clock (ϕ) cycle time
tsubcyc: Subclock (ϕ_{SUB}) cycle time

6.5 Module Standby Function

The module-standby function can be set to any peripheral module. In module standby mode, the clock supply to modules stops to enter the power-down mode. Module standby mode enables each on-chip peripheral module to enter the standby state by setting a bit in TCMR, SSCRL, or MSTCR1 that corresponds to each module to 1 and cancels the standby state by clearing the bit to 0.

9.3.2 Port Control Register 5 (PCR5)

PCR5 selects inputs/outputs in bit units for pins to be used as general I/O ports of port 5.

Bit	Bit Name	Initial Value	R/W	Description
7	PCR57	0	W	When each of the port 5 pins P57 to P50 functions as a general I/O port, setting a PCR5 bit to 1 makes the corresponding pin an output port, while clearing the bit to 0 makes the pin an input port.
6	PCR56	0	W	
5	PCR55	0	W	
4	PCR54	0	W	
3	PCR53	0	W	
2	PCR52	0	W	
1	PCR51	0	W	
0	PCR50	0	W	

9.3.3 Port Data Register 5 (PDR5)

PDR5 is a general I/O port data register of port 5.

Bit	Bit Name	Initial Value	R/W	Description
7	P57	0	R/W	Stores output data for port 5 pins.
6	P56	0	R/W	If PDR5 is read while PCR5 bits are set to 1, the value stored in PDR5 are read. If PDR5 is read while PCR5 bits are cleared to 0, the pin states are read regardless of the value stored in PDR5.
5	P55	0	R/W	
4	P54	0	R/W	
3	P53	0	R/W	
2	P52	0	R/W	
1	P51	0	R/W	
0	P50	0	R/W	

9.4.2 Port Data Register 6 (PDR6)

PDR6 is a general I/O port data register of port 6.

Bit	Bit Name	Initial Value	R/W	Description
7	P67	0	R/W	Stores output data for port 6 pins.
6	P66	0	R/W	If PDR6 is read while PCR6 bits are set to 1, the value stored in PDR6 are read. If PDR6 is read while PCR6 bits are cleared to 0, the pin states are read regardless of the value stored in PDR6.
5	P65	0	R/W	
4	P64	0	R/W	
3	P63	0	R/W	
2	P62	0	R/W	
1	P61	0	R/W	
0	P60	0	R/W	

9.4.3 Pin Functions

The correspondence between the register specification and the port functions is shown below.

- P67/FTIOD1 pin

Register	TOER	TFCR	TPMR	TIORC1	PCR6	
Bit Name	ED1	CMD1, CMD0	PWMD1	IOD2 to IOD0	PCR67	Pin Function
Setting Value	1	00	0	000 or 1XX	0	P67 input/FTIOD1 input pin
					1	P67 output pin
	0	00	0	001 or 01X	X	FTIOD1 output pin
			1	XXX		
		Other than 00	X	XXX		

[Legend]

X: Don't care.

14.3.1 Receive Shift Register (RSR)

RSR is a shift register that is used to receive serial data input from the RXD pin and convert it into parallel data. When one frame of data has been received, it is transferred to RDR automatically. RSR cannot be directly accessed by the CPU.

14.3.2 Receive Data Register (RDR)

RDR is an 8-bit register that stores received data. When the SCI3 has received one frame of serial data, it transfers the received serial data from RSR to RDR, where it is stored. After this, RSR is receive-enabled. As RSR and RDR function as a double buffer in this way, continuous receive operations are possible. After confirming that the RDRF bit in SSR is set to 1, read RDR only once. RDR cannot be written to by the CPU. RDR is initialized to H'00.

14.3.3 Transmit Shift Register (TSR)

TSR is a shift register that transmits serial data. To perform serial data transmission, the SCI3 first transfers transmit data from TDR to TSR automatically, then sends the data that starts from the LSB to the TXD pin. TSR cannot be directly accessed by the CPU.

14.3.4 Transmit Data Register (TDR)

TDR is an 8-bit register that stores data for transmission. When the SCI3 detects that TSR is empty, it transfers the transmit data written in TDR to TSR and starts transmission. The double-buffered structure of TDR and TSR enables continuous serial transmission. If the next transmit data has already been written to TDR during transmission of one-frame data, the SCI3 transfers the written data to TSR to continue transmission. To achieve reliable serial transmission, write transmit data to TDR only once after confirming that the TDRE bit in SSR is set to 1. TDR is initialized to H'FF.

Bit	Bit Name	Initial Value	R/W	Description
0	—	0	—	Reserved This bit is always read as 0. This bit is relevant to the receive-only Mailbox, and its value cannot be changed.

Note: * Only 1 can be written to clear the flag.

15.3.10 Abort Acknowledge Register (ABACK)

ABACK is a status flag that indicates successful cancellation of Mailbox transmit messages. If the transmit request cancellation is completed, the bit in ABACK corresponding to the transmit message is set to 1.

Bit	Bit Name	Initial Value	R/W	Description
7 to 4	—	All 0	—	Reserved These bits are always read as 0.
3	MB3	0	R/(W)*	[Setting condition]
2	MB2	0	R/(W)*	When cancellation of the transmit message in the corresponding Mailbox has completed
1	MB1	0	R/(W)*	[Clearing condition] When 1 is written to these bits
0	—	0	—	Reserved This bit is always read as 0. This bit is relevant to the receive-only Mailbox, and its value cannot be changed.

Note: * Only 1 can be written to clear the flag.

- TCIRR1

Bit	Bit Name	Initial Value	R/W	Description
7 to 5	—	All 0	—	Reserved These bits are always read as 0.
4	WUPI	0	R/(W)*	Wakeup Interrupt Flag Status flag indicating detection of a dominant bit on the CAN bus while the LSI is in standby mode. This flag can be set to 1 only in standby mode. [Setting condition] When the falling edge of HRXD is detected in standby mode [Clearing condition] When 1 is written to this bit
3, 2	—	All 0	—	Reserved These bits are always read as 0.
1	OVRI	0	R	Unread Message Interrupt Flag Status flag indicating that a new message has been received regardless of existence of an unread message. The NMC bit in MCn0 (n = 0 to 3) will determine how to handle the newly received message: NMC = 1 selects overwrite and NMC = 0 selects overrun (ignore). [Setting condition] When a new message is received with the MBIMR corresponding to the receive message cleared to 0 and the corresponding bit in RXPR or RFPR set to 1 [Clearing condition] When all bits in UMSR are cleared to 0
0	EMPI	0	R	Mailbox Empty Interrupt Flag Status flag indicating that the next transmit message can be written to the Mailbox. [Setting condition] When TXPR is cleared to 0 by completion of transmission or completion of transmission cancellation [Clearing condition] When TXACK and ABACK is cleared to 0

Note: * Only 1 can be written to clear the flag.

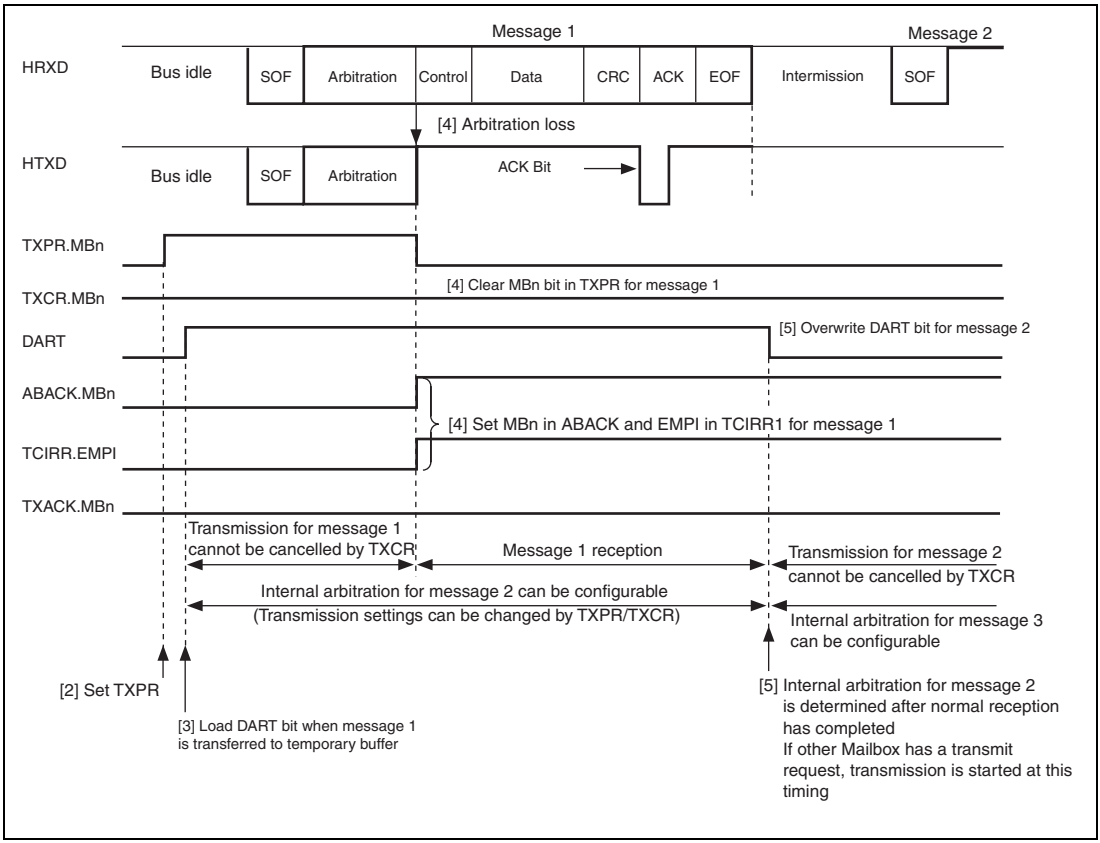


Figure 15.10 Internal Arbitration at Reception Caused by CAN Bus Arbitration Loss (DART = 1)

CAN Bus Error: Figures 15.11 to 15.13 show timings for internal arbitration caused by an error on the CAN bus. Procedure and operation are as follows.

1. Write data of a transmit message to MCn0, MCn4 to MCn7, and MDn0 to MDn7 [n = 1 to 3] before clearing the MBn bit in MBCR corresponding to the Mailbox of the transmit message to 0 (initial setting).
2. Set the MBn bit in TXPR to 1 (start condition issuance). Then, the start condition is generated.
3. The internal arbitration for message 1 is determined and the transmit message is transferred to the temporary buffer. After that, even if a transmit request cancellation is issued to the message being transmitted by the DART or MBn bit in TXCR, message 1 is transmitted continuously unless the TinyCAN detects an arbitration loss or error on the CAN bus.

Serial Data Reception: Figure 16.7 shows an example of the SSU operation for reception. In serial reception, the SSU operates as described below.

When the SSU is set as a master device, it outputs a synchronous clock and inputs data. When the SSU is set as a slave device, it inputs data in synchronized with the input clock. When the SSU is set as a master device, it outputs a receive clock and starts reception by performing dummy read on SSRDR.

After eight bits of data is received, the RDRF bit in SSSR is set to 1 and received data is stored in SSRDR. If the RIE bit in SSER is set to 1 at this time, a RXI is generated. If SSRDR is read, the RDRF bit is automatically cleared to 0.

When the SSU is set as a master device and reception is ended, received data is read after setting the RSSTP bit in SSER to 1. Then the SSU outputs eight bits of clocks and operation is stopped. After that, the RE and RSSTP bits are cleared to 0 and the last received data is read. Note that if SSRDR is read while the RE bit is set to 1, received clock is output again.

When the eighth clock rises while the RDRF bit is 1, the ORER bit in SSSR is set. Then an overrun error (OEI) is generated and operation is stopped. When the ORER bit in SSSR is set to 1, reception cannot be performed. Therefore confirm that the ORER bit is cleared to 0 before reception.

Figure 16.8 shows a sample flowchart for serial data reception.

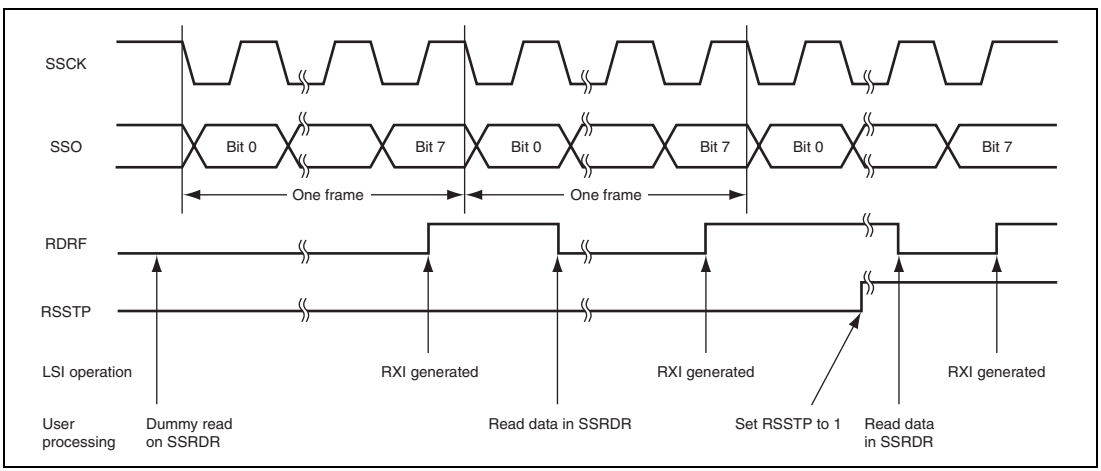


Figure 16.7 Example of Operation in Data Reception (MSS = 1)

- Subclock error

  In addition to the above rounding error, the subtimer may have a count error caused by time lag between the system clock and the on-chip oscillator. The example is shown below.

Table 17.1 Example of Subclock Error

Condition: System clock = 10 MHz, on-chip oscillator = 400 kHz, and subclock = 12 kHz

	Min.	Expected Value	Max.
Count Value n	**49**	**50**	**51**
Division ratio k	34	33	33
Rounding error of division ratio σ	—	+1.0 %	—
Rounding error of division ratio σ + count error	–2.0 %	—	+1.0 %

After deciding the division ratio according to formulas (1) to (3), the division ratio is configured in ROPCR. After ROPCR divides clocks of the on-chip oscillator, clocks for the subtimer counter, input clocks to the system, and input clocks to the watchdog timer are generated.

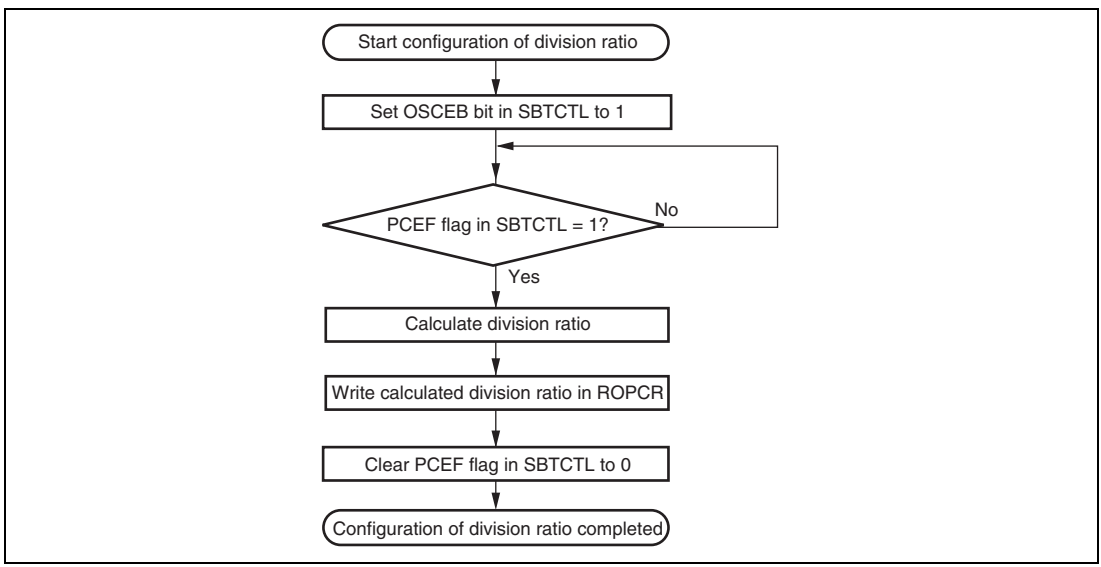


Figure 17.3 SBTPS Setting Flowchart

this time, the LVDUF bit in LVDSR is set to 1 and an IRQ0 interrupt request is simultaneously generated.

If the power supply voltage (Vcc) falls below Vreset1 (typ. = 2.3 V) voltage, the LVDR function is performed.

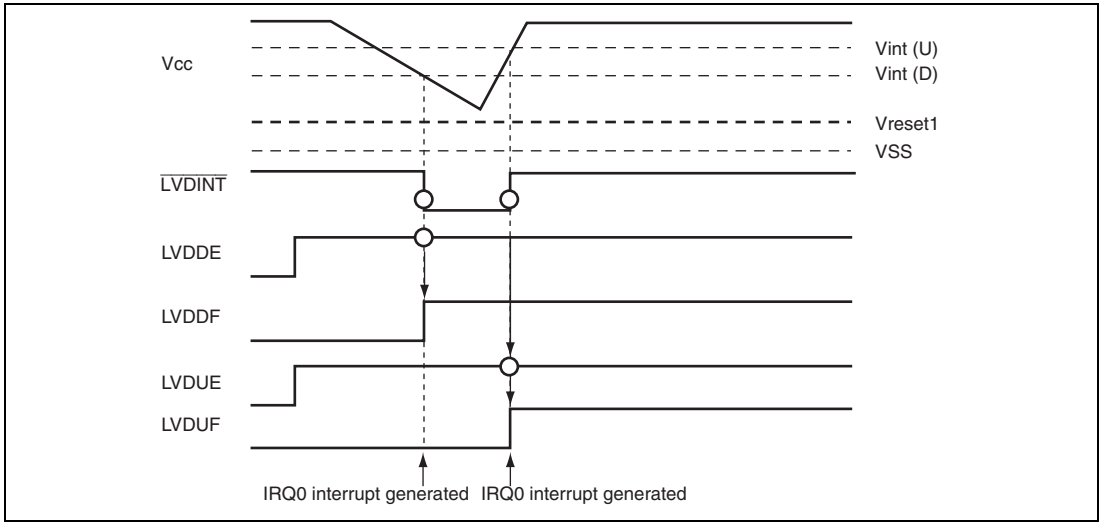


Figure 19.4 Operational Timing of LVDI Circuit

Register Name	Abbre-viation	Bit No	Address	Module Name	Data Bus Width	Access State
Message data 1 [4]	MD1[4]	8	H'F64C	TinyCAN	8	4
Message data 1 [5]	MD1[5]	8	H'F64D	TinyCAN	8	4
Message data 1 [6]	MD1[6]	8	H'F64E	TinyCAN	8	4
Message data 1 [7]	MD1[7]	8	H'F64F	TinyCAN	8	4
Message data 2 [0]	MD2[0]	8	H'F650	TinyCAN	8	4
Message data 2 [1]	MD2[1]	8	H'F651	TinyCAN	8	4
Message data 2 [2]	MD2[2]	8	H'F652	TinyCAN	8	4
Message data 2 [3]	MD2[3]	8	H'F653	TinyCAN	8	4
Message data 2 [4]	MD2[4]	8	H'F654	TinyCAN	8	4
Message data 2 [5]	MD2[5]	8	H'F655	TinyCAN	8	4
Message data 2 [6]	MD2[6]	8	H'F656	TinyCAN	8	4
Message data 2 [7]	MD2[7]	8	H'F657	TinyCAN	8	4
Message data 3 [0]	MD3[0]	8	H'F658	TinyCAN	8	4
Message data 3 [1]	MD3[1]	8	H'F659	TinyCAN	8	4
Message data 3 [2]	MD3[2]	8	H'F65A	TinyCAN	8	4
Message data 3 [3]	MD3[3]	8	H'F65B	TinyCAN	8	4
Message data 3 [4]	MD3[4]	8	H'F65C	TinyCAN	8	4
Message data 3 [5]	MD3[5]	8	H'F65D	TinyCAN	8	4
Message data 3 [6]	MD3[6]	8	H'F65E	TinyCAN	8	4
Message data 3 [7]	MD3[7]	8	H'F65F	TinyCAN	8	4
Local acceptance filter mask L01	LAFML01	8	H'F660	TinyCAN	8	4
Local acceptance filter mask L00	LAFML00	8	H'F661	TinyCAN	8	4
Local acceptance filter mask H01	LAFMH01	8	H'F662	TinyCAN	8	4
Local acceptance filter mask H00	LAFMH00	8	H'F663	TinyCAN	8	4
Local acceptance filter mask L11	LAFML11	8	H'F664	TinyCAN	8	4
Local acceptance filter mask L10	LAFML10	8	H'F665	TinyCAN	8	4
Local acceptance filter mask H11	LAFMH11	8	H'F666	TinyCAN	8	4
Local acceptance filter mask H10	LAFMH10	8	H'F667	TinyCAN	8	4
Local acceptance filter mask L21	LAFML21	8	H'F668	TinyCAN	8	4
Local acceptance filter mask L20	LAFML20	8	H'F669	TinyCAN	8	4

Register Abbreviation	Reset	Active	Sleep	Subactive	Subsleep	Standby	Module
MC1[4]	—	—	—	—	—	—	TinyCAN
MC1[5]	—	—	—	—	—	—	
MC2[1]	—	—	—	—	—	—	
MC2[2]	—	—	—	—	—	—	
MC2[3]	—	—	—	—	—	—	
MC2[4]	—	—	—	—	—	—	
MC2[5]	—	—	—	—	—	—	
MC3[1]	—	—	—	—	—	—	
MC3[2]	—	—	—	—	—	—	
MC3[3]	—	—	—	—	—	—	
MC3[4]	—	—	—	—	—	—	
MC3[5]	—	—	—	—	—	—	
MD0[1]	—	—	—	—	—	—	
MD0[2]	—	—	—	—	—	—	
MD0[3]	—	—	—	—	—	—	
MD0[4]	—	—	—	—	—	—	
MD0[5]	—	—	—	—	—	—	
MD0[6]	—	—	—	—	—	—	
MD0[7]	—	—	—	—	—	—	
MD0[8]	—	—	—	—	—	—	
MD1[1]	—	—	—	—	—	—	
MD1[2]	—	—	—	—	—	—	
MD1[3]	—	—	—	—	—	—	
MD1[4]	—	—	—	—	—	—	
MD1[5]	—	—	—	—	—	—	
MD1[6]	—	—	—	—	—	—	
MD1[7]	—	—	—	—	—	—	
MD1[8]	—	—	—	—	—	—	
MD2[1]	—	—	—	—	—	—	
MD2[2]	—	—	—	—	—	—	
MD2[3]	—	—	—	—	—	—	

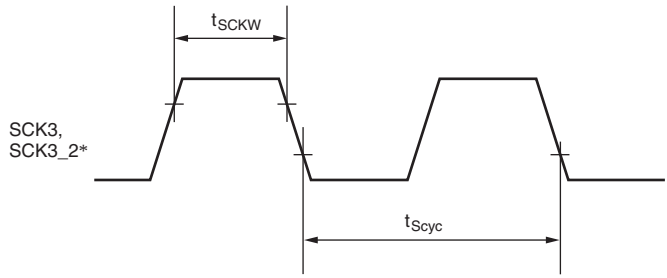
Register Abbreviation	Reset	Active	Sleep	Subactive	Subsleep	Standby	Module
TMDR	Initialized	—	—	—	—	—	Timer Z
TPMR	Initialized	—	—	—	—	—	
TFCR	Initialized	—	—	—	—	—	
TOER	Initialized	—	—	—	—	—	
TOCR	Initialized	—	—	—	—	—	
LVDCR	Initialized	—	—	—	—	—	LVDC (optional)*[1]
LVDSR	Initialized	—	—	—	—	—	
SMR_2	Initialized	—	—	Initialized	Initialized	Initialized	SCI3_2*[3]
BRR_2	Initialized	—	—	Initialized	Initialized	Initialized	
SCR3_2	Initialized	—	—	Initialized	Initialized	Initialized	
TDR_2	Initialized	—	—	Initialized	Initialized	Initialized	
SSR_2	Initialized	—	—	Initialized	Initialized	Initialized	
RDR_2	Initialized	—	—	Initialized	Initialized	Initialized	
TMB1	Initialized	—	—	—	—	—	Timer B1
TCB1	Initialized	—	—	—	—	—	
Tlb1	Initialized	—	—	—	—	—	
FLMCR1	Initialized	—	—	Initialized	Initialized	Initialized	ROM
FLMCR2	Initialized	—	—	—	—	—	
FLPWCR	Initialized	—	—	—	—	—	
EBR1	Initialized	—	—	Initialized	Initialized	Initialized	
FENR	Initialized	—	—	—	—	—	
TCRV0	Initialized	—	—	Initialized	Initialized	Initialized	Timer V
TCSRV	Initialized	—	—	Initialized	Initialized	Initialized	
TCORA	Initialized	—	—	Initialized	Initialized	Initialized	
TCORB	Initialized	—	—	Initialized	Initialized	Initialized	
TCNTV	Initialized	—	—	Initialized	Initialized	Initialized	
TCRV1	Initialized	—	—	Initialized	Initialized	Initialized	
SMR	Initialized	—	—	Initialized	Initialized	Initialized	SCI3
BRR	Initialized	—	—	Initialized	Initialized	Initialized	
SCR3	Initialized	—	—	Initialized	Initialized	Initialized	
TDR	Initialized	—	—	Initialized	Initialized	Initialized	

22.3.2 DC Characteristics

Table 22.12 DC Characteristics (1)

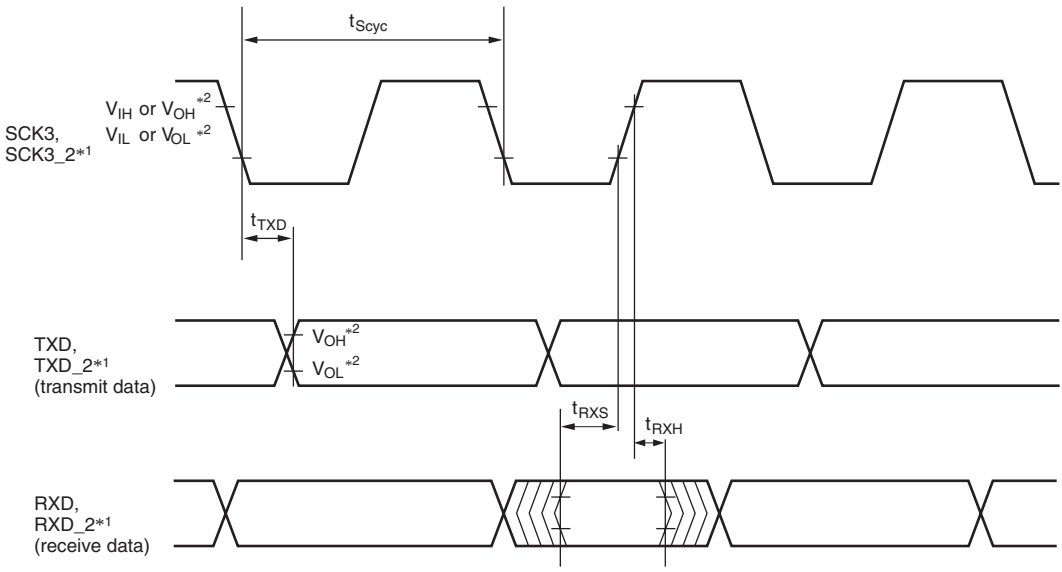
V_{CC} = 2.7 to 5.5 V, V_{SS} = 0.0 V, T_a = –20 to +75°C (regular specifications) or T_a = –40 to +85°C (wide-range specifications), unless otherwise indicated.

				Values				
Item	**Symbol**	**Applicable Pins**	**Test Condition**	**Min.**	**Typ.**	**Max.**	**Unit**	**Notes**
Input high voltage	V_{IH}	$\overline{RES}$, $\overline{NMI}$, $\overline{WKP0}$ to $\overline{WKP5}$, $\overline{IRQ0}$ to $\overline{IRQ3}$, $\overline{ADTRG}$,TMRIV, TMCIV, FTIOA0 to FTIOD0, FTIOA1 to FTIOD1, SCK3, SCK3_2*[1], $\overline{SCS}$, SSCK, TRGV, TMIB1	V_{cc} = 4.0 to 5.5 V	$V_{cc} \times 0.8$	—	V_{cc} + 0.3	V	
				$V_{cc} \times 0.9$	—	V_{cc} + 0.3		
		RXD, RXD_2*[1], SSI, SSO, HRXD, P10 to P12, P14 to P17, P20 to P24, P50 to P57, P60 to P67, P70 to P72, P74 to P76, P85 to P87 P90 to P97	V_{cc} = 4.0 to 5.5 V	$V_{cc} \times 0.7$	—	V_{cc} + 0.3	V	
				$V_{cc} \times 0.8$	—	V_{cc} + 0.3		
	V_{IH}	PB0 to PB7	V_{cc} = 4.0 to 5.5 V	$V_{cc} \times 0.7$	—	AV_{cc} + 0.3	V	
				$V_{cc} \times 0.8$	—	AV_{cc} + 0.3		
		OSC1	V_{cc} = 4.0 to 5.5 V	V_{cc} – 0.5	—	V_{cc} + 0.3	V	
				V_{cc} – 0.3	—	V_{cc} + 0.3		



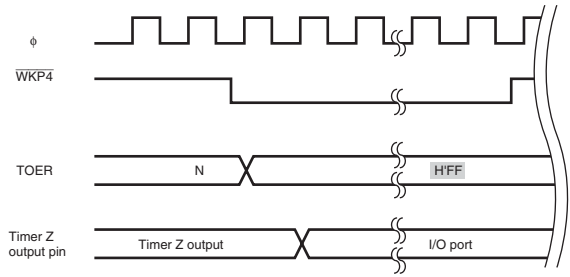
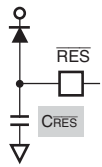
Note: * The H8/36037 Group does not have this pin.

Figure 22.4 SCK3 Input Clock Timing



Notes: 1. The H8/36037 Group does not have these pins.
2. Output timing reference levels
Output high: V_{OH}= 2.0 V
Output low: V_{OL}= 0.8 V
Load conditions are shown in figure 22.12.

Figure 22.5 SCI Input/Output Timing in Clocked Synchronous Mode

Item	Page	Revision (See Manual for Details)
Figure 12.45 Example of Output Disable Timing of Timer Z by External Trigger	230	Amended 
13.2.1 Timer Control/Status Register WD (TCSRWD)	246	Amended **Bit** / **Bit Name** / **Description** 4 / TCSRWE / Timer Control/Status Register WD Write Enable The WDON and WRST bits can be written when the TCSRWE bit is set to 1. When writing data to this bit, the value for bit 5 must be 0.
16.5 Usage Note	378	Added
18.3.1 A/D Data Registers A to D (ADDRA to ADDRD)	394	Amended …. The temporary register contents are transferred from the ADDR when the upper byte data is read. Therefore, byte access to ADDR should be done by reading the upper byte first then the lower one. Word access is also possible. ADDR is initialized to H'0000.
Figure 19.1 Block Diagram of Power-On Reset Circuit and Low-Voltage Detection Circuit	404	Amended 

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