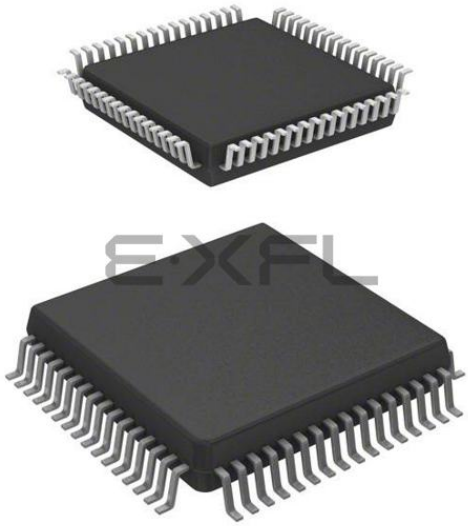

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300H
Core Size	16-Bit
Speed	20MHz
Connectivity	CANbus, SCI, SSU
Peripherals	LVD, POR, PWM, WDT
Number of I/O	45
Program Memory Size	56KB (56K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-BQFP
Supplier Device Package	64-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df36057ghjv

Contents

Section 15 Controller Area Network for Tiny (TinyCAN)

- Power-down state
  — Transition to power-down state by SLEEP instruction

2.1 Address Space and Memory Map

The address space of this LSI is 64 kbytes, which includes the program area and the data area.

Figures 2.1 show the memory map.

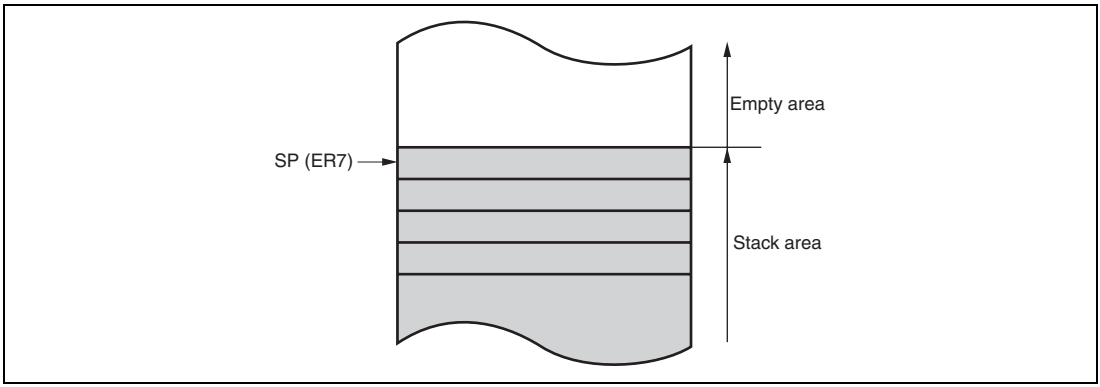


Figure 2.4 Relationship between Stack Pointer and Stack Area

2.2.2 Program Counter (PC)

This 24-bit counter indicates the address of the next instruction the CPU will execute. The length of all CPU instructions is 2 bytes (one word), so the least significant PC bit is ignored. (When an instruction is fetched, the least significant PC bit is regarded as 0). The PC is initialized when the start address is loaded by the vector address generated during reset exception-handling sequence.

2.2.3 Condition-Code Register (CCR)

This 8-bit register contains internal CPU status information, including an interrupt mask bit (I) and half-carry (H), negative (N), zero (Z), overflow (V), and carry (C) flags. The I bit is initialized to 1 by reset exception-handling sequence, but other bits are not initialized.

Some instructions leave flag bits unchanged. Operations can be performed on the CCR bits by the LDC, STC, ANDC, ORC, and XORC instructions. The N, Z, V, and C flags are used as branching conditions for conditional branch (Bcc) instructions.

For the action of each instruction on the flag bits, see appendix A.1, Instruction List.

9.6.2 Port Data Register 8 (PDR8)

PDR8 is a general I/O port data register of port 8.

Bit	Bit Name	Initial Value	R/W	Description
7	P87	0	R/W	PDR8 stores output data for port 8 pins.
6	P86	0	R/W	If PDR8 is read while PCR8 bits are set to 1, the value stored in PDR8 is read. If PDR8 is read while PCR8 bits are cleared to 0, the pin states are read regardless of the value stored in PDR8.
5	P85	0	R/W	
4 to 0	—	All 1	—	Reserved These bits are always read as 1.

9.6.3 Pin Functions

The correspondence between the register specification and the port functions is shown below.

- P87 pin

Register	PCR8	
Bit Name	PCR87	Pin Function
Setting Value	0	P87 input pin
	1	P87 output pin

- P86 pin

Register	PCR8	
Bit Name	PCR86	Pin Function
Setting Value	0	P86 input pin
	1	P86 output pin

- P85 pin

Register	PCR8	
Bit Name	PCR85	Pin Function
Setting Value	0	P85 input pin
	1	P85 output pin

11.2 Input/Output Pins

Table 11.1 shows the timer V pin configuration.

Table 11.1 Pin Configuration

Name	Abbreviation	I/O	Function
Timer V output	TMOV	Output	Timer V waveform output
Timer V clock input	TMCIV	Input	Clock input to TCNTV
Timer V reset input	TMRIV	Input	External input to reset TCNTV
Trigger input	TRGV	Input	Trigger input to initiate counting

11.3 Register Descriptions

The time V has the following registers.

- Timer counter V (TCNTV)
- Timer constant register A (TCORA)
- Timer constant register B (TCORB)
- Timer control register V0 (TCRV0)
- Timer control/status register V (TCSRV)
- Timer control register V1 (TCRV1)

11.3.1 Timer Counter V (TCNTV)

TCNTV is an 8-bit up-counter. The clock source is selected by bits CKS2 to CKS0 in timer control register V0 (TCRV0). The TCNTV value can be read and written by the CPU at any time. TCNTV can be cleared by an external reset input signal, or by compare match A or B. The clearing signal is selected by bits CCLR1 and CCLR0 in TCRV0.

When TCNTV overflows, OVF is set to 1 in timer control/status register V (TCSRV).

TCNTV is initialized to H'00.

12.2 Input/Output Pins

Table 12.2 summarizes the timer Z pins.

Table 12.2 Pin Configuration

Name	Abbreviation	I/O	Function
Input capture/output compare A0	FTIOA0	I/O	GRA_0 output compare output, GRA_0 input capture input, or external clock input (TCLK)
Input capture/output compare B0	FTIOB0	I/O	GRB_0 output compare output, GRB_0 input capture input, or PWM output
Input capture/output compare C0	FTIOC0	I/O	GRC_0 output compare output, GRC_0 input capture input, or PWM synchronous output (in reset synchronous PWM and complementary PWM modes)
Input capture/output compare D0	FTIOD0	I/O	GRD_0 output compare output, GRD_0 input capture input, or PWM output
Input capture/output compare A1	FTIOA1	I/O	GRA_1 output compare output, GRA_1 input capture input, or PWM output (in reset synchronous PWM and complementary PWM modes)
Input capture/output compare B1	FTIOB1	I/O	GRB_1 output compare output, GRB_1 input capture input, or PWM output
Input capture/output compare C1	FTIOC1	I/O	GRC_1 output compare output, GRC_1 input capture input, or PWM output
Input capture/output compare D1	FTIOD1	I/O	GRD_1 output compare output, GRD_1 input capture input, or PWM output

Figure 12.23 shows another example of operation in PWM mode. The output signals go to 0 and TCNT is reset at compare match A, and the output signals go to 1 at compare match B, C, and D (TOB, TOC, and TOD = 0, POLB, POLC, and POLD = 1).

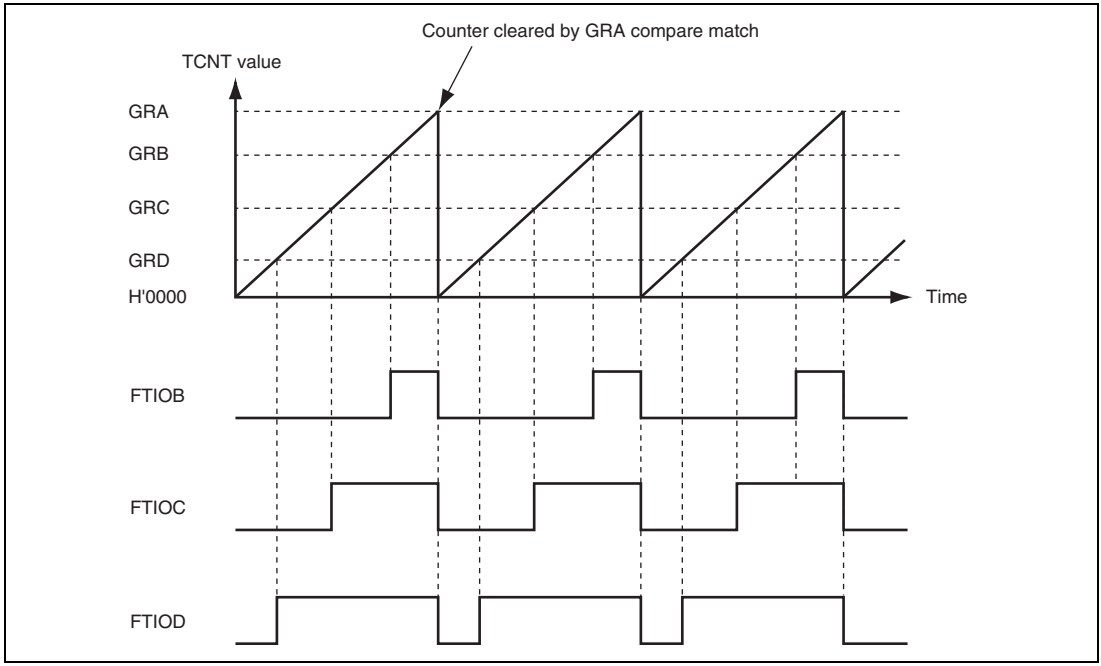


Figure 12.23 Example of PWM Mode Operation (2)

Figures 12.24 (when TOB, TOC, and TOD = 0, POLB, POLC, and POLD = 0) and 12.25 (when TOB, TOC, and TOD = 0, POLB, POLC, and POLD = 1) show examples of the output of PWM waveforms with duty cycles of 0% and 100% in PWM mode.

Figures 12.27 and 12.28 show examples of operation in reset synchronous PWM mode.

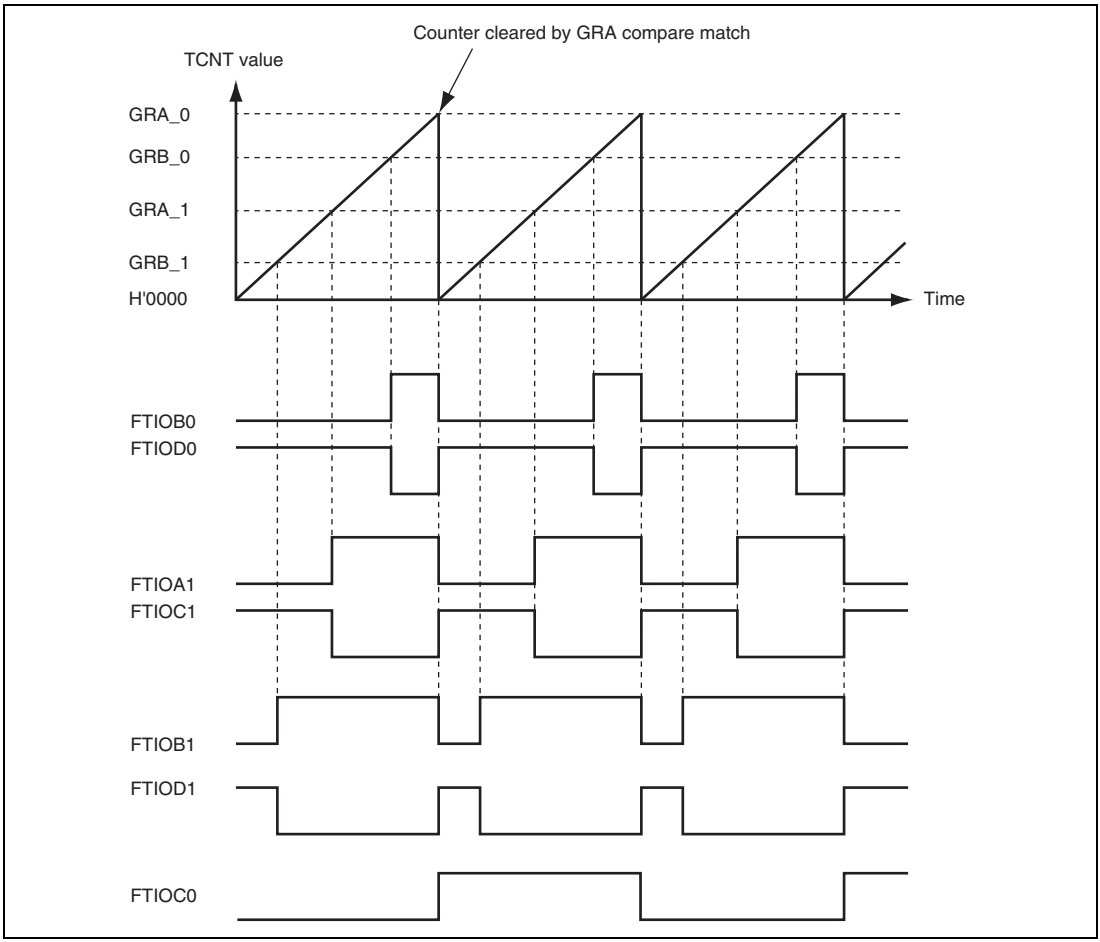


Figure 12.27 Example of Reset Synchronous PWM Mode Operation (OLS0 = OLS1 = 1)

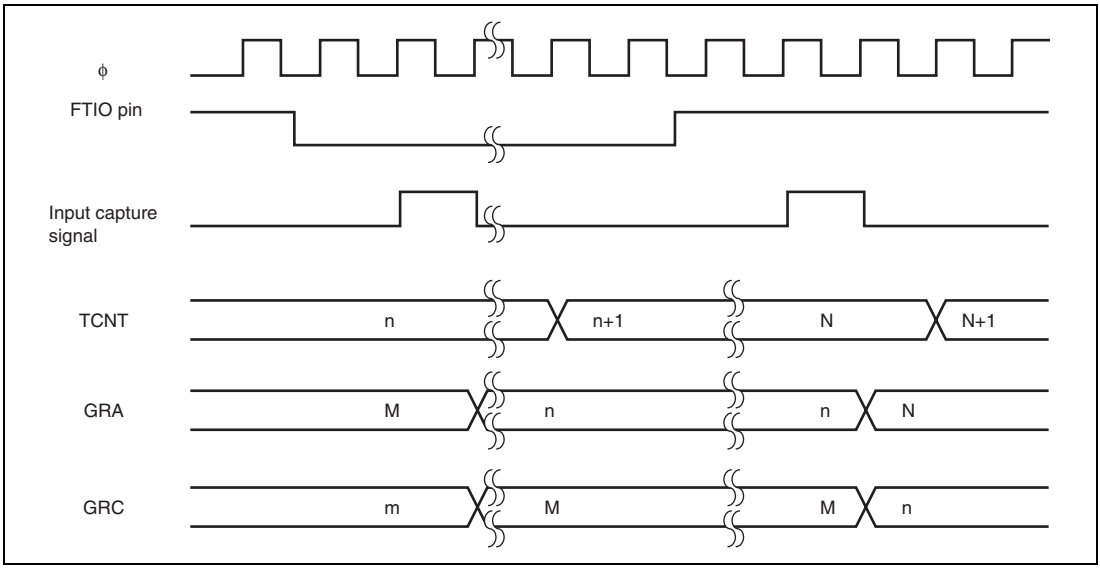
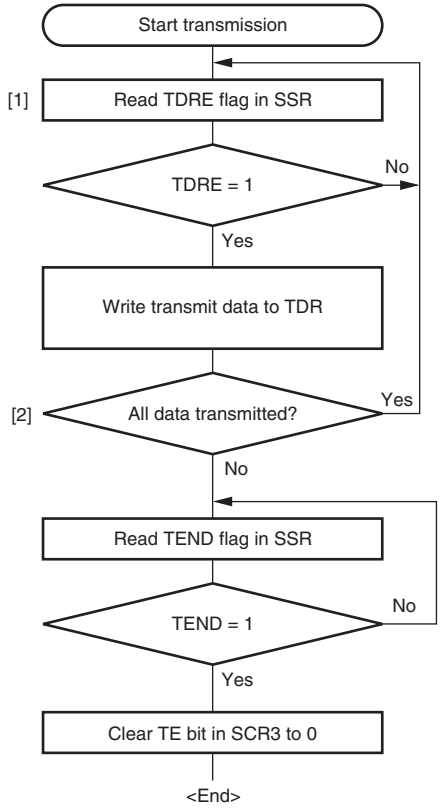


Figure 12.41 Input Capture Timing of Buffer Operation

	Operating Frequency ϕ (MHz)											
	8			9.8304			10			12		
Bit Rate (bit/s)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	141	0.03	2	174	–0.26	2	177	–0.25	2	212	0.03
150	2	103	0.14	2	127	0.00	2	129	0.14	2	155	0.14
300	1	207	0.14	1	255	0.00	2	64	0.14	2	77	0.14
600	1	103	0.14	1	127	0.00	1	129	0.14	1	155	0.14
1200	0	207	0.14	0	255	0.00	1	64	0.14	1	77	0.14
2400	0	103	0.14	0	127	0.00	0	129	0.14	0	155	0.14
4800	0	51	0.14	0	63	0.00	0	64	0.14	0	77	0.14
9600	0	25	0.14	0	31	0.00	0	32	–1.36	0	38	0.14
19200	0	12	0.14	0	15	0.00	0	15	1.73	0	19	–2.34
31250	0	7	0.00	0	9	–1.70	0	9	0.00	0	11	0.00
38400	0	6	-6.99	0	7	0.00	0	7	1.73	0	9	–2.34

[Legend]

—: A setting is available but error occurs.



[1] Read SSR and check that the TDRE flag is set to 1, then write transmit data to TDR. When data is written to TDR, the TDRE flag is automatically cleared to 0 and clocks are output to start the data transmission.

[2] To continue serial transmission, be sure to read 1 from the TDRE flag to confirm that writing is possible, then write data to TDR. When data is written to TDR, the TDRE flag is automatically cleared to 0.

Figure 14.11 Sample Serial Transmission Flowchart (Clocked Synchronous Mode)

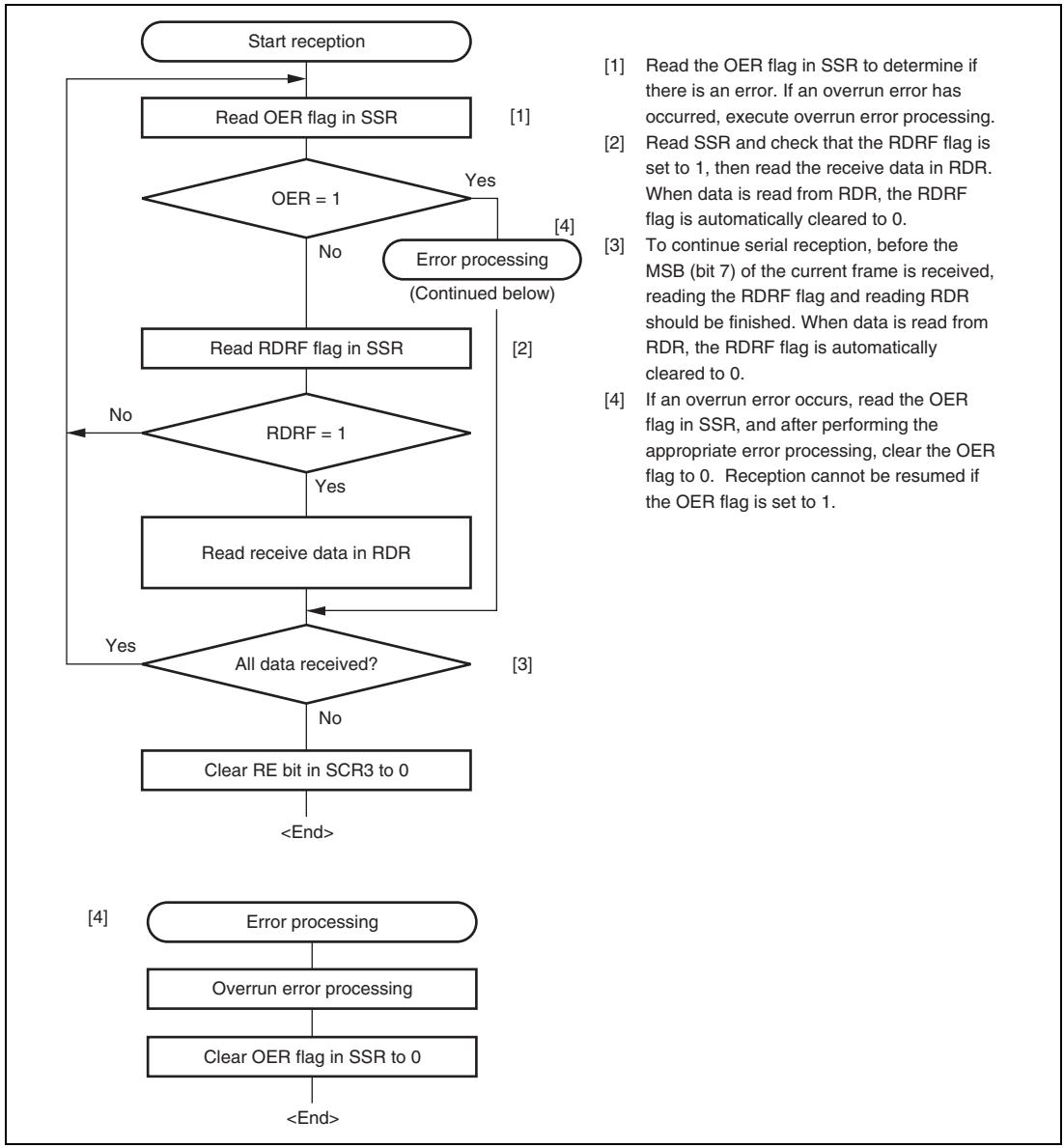


Figure 14.13 Sample Serial Reception Flowchart (Clocked Synchronous Mode)

19.3 Operation

19.3.1 Power-On Reset Circuit

Figure 19.2 shows the timing of the operation of the power-on reset circuit. As the power-supply voltage rises, the capacitor which is externally connected to the $\overline{\text{RES}}$ pin is gradually charged via the on-chip pull-up resistor (typ. 150 kΩ). Since the state of the $\overline{\text{RES}}$ pin is transmitted within the chip, the prescaler S and the entire chip are in their reset states. When the level on the $\overline{\text{RES}}$ pin reaches the specified value, the prescaler S is released from its reset state and it starts counting. The OVF signal is generated to release the internal reset signal after the prescaler S has counted 131,072 clock (ϕ) cycles. The noise canceler of approximately 500 ns is incorporated to prevent the incorrect operation of the chip by noise on the $\overline{\text{RES}}$ pin.

To achieve stable operation of this LSI, the power supply needs to rise to its full level and settles within the specified time. The maximum time required for the power supply to rise and settle after power has been supplied (t_{PWON}) is determined by the oscillation frequency (f_{OSC}) and capacitance which is connected to $\overline{\text{RES}}$ pin ($C_{\overline{\text{RES}}}$). If t_{PWON} means the time required to reach 90 % of power supply voltage, the power supply circuit should be designed to satisfy the following formula.

$$t_{PWON}\ (\text{ms}) \leq 90 \times C_{\overline{\text{RES}}}\ (\mu\text{F}) + 162/f_{OSC}\ (\text{MHz})$$

($t_{PWON} \leq 3000$ ms, $C_{\overline{\text{RES}}} \geq 0.22$ μF, and $f_{OSC} = 10$ in 2-MHz to 10-MHz operation)

Note that the power supply voltage (Vcc) must fall below Vpor = 100 mV and rise after charge on the $\overline{\text{RES}}$ pin is removed. To remove charge on the $\overline{\text{RES}}$ pin, it is recommended that the diode should be placed near Vcc. If the power supply voltage (Vcc) rises from the point above Vpor, a power-on reset may not occur.

22.5 Output Load Condition

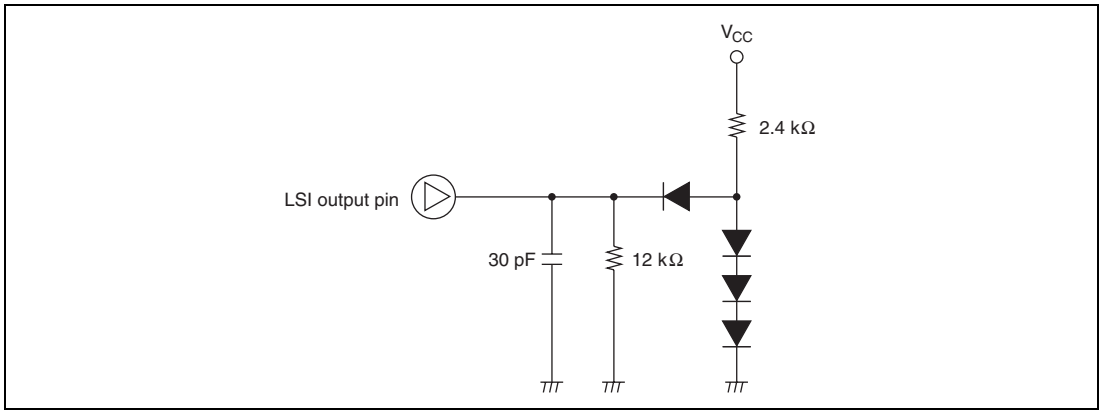


Figure 22.12 Output Load Circuit

Table A.3 Number of States Required for Execution

Execution Status (Instruction Cycle)		Access Location	
		On-Chip Memory	On-Chip Peripheral Module
Instruction fetch	S_I	2	—
Branch address read	S_J		
Stack operation	S_K		
Byte data access	S_L		2, 3, or 4*
Word data access	S_M		2, 3, or 4*
Internal operation	S_N	1	

Note: * Depends on which on-chip peripheral module is accessed. See section 21.1, Register Addresses (Address Order).

B.2 Port States in Each Operating State

Port	Reset	Sleep	Subsleep	Standby	Subactive	Active
P17 to P14, P12 to P10	High impedance	Retained	Retained	High impedance*	Functioning	Functioning
P24 to P20	High impedance	Retained	Retained	High impedance	Functioning	Functioning
P57 to P50	High impedance	Retained	Retained	High impedance*	Functioning	Functioning
P67 to P60	High impedance	Retained	Retained	High impedance	Functioning	Functioning
P76 to P74, P72 to P70	High impedance	Retained	Retained	High impedance	Functioning	Functioning
P87 to P85	High impedance	Retained	Retained	High impedance	Functioning	Functioning
P97 to P90	High impedance	Retained	Retained	High impedance	Functioning	Functioning
PB7 to PB0	High impedance	High impedance	High impedance	High impedance	High impedance	High impedance

Note: * High level output when the pull-up MOS is in on state.

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REJ09B0026-0400