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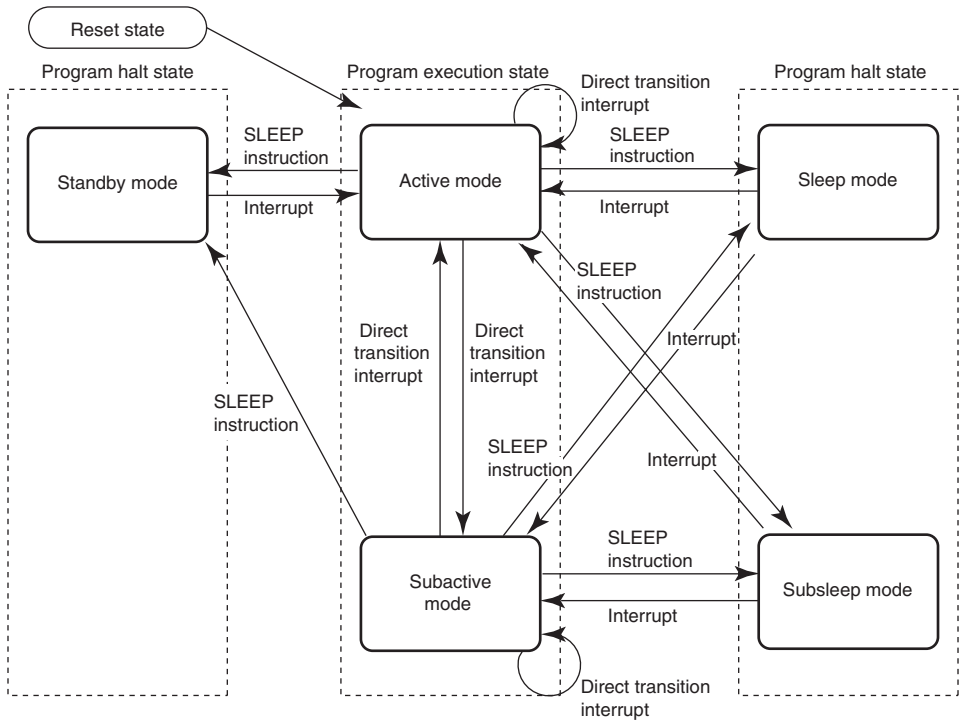
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300H
Core Size	16-Bit
Speed	20MHz
Connectivity	CANbus, SCI, SSU
Peripherals	LVD, POR, PWM, WDT
Number of I/O	45
Program Memory Size	56KB (56K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x10b SAR; D/A 1x10b
Oscillator Type	External, Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	64-BQFP
Supplier Device Package	64-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df36057ghv

6.2 Mode Transitions and States of LSI

Figure 6.1 shows the possible transitions among these operating modes. A transition is made from the program execution state to the program halt state by executing a SLEEP instruction. Interrupts allow for returning from the program halt state to the program execution state. A direct transition between active mode and subactive mode, which are both program execution states, can be made without halting the program. The operating frequency can also be changed in the same modes by making a transition directly from active mode to active mode, and from subactive mode to subactive mode. $\overline{\text{RES}}$ input enables transitions from a mode to the reset state. Table 6.2 shows the transition conditions of each mode after the SLEEP instruction is executed and a mode to return by an interrupt. Table 6.3 shows the internal states of the LSI in each mode.



Notes: 1. To make a transition to another mode by an interrupt, make sure interrupt handling is after the interrupt is accepted.
2. Details on the mode transition conditions are given in table 6.2.

Figure 6.1 Mode Transition Diagram

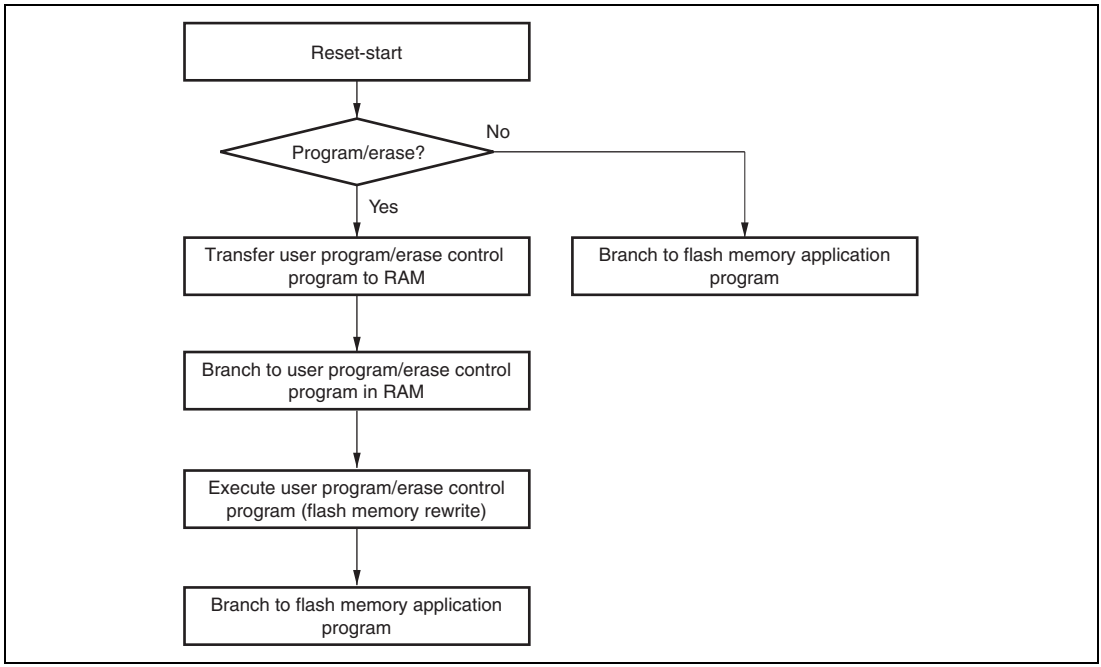


Figure 7.2 Programming/Erasing Flowchart Example in User Program Mode

Table 7.4 Reprogram Data Computation Table

Program Data	Verify Data	Reprogram Data	Comments
0	0	1	Programming completed
0	1	0	Reprogram bit
1	0	1	—
1	1	1	Remains in erased state

Table 7.5 Additional-Program Data Computation Table

Reprogram Data	Verify Data	Additional-Program Data	Comments
0	0	0	Additional-program bit
0	1	1	No additional programming
1	0	1	No additional programming
1	1	1	No additional programming

Table 7.6 Programming Time

n (Number of Writes)	Programming Time	In Additional Programming	Comments
1 to 6	30	10	
7 to 1,000	200	—	

Note: Time shown in μs.

- P16/$\overline{\text{IRQ2}}$ pin

Register	PMR1	PCR1	
Bit Name	**IRQ2**	**PCR16**	**Pin Function**
Setting value	0	0	P16 input pin
		1	P16 output pin
	1	X	$\overline{\text{IRQ2}}$ input pin

[Legend]
X: Don't care.

- P15/$\overline{\text{IRQ1}}$/TMIB1 pin

Register	PMR1	PCR1	
Bit Name	**IRQ1**	**PCR15**	**Pin Function**
Setting value	0	0	P15 input pin
		1	P15 output pin
	1	X	$\overline{\text{IRQ1}}$ input/TMIB1 input pin

[Legend]
X: Don't care.

- P14/$\overline{\text{IRQ0}}$ pin

Register	PMR1	PCR1	
Bit Name	**IRQ0**	**PCR14**	**Pin Function**
Setting value	0	0	P14 input pin
		1	P14 output pin
	1	X	$\overline{\text{IRQ0}}$ input pin

[Legend]
X: Don't care.

- P12 pin

Register	PCR1	
Bit Name	**PCR12**	**Pin Function**
Setting value	0	P12 input pin
	1	P12 output pin

10.2 Input/Output Pin

Table 10.1 shows the timer B1 pin configuration.

Table 10.1 Pin Configuration

Name	Abbreviation	I/O	Function
Timer B1 event input	TMIB1	Input	Event input to TCB1

10.5 Timer B1 Operating Modes

Table 10.2 shows the timer B1 operating modes.

Table 10.2 Timer B1 Operating Modes

Operating Mode		Reset	Active	Sleep	Subactive	Subsleep	Standby
TCB1	Interval	Reset	Functions	Functions	Halted	Halted	Halted
	Auto-reload	Reset	Functions	Functions	Halted	Halted	Halted
TMB1		Reset	Functions	Retained	Retained	Retained	Retained

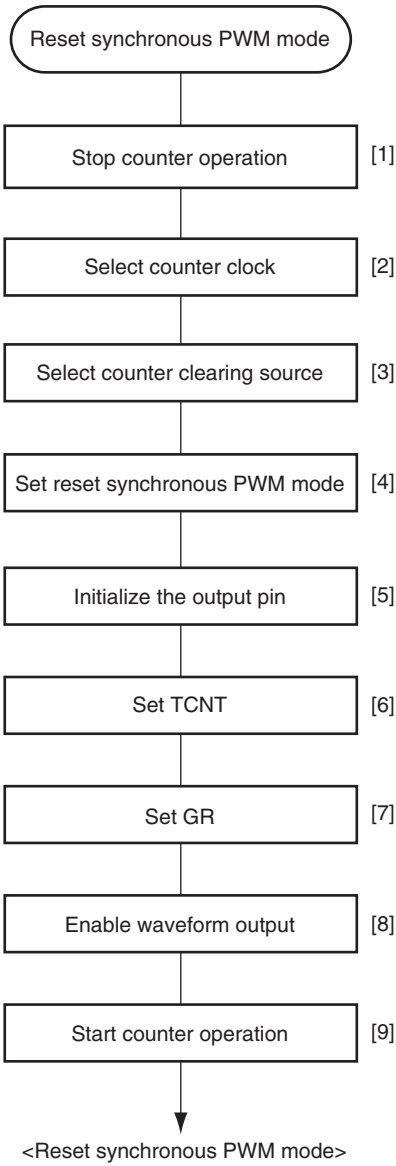
Bit	Bit Name	Initial Value	R/W	Description
1	OS1	0	R/W	Output Select 1 and 0
0	OS0	0	R/W	These bits select an output method for the TMOV pin by the compare match of TCORA and TCNTV. 00: No change 01: 0 output 10: 1 output 11: Output toggles

OS3 and OS2 select the output level for compare match B. OS1 and OS0 select the output level for compare match A. The two output levels can be controlled independently. After a reset, the timer output is 0 until the first compare match.

11.3.5 Timer Control Register V1 (TCRV1)

TCRV1 selects the edge at the TRGV pin, enables TRGV input, and selects the clock input to TCNTV.

Bit	Bit Name	Initial Value	R/W	Description
7 to 5	—	All 1	—	Reserved These bits are always read as 1.
4	TVEG1	0	R/W	TRGV Input Edge Select
3	TVEG0	0	R/W	These bits select the TRGV input edge. 00: TRGV trigger input is prohibited 01: Rising edge is selected 10: Falling edge is selected 11: Rising and falling edges are both selected
2	TRGE	0	R/W	TCNT starts counting up by the input of the edge which is selected by TVEG1 and TVEG0. 0: Disables starting counting-up TCNTV by the input of the TRGV pin and halting counting-up TCNTV when TCNTV is cleared by a compare match. 1: Enables starting counting-up TCNTV by the input of the TRGV pin and halting counting-up TCNTV when TCNTV is cleared by a compare match.



[1] Clear bit STR0 in TSTR to 0 and stop the counter operation of TCNT_0. Set reset synchronous PWM mode after TCNT_0 stops.
[2] Select the counter clock with bits TPSC2 to TOSC0 in TCR. When an external clock is selected, select the external clock edge with bits CKEG1 and CKEG0 in TCR.
[3] Use bits CCLR1 and CCLR0 in TCR to select counter clearing source GRA_0.
[4] Select the reset synchronous PWM mode with bits CMD1 and CMD0 in TFCR. FTIOB0 to FTIOD0 and FTIOA1 to FTIOD1 become PWM output pins automatically.
[5] Set H'00 to TOCR.
[6] Set TCNT_0 as H'0000. TCNT1 does not need to be set.
[7] GRA_0 is a cycle register. Set a cycle for GRA_0. Set the changing point timing of the PWM output waveform for GRB_0, GRA_1, and GRB_1.
[8] Enable or disable the timer output by TOER.
[9] Set the STR bit in TSTR to 1 and start the counter operation.

Figure 12.26 Example of Reset Synchronous PWM Mode Setting Procedure

Canceling Procedure of Complementary PWM Mode: Figure 12.30 shows the complementary PWM mode canceling procedure.

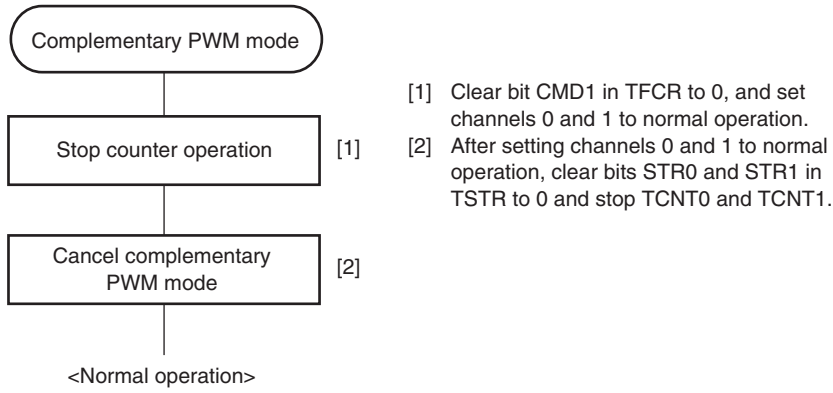


Figure 12.30 Canceling Procedure of Complementary PWM Mode

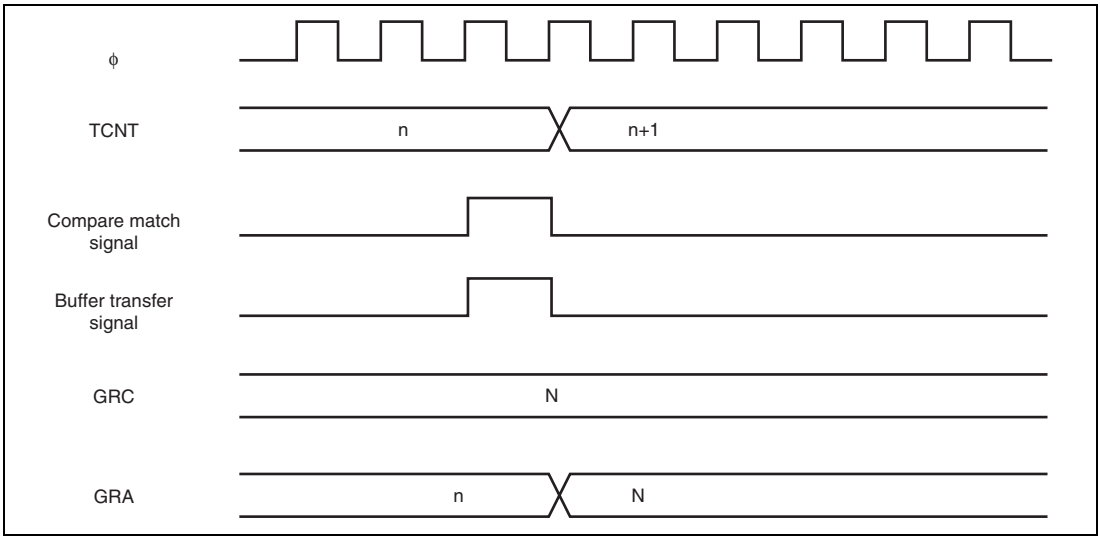


Figure 12.39 Example of Compare Match Timing for Buffer Operation

Figure 12.40 shows an operation example in which GRA has been designated as an input capture register, and buffer operation has been designated for GRA and GRC.

Counter clearing by input capture B has been set for TCNT, and falling edges have been selected as the FIOCB pin input capture input edge. And both rising and falling edges have been selected as the FIOCA pin input capture input edge.

As buffer operation has been set, when the TCNT value is stored in GRA upon the occurrence of input capture A, the value previously stored in GRA is simultaneously transferred to GRC. The transfer timing is shown in figure 12.41.

Note on Clearing TSR Flag: When a specific flag in TSR is cleared, a combination of the BCLR or MOV instructions is used to read 1 from the flag and then write 0 to the flag. However, if another bit is set during this processing, the bit may also be cleared simultaneously. To avoid this, the following processing that does not use the BCLR instruction must be executed. Note that this note is only applied to the F-ZTAT version. This problem has already been solved in the mask ROM version.

```
Example: When clearing bit 4 (OVF) in TSR
MOV.B @TSR,R0L
MOV.B #B'11101111, R0L <..... Only the bit to be cleared is 0 and
                              the other bits are all set to 1.
MOV.B R0L,@TSR
```

Note on Writing to the TOA0 to TOD0 Bits and the TOA1 to TOD1 Bits in TOCR:
The TOA0 to TOD0 bits and the TOA1 to TOD1 bits in TOCR decide the value of the FTIO pin, which is output until the first compare match occurs. Once a compare match occurs and this compare match changes the values of FTIOA0 to FTIOD0 and FTIOA1 to FTIOD1 output, the values of the FTIOA0 to FTIOD0 and FTIOA1 to FTIOD1 pin output and the values read from the TOA0 to TOD0 and TOA1 to TOD1 bits may differ. Moreover, when the writing to TOCR and the generation of the compare match A0 to D0 and A1 to D1 occur at the same timing, the writing to TOCR has the priority. Thus, output change due to the compare match is not reflected to the FTIOA0 to FTIOD0 and FTIOA1 to FTIOD1 pins. Therefore, when bit manipulation instruction is used to write to TOCR, the values of the FTIOA0 to FTIOD0 and FTIOA1 to FTIOD1 pin output may result in an unexpected result. When TOCR is to be written to while compare match is operating, stop the counter once before accessing to TOCR, read the port 6 state to reflect the values of FTIOA0 to FTIOD0 and FTIOA1 to FTIOD1 output, to TOA0 to TOD0 and TOA1 to TOD1, and then restart the counter. Figure 12.59 shows an example when the compare match and the bit manipulation instruction to TOCR occur at the same timing.

TOCR has been set to H'06. Compare match B0 and compare match C0 are used. The FTIOB0 pin is in the 1 output state, and is set to the toggle output or the 0 output by compare match B0.
When BCLR#2, @TOCR is executed to clear the TOC0 bit (the FTIOC0 signal is low) and compare match B0 occurs at the same timing as shown below, the H'02 writing to TOCR has priority and compare match B0 does not drive the FTIOB0 signal low; the FTIOB0 signal remains high.

Bit	7	6	5	4	3	2	1	0
TOCR	TOD1	TOC1	TOB1	TOA1	TOD0	TOC0	TOB0	TOA0
Set value	0	0	0	0	0	1	1	0

BCLR#2, @TOCR
(1) TOCR read operation: Read H'06
(2) Modify operation: Modify H'06 to H'02
(3) Write operation to TOCR: Write H'02

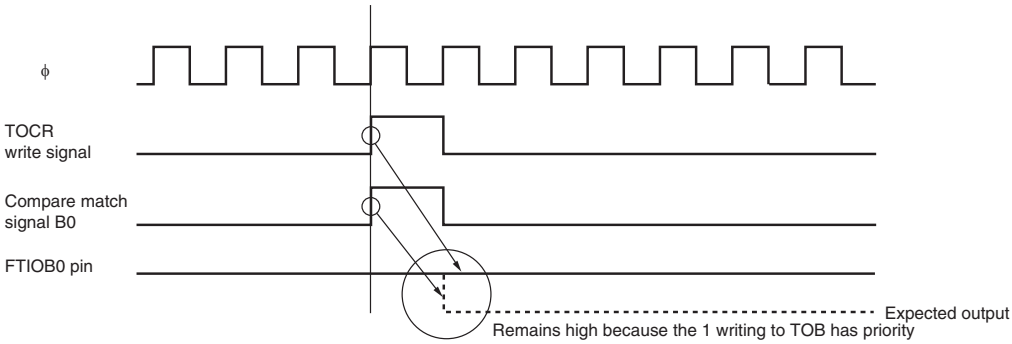


Figure 12.59 When Compare Match and Bit Manipulation Instruction to TOCR Occur at the Same Timing

15.3.4 General Status Register (GSR)

GSR indicates the status of the CAN bus. Each bit in GSR is set or cleared to notify the CPU of the TinyCAN status.

Bit	Bit Name	Initial Value	R/W	Description
7, 6	—	All 0	—	Reserved These bits are always read as 0.
5	ERPS	0	R	Error Passive Status Flag Indicates whether the CDLC is in the error-passive state. This flag is always set to 1 when the CDLC is in the error-passive state or bus off state. [Setting condition] When TEC ≥ 128 or REC ≥ 128 [Clearing condition] When the error-active state is entered
4	HALT	0	R	Halt Status Flag Indicates whether the TinyCAN is in halt mode. [Setting condition] When the CAN bus receives an intermission frame or the bus is idle with the HLTRQ bit in MCR set to 1 [Clearing condition] When the HLTRQ bit is cleared to 0 and halt mode is exited
3	RESET	1	R	Reset Status Flag Indicates whether the TinyCAN is in reset mode. [Setting condition] When the TinyCAN is in the reset state [Clearing condition] When communication with the CAN bus is enabled after the reset procedure completes

Bit	Bit Name	Initial Value	R/W	Description
2	SYSCKS	0	R/W	Subclock Supply Enable Enables or disables clock supply to the entire chip when the on-chip oscillator for the subtimer is used. 0: Clock supply is disabled. 1: Clock supply is enabled.
1	SBTIB	0	R/W	Subtimer Interrupt Request Enable When this bit is set to 1, an interrupt request caused by the SBTUF flag is enabled.
0	SBTUF	0	R/W	Underflow Interrupt Flag [Setting condition] When the SBTDCNT value underflows [Clearing condition] When 0 is written to this bit after reading 1

17.2.2 Subtimer Counter (SBTDCNT)

SBTDCNT is an 8-bit readable/writable down counter. When SBTDCNT underflows, an interrupt request is issued and the SBTUF flag in SBTCTL is set to 1. SBTDCNT is initialized to H'FF.

17.2.3 Ring Oscillator Prescaler Setting Register (ROPCR)

ROPCR is an 8-bit readable/writable register. When the OSCEB bit in SBTCTL is set to 1, SBTPS counts two system clock cycles from the first falling edge of the on-chip oscillator to the third falling edge and then transfers the count value to ROPCR. After that, ROPCR configures the division ratio of subclock. ROPCR is initialized to H'FF.

Register Abbreviation	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name
MD 2 [0]	MD07	MD06	MD05	MD04	MD03	MD02	MD01	MD00	TinyCAN
MD 2 [1]	MD17	MD16	MD15	MD14	MD13	MD12	MD11	MD10	
MD 2 [2]	MD27	MD26	MD25	MD24	MD23	MD22	MD21	MD20	
MD 2 [3]	MD37	MD36	MD35	MD34	MD33	MD32	MD31	MD30	
MD 2 [4]	MD47	MD46	MD45	MD44	MD43	MD42	MD41	MD40	
MD 2 [5]	MD57	MD56	MD55	MD54	MD53	MD52	MD51	MD50	
MD 2 [6]	MD67	MD66	MD65	MD64	MD63	MD62	MD61	MD60	
MD 2 [7]	MD77	MD76	MD75	MD74	MD73	MD72	MD71	MD70	
MD 3 [0]	MD07	MD06	MD05	MD04	MD03	MD02	MD01	MD00	
MD 3 [1]	MD17	MD16	MD15	MD14	MD13	MD12	MD11	MD10	
MD 3 [2]	MD27	MD26	MD25	MD24	MD23	MD22	MD21	MD20	
MD 3 [3]	MD37	MD36	MD35	MD34	MD33	MD32	MD31	MD30	
MD 3 [4]	MD47	MD46	MD45	MD44	MD43	MD42	MD41	MD40	
MD 3 [5]	MD57	MD56	MD55	MD54	MD53	MD52	MD51	MD50	
MD 3 [6]	MD67	MD66	MD65	MD64	MD63	MD62	MD61	MD60	
MD 3 [7]	MD77	MD76	MD75	MD74	MD73	MD72	MD71	MD70	
LAFML01	LAFML07	LAFML06	LAFML05	LAFML04	LAFML03	LAFML02	LAFML01	LAFML00	
LAFML00	LAFML015	LAFML014	LAFML013	LAFML012	LAFML011	LAFML010	LAFML09	LAFML08	
LAFMH01	LAFMH07	LAFMH06	LAFMH05	—	—	—	LAFMH01	LAFMH00	
LAFMH00	LAFMH015	LAFMH014	LAFMH013	LAFMH012	LAFMH011	LAFMH010	LAFMH09	LAFMH08	
LAFML11	LAFML17	LAFML16	LAFML15	LAFML14	LAFML13	LAFML12	LAFML11	LAFML10	
LAFML10	LAFML115	LAFML114	LAFML113	LAFML112	LAFML111	LAFML110	LAFML19	LAFML18	
LAFMH11	LAFMH17	LAFMH16	LAFMH15	—	—	—	LAFMH11	LAFMH10	
LAFMH10	LAFMH115	LAFMH114	LAFMH113	LAFMH112	LAFMH111	LAFMH110	LAFMH19	LAFMH18	
LAFML21	LAFML27	LAFML26	LAFML25	LAFML24	LAFML23	LAFML22	LAFML21	LAFML20	
LAFML20	LAFML215	LAFML214	LAFML213	LAFML212	LAFML211	LAFML210	LAFML29	LAFML28	
LAFMH21	LAFMH27	LAFMH26	LAFMH25	—	—	—	LAFMH21	LAFMH20	
LAFMH20	LAFMH215	LAFMH214	LAFMH213	LAFMH212	LAFMH211	LAFMH210	LAFMH29	LAFMH28	
LAFML31	LAFML37	LAFML36	LAFML35	LAFML34	LAFML33	LAFML32	LAFML31	LAFML30	
LAFML30	LAFML315	LAFML314	LAFML313	LAFML312	LAFML311	LAFML310	LAFML39	LAFML38	
LAFMH31	LAFMH37	LAFMH36	LAFMH35	—	—	—	LAFMH31	LAFMH30	
LAFMH30	LAFMH315	LAFMH314	LAFMH313	LAFMH312	LAFMH311	MAFMH310	LAFMH39	LAFMH38	

21.3 Register States in Each Operating Mode

Register Abbreviation	Reset	Active	Sleep	Subactive	Subsleep	Standby	Module
MCR	Initialized	—	—	—	—	—	TinyCAN
GSR	Initialized	—	—	—	—	—	
BCR1	Initialized	—	—	—	—	—	
BCR0	Initialized	—	—	—	—	—	
MBCR	Initialized	—	—	—	—	—	
TCMR	Initialized	—	—	—	—	—	
TXPR	Initialized	—	—	—	—	—	
TXCR	Initialized	—	—	—	—	—	
TXACK	Initialized	—	—	—	—	—	
ABACK	Initialized	—	—	—	—	—	
RXPR	Initialized	—	—	—	—	—	
RFPR	Initialized	—	—	—	—	—	
TCIRR1	Initialized	—	—	—	—	—	
TCIRR0	Initialized	—	—	—	—	—	
MBIMR	Initialized	—	—	—	—	—	
TCIMR1	Initialized	—	—	—	—	—	
TCIMR0	Initialized	—	—	—	—	—	
REC	Initialized	—	—	—	—	—	
TEC	Initialized	—	—	—	—	—	
TCR	Initialized	—	—	—	—	—	
UMSR	Initialized	—	—	—	—	—	
MC0[1]	—	—	—	—	—	—	
MC0[2]	—	—	—	—	—	—	
MC0[3]	—	—	—	—	—	—	
MC0[4]	—	—	—	—	—	—	
MC0[5]	—	—	—	—	—	—	
MC1[1]	—	—	—	—	—	—	
MC1[2]	—	—	—	—	—	—	
MC1[3]	—	—	—	—	—	—	

Item	Symbol	Applicable Pins	Test Condition	Values Min.	Typ.	Max.	Unit	Reference Figure
$\overline{RES}$ pin low width	t_{REL}	$\overline{RES}$	At power-on and in modes other than those below	t_{rc}	—	—	ms	Figure 22.2
			In active mode and sleep mode operation	1500	—	—	ns	
Input pin high width	t_{IH}	$\overline{NMI}$, $\overline{IRQ0}$ to $\overline{IRQ3}$, $\overline{WKP0}$ to $\overline{WKP5}$, TMCIV, TMRIV, TRGV, $\overline{ADTRG}$, FTIOA0 to FTIOD0, FTIOA1 to FTIOD1		2	—	—	t_{cyc} t_{subcyc}	Figure 22.3
Input pin low width	t_{IL}	$\overline{NMI}$, $\overline{IRQ0}$ to $\overline{IRQ3}$, $\overline{WKP0}$ to $\overline{WKP5}$, TMCIV, TMRIV, TRGV, $\overline{ADTRG}$, FTIOA0 to FTIOD0, FTIOA1 to FTIOD1		2	—	—	t_{cyc} t_{subcyc}	

Notes: 1. When an external clock is input, the minimum system clock oscillation frequency is 1.0 MHz.

2. Determined by the MA2, MA1, MA0, SA1, and SA0 bits in the system control register 2 (SYSCR2).

2. Arithmetic Instructions

Mnemonic		Operand Size	Addressing Mode and Instruction Length (bytes)									Operation	Condition Code						No. of States*1	
			#xx	Rn	@ERn	@(d, ERn)	@–ERn/@ERn+	@aa	@(d, PC)	@@aa	—		I	H	N	Z	V	C	Normal	Advanced
ADD	ADD.B #xx:8, Rd	B	2									Rd8+#xx:8 → Rd8	—	↕	↕	↕	↕	↕	2	
	ADD.B Rs, Rd	B		2								Rd8+Rs8 → Rd8	—	↕	↕	↕	↕	↕	2	
	ADD.W #xx:16, Rd	W	4									Rd16+#xx:16 → Rd16	—	(1)	↕	↕	↕	↕	4	
	ADD.W Rs, Rd	W		2								Rd16+Rs16 → Rd16	—	(1)	↕	↕	↕	↕	2	
	ADD.L #xx:32, ERd	L	6									ERd32+#xx:32 → ERd32	—	(2)	↕	↕	↕	↕	6	
	ADD.L ERs, ERd	L		2								ERd32+ERs32 → ERd32	—	(2)	↕	↕	↕	↕	2	
ADDX	ADDX.B #xx:8, Rd	B	2									Rd8+#xx:8 +C → Rd8	—	↕	↕	(3)	↕	↕	2	
	ADDX.B Rs, Rd	B		2								Rd8+Rs8 +C → Rd8	—	↕	↕	(3)	↕	↕	2	
ADDS	ADDS.L #1, ERd	L		2								ERd32+1 → ERd32	—	—	—	—	—	—	2	
	ADDS.L #2, ERd	L		2								ERd32+2 → ERd32	—	—	—	—	—	—	2	
	ADDS.L #4, ERd	L		2								ERd32+4 → ERd32	—	—	—	—	—	—	2	
INC	INC.B Rd	B		2								Rd8+1 → Rd8	—	—	↕	↕	↕	—	2	
	INC.W #1, Rd	W		2								Rd16+1 → Rd16	—	—	↕	↕	↕	—	2	
	INC.W #2, Rd	W		2								Rd16+2 → Rd16	—	—	↕	↕	↕	—	2	
	INC.L #1, ERd	L		2								ERd32+1 → ERd32	—	—	↕	↕	↕	—	2	
	INC.L #2, ERd	L		2								ERd32+2 → ERd32	—	—	↕	↕	↕	—	2	
DAA	DAA Rd	B		2								Rd8 decimal adjust → Rd8	—	*	↕	↕	*	↕	2	
SUB	SUB.B Rs, Rd	B		2								Rd8–Rs8 → Rd8	—	↕	↕	↕	↕	↕	2	
	SUB.W #xx:16, Rd	W	4									Rd16–#xx:16 → Rd16	—	(1)	↕	↕	↕	↕	4	
	SUB.W Rs, Rd	W		2								Rd16–Rs16 → Rd16	—	(1)	↕	↕	↕	↕	2	
	SUB.L #xx:32, ERd	L	6									ERd32–#xx:32 → ERd32	—	(2)	↕	↕	↕	↕	6	
	SUB.L ERs, ERd	L		2								ERd32–ERs32 → ERd32	—	(2)	↕	↕	↕	↕	2	
SUBX	SUBX.B #xx:8, Rd	B	2									Rd8–#xx:8–C → Rd8	—	↕	↕	(3)	↕	↕	2	
	SUBX.B Rs, Rd	B		2								Rd8–Rs8–C → Rd8	—	↕	↕	(3)	↕	↕	2	
SUBS	SUBS.L #1, ERd	L		2								ERd32–1 → ERd32	—	—	—	—	—	—	2	
	SUBS.L #2, ERd	L		2								ERd32–2 → ERd32	—	—	—	—	—	—	2	
	SUBS.L #4, ERd	L		2								ERd32–4 → ERd32	—	—	—	—	—	—	2	
DEC	DEC.B Rd	B		2								Rd8–1 → Rd8	—	—	↕	↕	↕	—	2	
	DEC.W #1, Rd	W		2								Rd16–1 → Rd16	—	—	↕	↕	↕	—	2	
	DEC.W #2, Rd	W		2								Rd16–2 → Rd16	—	—	↕	↕	↕	—	2	

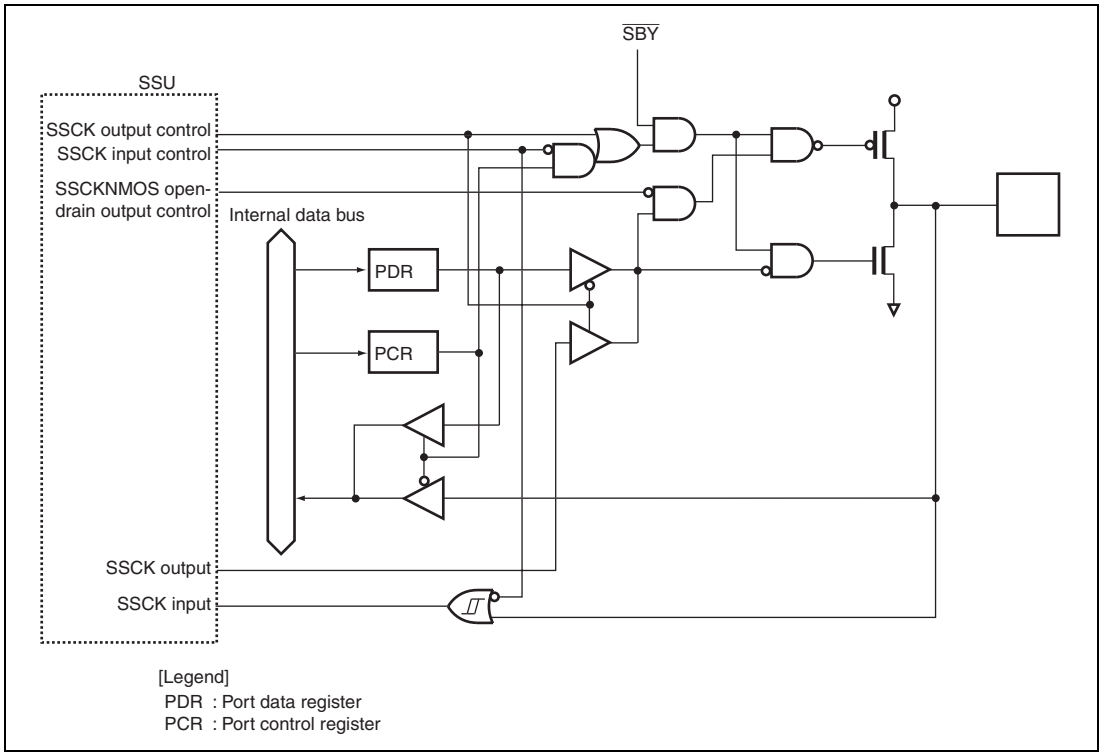


Figure B.25 Port 9 Block Diagram (P91)

Appendix C Product Code Lineup

Product Classification			Package Code: QFP-64 (FP-64A)	Package Code: LQFP-64 (FP-64K)
H8/36057	Flash memory version	Standard product	HD64F36057H	HD64F36057FZ
		Product with POR & LVDC	HD64F36057GH	HD64F36057GFZ
	Masked ROM version	Standard product	HD64336057(***)H	HD64336057(***)FZ
		Product with POR & LVDC	HD64336057G(***)H	HD64336057G(***)FZ
H8/36054	Flash memory version	Standard product	HD64F36054H	HD64F36054FZ
		Product with POR & LVDC	HD64F36054GH	HD64F36054GFZ
	Masked ROM version	Standard product	HD64336054(***)H	HD64336054(***)FZ
		Product with POR & LVDC	HD64336054G(***)H	HD64336054G(***)FZ
H8/36037	Flash memory version	Standard product	HD64F36037H	HD64F36037FZ
		Product with POR & LVDC	HD64F36037GH	HD64F36037GFZ
	Masked ROM version	Standard product	HD64336037(***)H	HD64336037(***)FZ
		Product with POR & LVDC	HD64336037G(***)H	HD64336037G(***)FZ
H8/36036	Masked ROM version	Standard product	HD64336036(***)H	HD64336036(***)FZ
		Product with POR & LVDC	HD64336036G(***)H	HD64336036G(***)FZ
H8/36035	Masked ROM version	Standard product	HD64336035(***)H	HD64336035(***)FZ
		Product with POR & LVDC	HD64336035G(***)H	HD64336035G(***)FZ