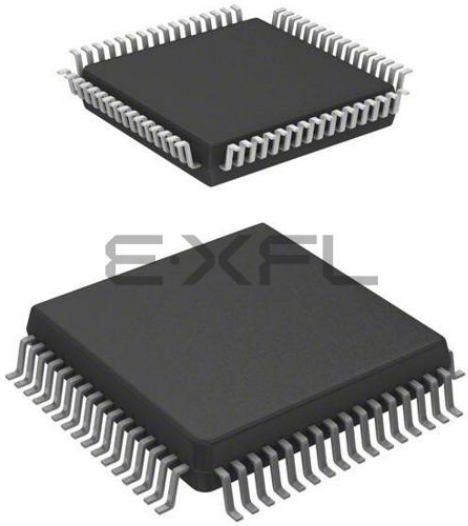

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300H
Core Size	16-Bit
Speed	20MHz
Connectivity	CANbus, SCI, SSU
Peripherals	PWM, WDT
Number of I/O	45
Program Memory Size	56KB (56K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-BQFP
Supplier Device Package	64-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df36057hjv

Figures

3.2.4 Interrupt Enable Register 2 (IENR2)

IENR2 enables, timer B1 overflow interrupts.

Bit	Bit Name	Initial Value	R/W	Description
7, 6	—	All 0	—	Reserved These bits are always read as 0.
5	IENTB1	0	R/W	Timer B1 Interrupt Enable When this bit is set to 1, timer B1 overflow interrupt requests are enabled.
4 to 0	—	All 1	—	Reserved These bits are always read as 1.

When disabling interrupts by clearing bits in an interrupt enable register, or when clearing bits in an interrupt flag register, always do so while interrupts are masked (I = 1). If the above clear operations are performed while I = 0, and as a result a conflict arises between the clear instruction and an interrupt request, exception handling for the interrupt will be executed after the clear instruction has been executed.

3.2.5 Interrupt Flag Register 1 (IRR1)

IRR1 is a status flag register for direct transition interrupts and IRQ3 to IRQ0 interrupt requests.

Bit	Bit Name	Initial Value	R/W	Description
7	IRRDT	0	R/W	Direct Transfer Interrupt Request Flag [Setting condition] When a direct transfer is made by executing a SLEEP instruction while DTON in SYSCR2 is set to 1. [Clearing condition] When IRRDT is cleared by writing 0
6	—	0	—	Reserved This bit is always read as 0.
5, 4	—	All 1	—	Reserved These bits are always read as 1.

Section 6 Power-Down Modes

This LSI has six modes of operation after a reset. These include a normal active mode and four power-down modes, in which power consumption is significantly reduced. Module standby mode reduces power consumption by selectively halting on-chip module functions.

- Active mode

  The CPU and all on-chip peripheral modules are operable on the system clock. The system clock frequency can be selected from ϕosc, ϕosc/8, ϕosc/16, ϕosc/32, and ϕosc/64.
- Subactive mode

  The CPU and all on-chip peripheral modules are operable on the subclock. The subclock frequency can be selected from ϕw/2, ϕw/4, and ϕw/8.
- Sleep mode

  The CPU halts. On-chip peripheral modules are operable on the system clock.
- Subsleep mode

  The CPU halts. On-chip peripheral modules are operable on the subclock.
- Standby mode

  The CPU and all on-chip peripheral modules halt.
- Module standby mode

  Independent of the above modes, power consumption can be reduced by halting on-chip peripheral modules that are not used in module units.

Table 7.4 Reprogram Data Computation Table

Program Data	Verify Data	Reprogram Data	Comments
0	0	1	Programming completed
0	1	0	Reprogram bit
1	0	1	—
1	1	1	Remains in erased state

Table 7.5 Additional-Program Data Computation Table

Reprogram Data	Verify Data	Additional-Program Data	Comments
0	0	0	Additional-program bit
0	1	1	No additional programming
1	0	1	No additional programming
1	1	1	No additional programming

Table 7.6 Programming Time

n (Number of Writes)	Programming Time	In Additional Programming	Comments
1 to 6	30	10	
7 to 1,000	200	—	

Note: Time shown in μs.

- P11 pin

Register	PCR1	
Bit Name	**PCR11**	**Pin Function**
Setting value	0	P11 input pin
	1	P11 output pin

- P10 pin

Register	PCR1	
Bit Name	**PCR10**	**Pin Function**
Setting value	0	P10 input pin
	1	P10 output pin

9.2 Port 2

Port 2 is a general I/O port also functioning as SCI3 I/O pins. Each pin of the port 2 is shown in figure 9.2. The register settings of PMR1and SCI3 have priority for functions of the pins for both uses.

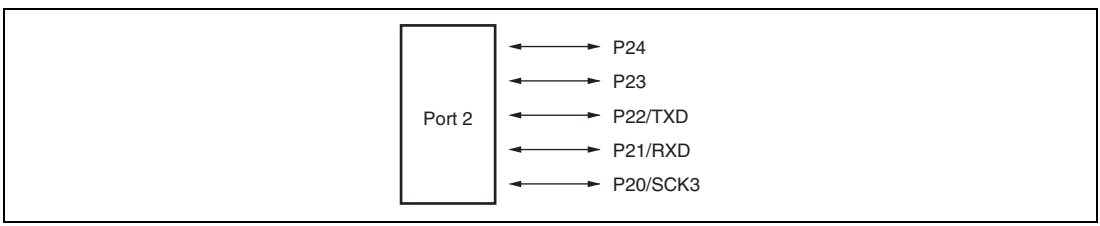


Figure 9.2 Port 2 Pin Configuration

Port 2 has the following registers.

- Port control register 2 (PCR2)
- Port data register 2 (PDR2)
- Port mode register 3 (PMR3)

- P62/FTIOC0 pin

Register	TOER	TFCR	TPMR	TIORC0	PCR6	
Bit Name	**EC0**	**CMD1, CMD0**	**PWMC0**	**IOC2 to IOC0**	**PCR62**	**Pin Function**
Setting Value	1	00	0	000 or 1XX	0	P62 input/FTIOC0 input pin
					1	P62 output pin
	0	00	0	001 or 01X	X	FTIOC0 output pin
			1	XXX		
		Other than 00	X	XXX		

[Legend]
X: Don't care.

- P61/FTIOB0 pin

Register	TOER	TFCR	TPMR	TIORA0	PCR6	
Bit Name	**EB0**	**CMD1, CMD0**	**PWMB0**	**IOB2 to IOB0**	**PCR61**	**Pin Function**
Setting Value	1	00	0	000 or 1XX	0	P61 input/FTIOB0 input pin
					1	P61 output pin
	0	00	0	001 or 01X	X	FTIOB0 output pin
			1	XXX		
		Other than 00	X	XXX		

[Legend]
X: Don't care.

Bit	Bit Name	Initial Value	R/W	Description
1	—	1	—	Reserved This bit is always read as 1.
0	ICKS0	0	R/W	Internal Clock Select 0 This bit selects clock signals to input to TCNTV in combination with CKS2 to CKS0 in TCRV0. Refer to table 11.2.

11.4 Operation

11.4.1 Timer V Operation

1. According to table 11.2, six internal/external clock signals output by prescaler S can be selected as the timer V operating clock signals. When the operating clock signal is selected, TCNTV starts counting-up. Figure 11.2 shows the count timing with an internal clock signal selected, and figure 11.3 shows the count timing with both edges of an external clock signal selected.
2. When TCNTV overflows (changes from H'FF to H'00), the overflow flag (OVF) in TCRV0 will be set. The timing at this time is shown in figure 11.4. An interrupt request is sent to the CPU when OVIE in TCRV0 is 1.
3. TCNTV is constantly compared with TCORA and TCORB. Compare match flag A or B (CMFA or CMFB) is set to 1 when TCNTV matches TCORA or TCORB, respectively. The compare-match signal is generated in the last state in which the values match. Figure 11.5 shows the timing. An interrupt request is generated for the CPU when CMIEA or CMIEB in TCRV0 is 1.
4. When a compare match A or B is generated, the TMOV responds with the output value selected by bits OS3 to OS0 in TCSRV. Figure 11.6 shows the timing when the output is toggled by compare match A.
5. When CCLR1 or CCLR0 in TCRV0 is 01 or 10, TCNTV can be cleared by the corresponding compare match. Figure 11.7 shows the timing.
6. When CCLR1 or CCLR0 in TCRV0 is 11, TCNTV can be cleared by the rising edge of the input of TMRIV pin. A TMRIV input pulse-width of at least 1.5 system clocks is necessary. Figure 11.8 shows the timing.
7. When a counter-clearing source is generated with TRGE in TCRV1 set to 1, the counting-up is halted as soon as TCNTV is cleared. TCNTV resumes counting-up when the edge selected by TVEG1 or TVEG0 in TCRV1 is input from the TGRV pin.

Contention between GR Read and Input Capture: If an input capture signal is generated in the T_1 state of a GR read cycle, the data that is read will be transferred before input capture transfer. Figure 12.56 shows the timing in this case.

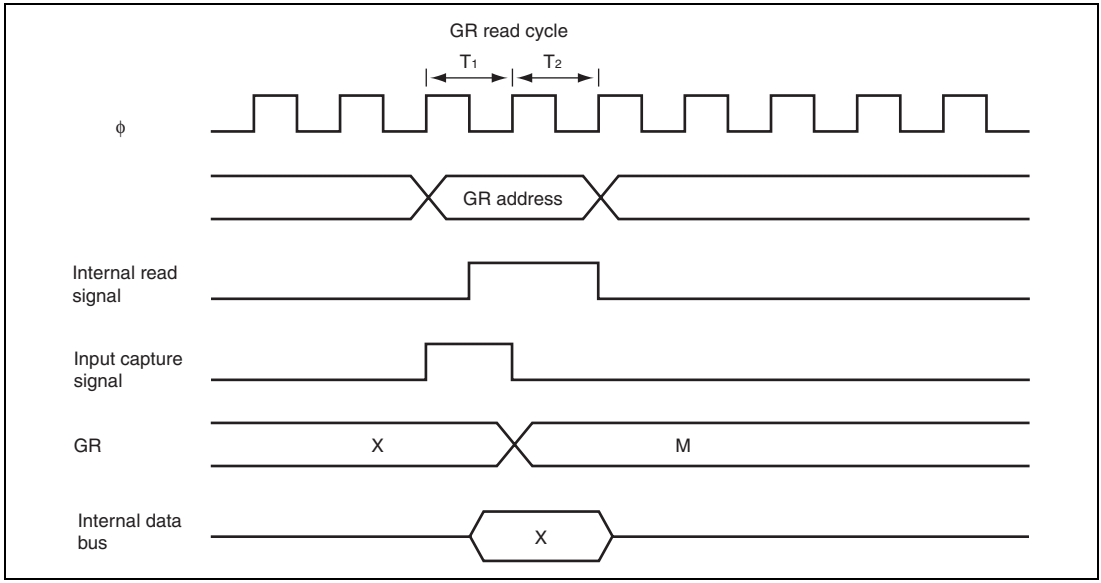
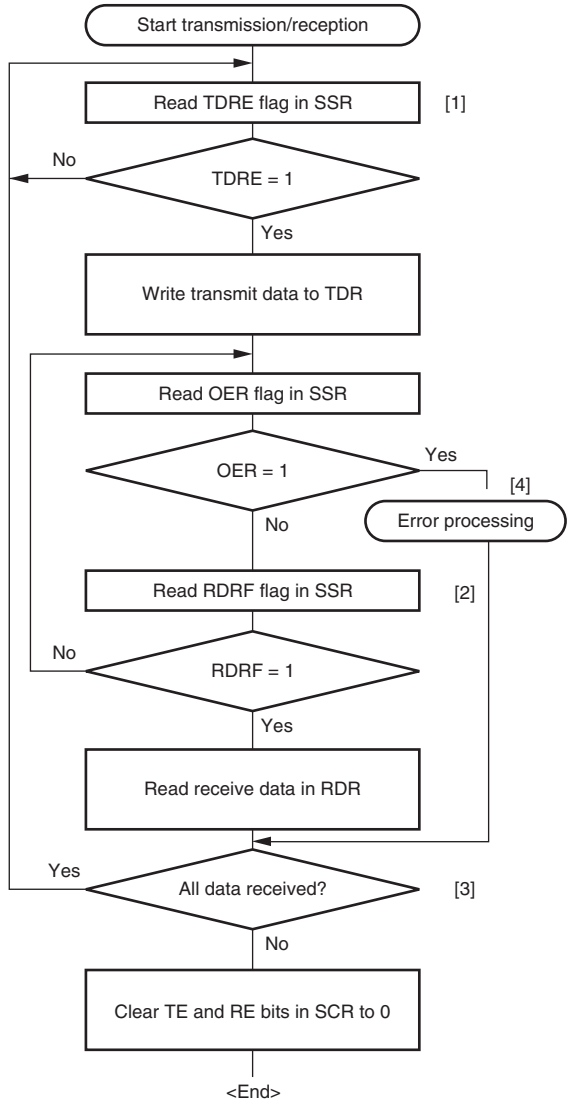


Figure 12.56 Contention between GR Read and Input Capture



[1] Read SSR and check that the TDRE flag is set to 1, then write transmit data to TDR.
When data is written to TDR, the TDRE flag is automatically cleared to 0.

[2] Read SSR and check that the RDRF flag is set to 1, then read the receive data in RDR.
When data is read from RDR, the RDRF flag is automatically cleared to 0.

[3] To continue serial transmission/ reception, before the MSB (bit 7) of the current frame is received, finish reading the RDRF flag, reading RDR. Also, before the MSB (bit 7) of the current frame is transmitted, read 1 from the TDRE flag to confirm that writing is possible. Then write data to TDR.
When data is written to TDR, the TDRE flag is automatically cleared to 0. When data is read from RDR, the RDRF flag is automatically cleared to 0.

[4] If an overrun error occurs, read the OER flag in SSR, and after performing the appropriate error processing, clear the OER flag to 0. Transmission/reception cannot be resumed if the OER flag is set to 1. For overrun error processing, see figure 14.13.

Figure 14.14 Sample Flowchart of Simultaneous Serial Transmit and Receive Operations (Clocked Synchronous Mode)

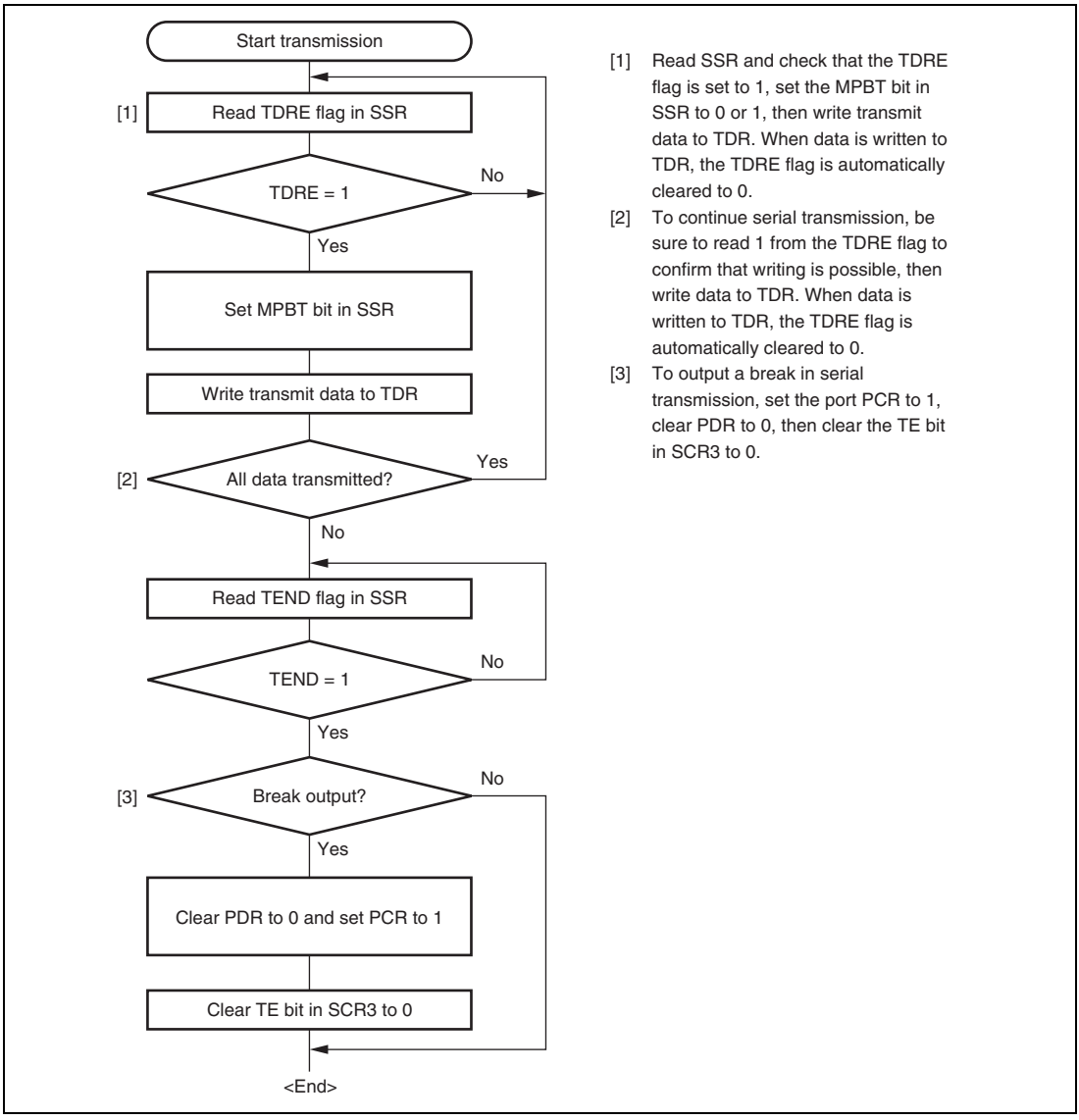


Figure 14.16 Sample Multiprocessor Serial Transmission Flowchart

14.6.2 Multiprocessor Serial Data Reception

Figure 14.17 shows a sample flowchart for multiprocessor serial data reception. If the MPIE bit in SCR3 is set to 1, data is skipped until data with a 1 multiprocessor bit is sent. On receiving data with a 1 multiprocessor bit, the receive data is transferred to RDR. An RXI interrupt request is

15.3.5 Bit Configuration Registers 0, 1 (BCR0, BCR1)

BCR configures the CAN bit timing parameters and baud rate prescaler for the CDLC.

- BCR0

Bit	Bit Name	Initial Value	R/W	Description
7	SJW1	0	R/W	Re-Synchronization Jump Width
6	SJW0	0	R/W	These bits set the maximum value of synchronization width. 00: 1 time quantum 01: 2 time quanta 10: 3 time quanta 11: 4 time quanta
5	BRP5	0	R/W	Baud Rate Prescaler
4	BRP4	0	R/W	These bits set the clock used for time quanta.
3	BRP3	0	R/W	000000: Setting prohibited
2	BRP2	0	R/W	000001: 2 system clocks
1	BRP1	0	R/W	: : (BRP + 1) system clocks
0	BRP0	0	R/W	111111: 64 system clocks

- BCR1

Bit	Bit Name	Initial Value	R/W	Description
7	—	0	—	Reserved This bit is always read as 0. The write value should always be 0.

Register Name	Bit	Bit Name	R/W	Description
MCn[0] (n = 0 to 3)	7	DART	R/W	Automatic Retransmission Disable When this bit is set to 1,the message disables to be retransmitted in the event of an error on CAN bus or an arbitration lost on CAN bus. 0: Automatic retransmission is carried out 1: Automatic retransmission is prohibited
	6	NMC	R/W	New Message Control When a Mailbox with an unread message receives a new message, this bit selects whether to overrun or overwrite the unread message with the new message. 0: The new receive message is ignored and the unread message is saved, and the corresponding UMSR bit is set to 1 (overrun) 1: The unread message is lost by being overwritten with the new receive message, and the corresponding UMSR bit is set to 1 (overwrite)
	5, 4	—	—	Reserved These bits are always read as 0.
	3 to 0	DLC3 to DLC0	R/W	Data Length Code These bits set the transmit data length of data frames and data length requested by remote frames. These bits are stipulated in Bosch 2.0B active. 0000: 0 bytes 0001: 1 byte 0010: 2 bytes 0011: 3 bytes 0100: 4 bytes 0101: 5 bytes 0110: 6 bytes 0111: 7 bytes 1xxx: 8 bytes
MCn[4] (n = 0 to 3)	7 to 5	ID20 to ID18	R/W	These bits set bits 2 to 0 in the standard identifier of data frames and remote frames.

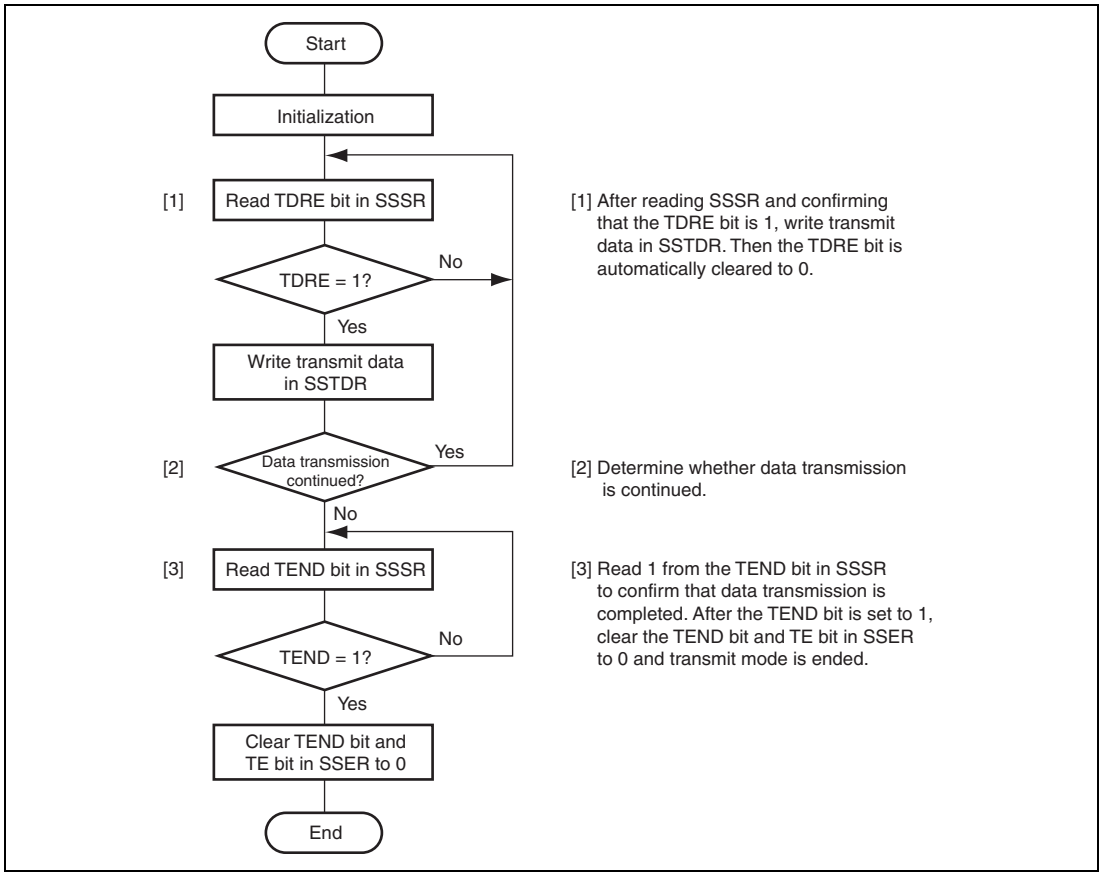


Figure 16.6 Sample Serial Transmission Flowchart

Section 17 Subsystem Timer (Subtimer)

The subtimer is a timer for controlling subsystem which has an on-chip oscillator for supplying system clocks in subactive and subsleep modes and an on-chip 8-bit down counter. Since the subtimer has a prescaler that can set the division ratio by software, it can supply a clock with any frequency. This LSI has an on-chip single-channel subtimer.

17.1 Features

- On-chip oscillator
  Oscillation frequency: 64 kHz to 850 kHz
  Temperature characteristic: Source clock ± 10% (typ.)
- Counter: two
  8-bit readable/writable down counter
  8-bit counter for measuring oscillation frequency of the on-chip oscillator
- CPU interrupt source
  Underflow (interrupt interval: 731 µsec to 67.4 msec)
- Subtimer clock supply operating modes:
  Subactive mode
  Subsleep mode
- On-chip oscillator
  The on-chip oscillator supplies three kinds of clocks:
  Subactive or subsleep mode (ϕ_w)
  Subtimer down counter (input clock)
  Watchdog timer (input clock)
- Subtimer prescaler (SBTPS)
  The subtimer prescaler is a divider which controls input clocks to the counter which measures oscillation cycle of the on-chip oscillator and the down counter for the subtimer.

Register Abbreviation	Reset	Active	Sleep	Subactive	Subsleep	Standby	Module
MC1[4]	—	—	—	—	—	—	TinyCAN
MC1[5]	—	—	—	—	—	—	
MC2[1]	—	—	—	—	—	—	
MC2[2]	—	—	—	—	—	—	
MC2[3]	—	—	—	—	—	—	
MC2[4]	—	—	—	—	—	—	
MC2[5]	—	—	—	—	—	—	
MC3[1]	—	—	—	—	—	—	
MC3[2]	—	—	—	—	—	—	
MC3[3]	—	—	—	—	—	—	
MC3[4]	—	—	—	—	—	—	
MC3[5]	—	—	—	—	—	—	
MD0[1]	—	—	—	—	—	—	
MD0[2]	—	—	—	—	—	—	
MD0[3]	—	—	—	—	—	—	
MD0[4]	—	—	—	—	—	—	
MD0[5]	—	—	—	—	—	—	
MD0[6]	—	—	—	—	—	—	
MD0[7]	—	—	—	—	—	—	
MD0[8]	—	—	—	—	—	—	
MD1[1]	—	—	—	—	—	—	
MD1[2]	—	—	—	—	—	—	
MD1[3]	—	—	—	—	—	—	
MD1[4]	—	—	—	—	—	—	
MD1[5]	—	—	—	—	—	—	
MD1[6]	—	—	—	—	—	—	
MD1[7]	—	—	—	—	—	—	
MD1[8]	—	—	—	—	—	—	
MD2[1]	—	—	—	—	—	—	
MD2[2]	—	—	—	—	—	—	
MD2[3]	—	—	—	—	—	—	

Item	Symbol	Applicable Pins	Test Condition	Values Min.	Typ.	Max.	Unit	Notes
Output low voltage	V_{OL}	P10 to P12, P14 to P17, P20 to P24, P50 to P57, P70 to P72, P74 to P76, P85 to P87 P90 to P97	V_{CC} = 4.0 to 5.5 V I_{OL} = 1.6 mA	—	—	0.6	V	
			I_{OL} = 0.4 mA	—	—	0.4		
		P60 to P67	V_{CC} = 4.0 to 5.5 V I_{OL} = 20.0 mA	—	—	1.5	V	
			V_{CC} = 4.0 to 5.5 V I_{OL} = 10.0 mA	—	—	1.0		
			V_{CC} = 4.0 to 5.5 V I_{OL} = 1.6 mA	—	—	0.4		
			I_{OL} = 0.4 mA	—	—	0.4		
Input/ output leakage current	$\lvert I_{IL} \rvert$	OSC1, $\overline{RES}$, $\overline{NMI}$, $\overline{WKP0}$ to $\overline{WKP5}$, $\overline{IRQ0}$ to $\overline{IRQ3}$, $\overline{ADTRG}$, TRGV, TMRIV, TMCIV, FTIOA0 to FTIOD0, FTIOA1 to FTIOD1, RXD, SCK3, RXD_2*[1], SCK3_2*[1], SSCK, $\overline{SCS}$, SSI, SSO, HRXD	V_{IN} = 0.5 V or higher (V_{CC} – 0.5 V)	—	—	1.0	µA	
		P10 to P12, P14 to P17, P20 to P24, P50 to P57, P60 to P67, P70 to P72, P74 to P76, P85 to P87, P90 to P97	V_{IN} = 0.5 V or higher (V_{CC} – 0.5 V)	—	—	1.0	µA	
		PB0 to PB7	V_{IN} = 0.5 V or higher (AV_{CC} – 0.5 V)	—	—	1.0	µA	

Table 22.13 DC Characteristics (2)

V_{CC} = 2.7 to 5.5 V, V_{SS} = 0.0 V, T_a = –20 to +75°C (regular specifications) or T_a = –40 to +85°C (wide-range specifications), unless otherwise indicated.

				Values			
Item	**Symbol**	**Applicable Pins**	**Test Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
Allowable output low current (per pin)	I_{OL}	Output pins except port 6	V_{CC} = 4.0 to 5.5 V	—	—	2.0	mA
		Port 6		—	—	20.0	
		Output pins except port 6		—	—	0.5	
		Port 6		—	—	10.0	
Allowable output low current (total)	ΣI_{OL}	Output pins except port 6	V_{CC} = 4.0 to 5.5 V	—	—	40.0	mA
		Port 6		—	—	80.0	
		Output pins except port 6		—	—	20.0	
		Port 6		—	—	40.0	
Allowable output high current (per pin)	$\lvert -I_{OH} \rvert$	All output pins	V_{CC} = 4.0 to 5.5 V	—	—	2.0	mA
				—	—	0.2	
Allowable output high current (total)	$\Sigma \lvert -I_{OH} \rvert$	All output pins	V_{CC} = 4.0 to 5.5 V	—	—	30.0	mA
				—	—	8.0	

Appendix B I/O Port Block Diagrams

B.1 I/O Port Block Diagrams

$\overline{RES}$ goes low in a reset, and $\overline{SBY}$ goes low at reset and in standby mode.

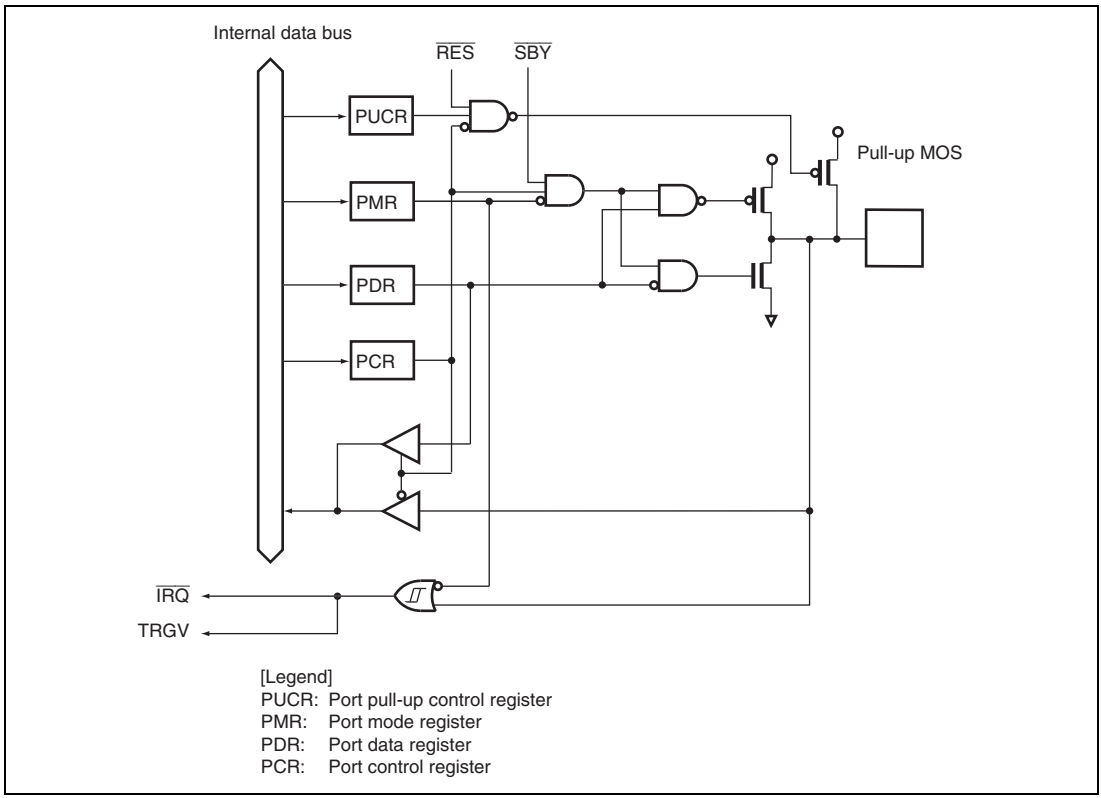


Figure B.1 Port 1 Block Diagram (P17)

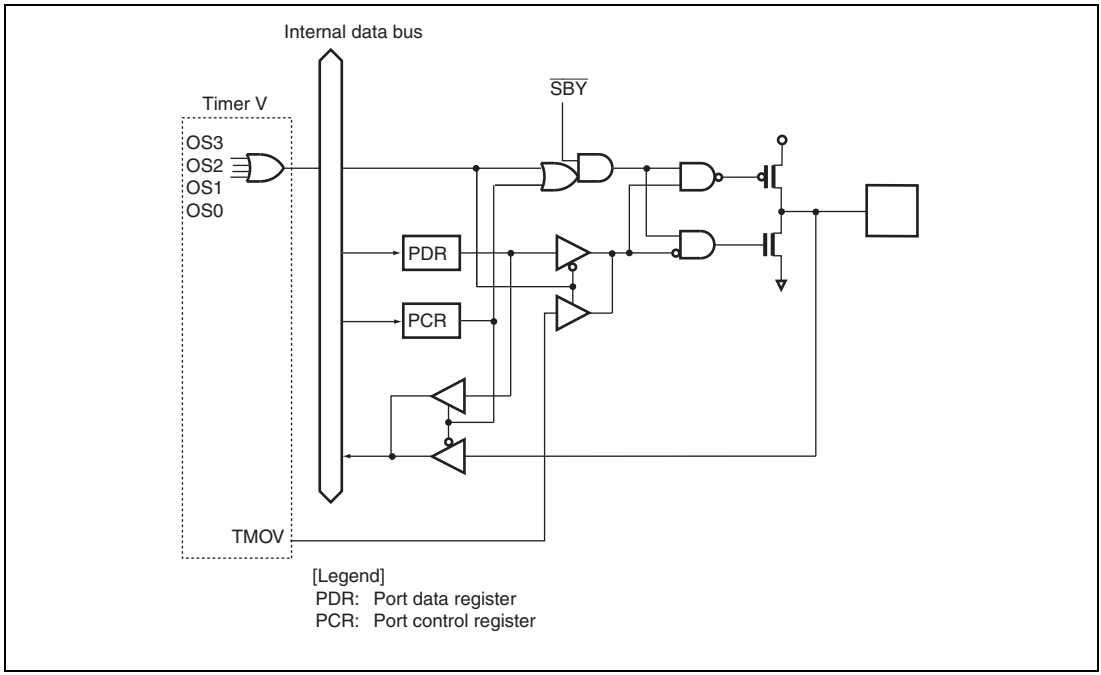


Figure B.13 Port 7 Block Diagram (P76)