Atmel - ATTINY44-20MUR Datasheet

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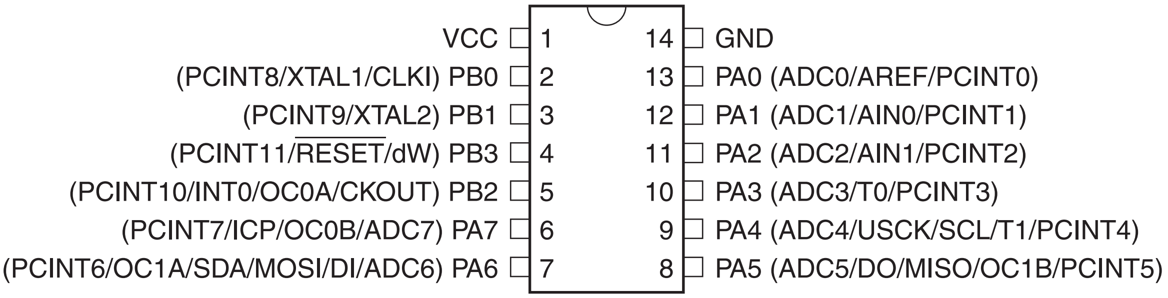
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8-Bit
Speed	20MHz
Connectivity	USI
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	12
Program Memory Size	4KB (2K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-WFQFN Exposed Pad
Supplier Device Package	20-QFN-EP (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/atmel/attiny44-20mur

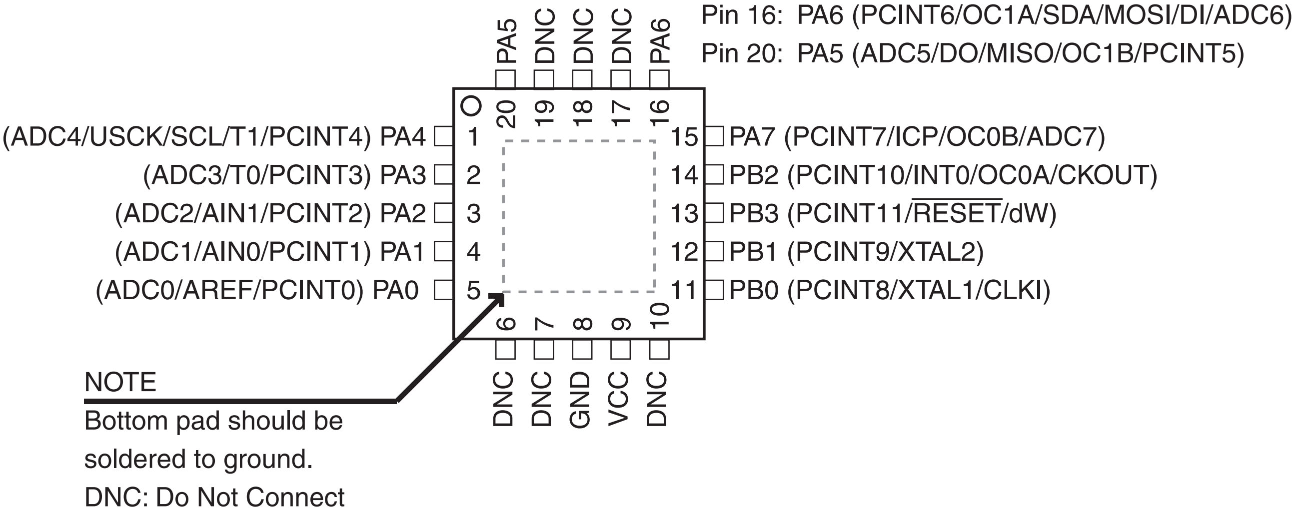
1. Pin Configurations

Figure 1-1. Pinout ATtiny24/44/84

PDIP/SOIC



QFN/MLF



1.1 Pin Descriptions

1.1.1 VCC

Supply voltage.

1.1.2 GND

Ground.

1.1.3 Port B (PB3:PB0)

Port B is a 4-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability except PB3 which has the $\overline{\text{RESET}}$ capability. To use pin PB3 as an I/O pin, instead of RESET pin, program (‘0’) RSTDISBL fuse. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port B also serves the functions of various special features of the ATtiny24/44/84 as listed in Section 10.2 “Alternate Port Functions” on page 58.

1.1.4 $\overline{\text{RESET}}$

Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running and provided the reset pin has not been disabled. The minimum pulse length is given in Table 20-4 on page 177. Shorter pulses are not guaranteed to generate a reset.

The reset pin can also be used as a (weak) I/O pin.

1.1.5 Port A (PA7:PA0)

Port A is a 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port A output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port A pins that are externally pulled low will source current if the pull-up resistors are activated. The Port A pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port A has alternate functions as analog inputs for the ADC, analog comparator, timer/counter, SPI and pin change interrupt as described in “Alternate Port Functions” on page 58.

The ATtiny24/44/84 provides the following features: 2/4/8K byte of In-System Programmable Flash, 128/256/512 bytes EEPROM, 128/256/512 bytes SRAM, 12 general purpose I/O lines, 32 general purpose working registers, an 8-bit Timer/Counter with two PWM channels, a 16-bit timer/counter with two PWM channels, Internal and External Interrupts, a 8-channel 10-bit ADC, programmable gain stage (1x, 20x) for 12 differential ADC channel pairs, a programmable Watchdog Timer with internal oscillator, internal calibrated oscillator, and four software selectable power saving modes. Idle mode stops the CPU while allowing the SRAM, Timer/Counter, ADC, Analog Comparator, and Interrupt system to continue functioning. ADC Noise Reduction mode minimizes switching noise during ADC conversions by stopping the CPU and all I/O modules except the ADC. In Power-down mode registers keep their contents and all chip functions are disbaled until the next interrupt or hardware reset. In Standby mode, the crystal/resonator oscillator is running while the rest of the device is sleeping, allowing very fast start-up combined with low power consumption.

The device is manufactured using Atmel's high density non-volatile memory technology. The on-chip ISP Flash allows the Program memory to be re-programmed in-system through an SPI serial interface, by a conventional non-volatile memory programmer or by an on-chip boot code running on the AVR core.

The ATtiny24/44/84 AVR is supported with a full suite of program and system development tools including: C Compilers, Macro Assemblers, Program Debugger/Simulators and Evaluation kits.

3. About

3.1 Resources

A comprehensive set of drivers, application notes, data sheets and descriptions on development tools are available for download at http://www.atmel.com/avr.

3.2 Code Examples

This documentation contains simple code examples that briefly show how to use various parts of the device. These code examples assume that the part specific header file is included before compilation. Be aware that not all C compiler vendors include bit definitions in the header files and interrupt handling in C is compiler dependent. Please confirm with the C compiler documentation for more details.

For I/O Registers located in the extended I/O map, “IN”, “OUT”, “SBIS”, “SBIC”, “CBI”, and “SBI” instructions must be replaced with instructions that allow access to extended I/O. Typically, this means “LDS” and “STS” combined with “SBRS”, “SBRC”, “SBR”, and “CBR”. Note that not all AVR devices include an extended I/O map.

3.3 Data Retention

Reliability Qualification results show that the projected data retention failure rate is much less than 1 PPM over 20 years at 85°C or 100 years at 25°C.

3.4 Disclaimer

Typical values contained in this datasheet are based on simulations and characterization of other AVR microcontrollers manufactured on the same process technology.

4. Register Summary

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
0x3F (0x5F)	SREG	I	T	H	S	V	N	Z	C	Page 8
0x3E (0x5E)	SPH	–	–	–	–	–	–	SP9	SP8	Page 11
0x3D (0x5D)	SPL	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	Page 11
0x3C (0x5C)	OCR0B	Timer/Counter0 – Output Compare Register B								Page 85
0x3B (0x5B)	GIMSK	–	INT0	PCIE1	PCIE0	–	–	–	–	Page 51
0x3A (0x5A	GIFR	–	INTF0	PCIF1	PCIF0	–	–	–	–	Page 52
0x39 (0x59)	TIMSK0	–	–	–	–	–	OCIE0B	OCIE0A	TOIE0	Page 85
0x38 (0x58)	TIFR0		–	–	–	–	OCF0B	OCF0A	TOV0	Page 85
0x37 (0x57)	SPMCSR	–	–	RSIG	CTPB	RFLB	PGWRT	PGERS	SPMEN	Page 157
0x36 (0x56)	OCR0A	Timer/Counter0 – Output Compare Register A								Page 84
0x35 (0x55)	MCUCR	BODS	PUD	SE	SM1	SM0	BODSE	ISC01	ISC00	Pages 36, 51, and 67
0x34 (0x54)	MCUSR	–	–	–	–	WDRF	BORF	EXTRF	PORF	Page 45
0x33 (0x53)	TCCR0B	FOC0A	FOC0B	–	–	WGM02	CS02	CS01	CS00	Page 83
0x32 (0x52)	TCNT0	Timer/Counter0								Page 84
0x31 (0x51)	OSCCAL	CAL7	CAL6	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0	Page 30
0x30 (0x50)	TCCR0A	COM0A1	COM0A0	COM0B1	COM0B0	–		WGM01	WGM00	Page 80
0x2F (0x4F)	TCCR1A	COM1A1	COM1A0	COM1B1	COM1B0	–		WGM11	WGM10	Page 108
0x2E (0x4E)	TCCR1B	ICNC1	ICES1	–	WGM13	WGM12	CS12	CS11	CS10	Page 110
0x2D (0x4D)	TCNT1H	Timer/Counter1 – Counter Register High Byte								Page 112
0x2C (0x4C)	TCNT1L	Timer/Counter1 – Counter Register Low Byte								Page 112
0x2B (0x4B)	OCR1AH	Timer/Counter1 – Compare Register A High Byte								Page 112
0x2A (0x4A)	OCR1AL	Timer/Counter1 – Compare Register A Low Byte								Page 112
0x29 (0x49)	OCR1BH	Timer/Counter1 – Compare Register B High Byte								Page 112
0x28 (0x48)	OCR1BL	Timer/Counter1 – Compare Register B Low Byte								Page 112
0x27 (0x47)	DWDR	DWDR[7:0]								Page 152
0x26 (0x46)	CLKPR	CLKPCE	–	–	–	CLKPS3	CLKPS2	CLKPS1	CLKPS0	Page 31
0x25 (0x45)	ICR1H	Timer/Counter1 - Input Capture Register High Byte								Page 113
0x24 (0x44)	ICR1L	Timer/Counter1 - Input Capture Register Low Byte								Page 113
0x23 (0x43)	GTCCR	TSM	–	–	–	–	–	–	PSR10	Page 116
0x22 (0x42)	TCCR1C	FOC1A	FOC1B	–	–	–	–	–	–	Page 111
0x21 (0x41)	WDTCSR	WDIF	WDIE	WDP3	WDCE	WDE	WDP2	WDP1	WDP0	Page 45
0x20 (0x40)	PCMSK1	–	–	–	–	PCINT11	PCINT10	PCINT9	PCINT8	Page 52
0x1F (0x3F)	EEARH	–	–	–	–	–	–	–	EEAR8	Page 20
0x1E (0x3E)	EEARL	EEAR7	EEAR6	EEAR5	EEAR4	EEAR3	EEAR2	EEAR1	EEAR0	Page 21
0x1D (0x3D)	EEDR	EEPROM Data Register								Page 21
0x1C (0x3C)	EECR	–	–	EEPM1	EEPM0	EERIE	EEMPE	EEPE	EERE	Page 21
0x1B (0x3B)	PORTA	PORTA7	PORTA6	PORTA5	PORTA4	PORTA3	PORTA2	PORTA1	PORTA0	Page 67
0x1A (0x3A)	DDRA	DDA7	DDA6	DDA5	DDA4	DDA3	DDA2	DDA1	DDA0	Page 67
0x19 (0x39)	PINA	PINA7	PINA6	PINA5	PINA4	PINA3	PINA2	PINA1	PINA0	Page 68
0x18 (0x38)	PORTB	–	–	–	–	PORTB3	PORTB2	PORTB1	PORTB0	Page 68
0x17 (0x37)	DDRB	–	–	–	–	DDB3	DDB2	DDB1	DDB0	Page 68
0x16 (0x36)	PINB	–	–	–	–	PINB3	PINB2	PINB1	PINB0	Page 68
0x15 (0x35)	GPIOR2	General Purpose I/O Register 2								Page 23
0x14 (0x34)	GPIOR1	General Purpose I/O Register 1								Page 23
0x13 (0x33)	GPIOR0	General Purpose I/O Register 0								Page 23
0x12 (0x32)	PCMSK0	PCINT7	PCINT6	PCINT5	PCINT4	PCINT3	PCINT2	PCINT1	PCINT0	Page 53
0x11 (0x31))	Reserved	–								
0x10 (0x30)	USIBR	USI Buffer Register								Page 125
0x0F (0x2F)	USIDR	USI Data Register								Page 124
0x0E (0x2E)	USISR	USISIF	USIOIF	USIPF	USIDC	USICNT3	USICNT2	USICNT1	USICNT0	Page 125
0x0D (0x2D)	USICR	USISIE	USIOIE	USIWM1	USIWM0	USICS1	USICS0	USICLK	USITC	Page 126
0x0C (0x2C)	TIMSK1	–	–	ICIE1	–	–	OCIE1B	OCIE1A	TOIE1	Page 113
0x0B (0x2B)	TIFR1	–	–	ICF1	–	–	OCF1B	OCF1A	TOV1	Page 114
0x0A (0x2A)	Reserved	–								
0x09 (0x29)	Reserved	–								
0x08 (0x28)	ACSR	ACD	ACBG	ACO	ACI	ACIE	ACIC	ACIS1	ACIS0	Page 130
0x07 (0x27)	ADMUX	REFS1	REFS0	MUX5	MUX4	MUX3	MUX2	MUX1	MUX0	Page 145
0x06 (0x26)	ADCSRA	ADEN	ADSC	ADATE	ADIF	ADIE	ADPS2	ADPS1	ADPS0	Page 147
0x05 (0x25)	ADCH	ADC Data Register High Byte								Page 149
0x04 (0x24)	ADCL	ADC Data Register Low Byte								Page 149
0x03 (0x23)	ADCSRB	BIN	ACME	–	ADLAR	–	ADTS2	ADTS1	ADTS0	Page 131, Page 149
0x02 (0x22)	Reserved	–								
0x01 (0x21)	DIDR0	ADC7D	ADC6D	ADC5D	ADC4D	ADC3D	ADC2D	ADC1D	ADC0D	Page 131, Page 150
0x00 (0x20)	PRR	–	–	–	–	PRTIM1	PRTIM0	PRUSI	PRADC	Page 37

Mnemonics	Operands	Description	Operation	Flags	#Clocks
ROR	Rd	Rotate Right Through Carry	Rd(7)←C,Rd(n)← Rd(n+1),C←Rd(0)	Z,C,N,V	1
ASR	Rd	Arithmetic Shift Right	Rd(n) ← Rd(n+1), n=0..6	Z,C,N,V	1
SWAP	Rd	Swap Nibbles	Rd(3..0)←Rd(7..4),Rd(7..4)←Rd(3..0)	None	1
BSET	s	Flag Set	SREG(s) ← 1	SREG(s)	1
BCLR	s	Flag Clear	SREG(s) ← 0	SREG(s)	1
BST	Rr, b	Bit Store from Register to T	T ← Rr(b)	T	1
BLD	Rd, b	Bit load from T to Register	Rd(b) ← T	None	1
SEC		Set Carry	C ← 1	C	1
CLC		Clear Carry	C ← 0	C	1
SEN		Set Negative Flag	N ← 1	N	1
CLN		Clear Negative Flag	N ← 0	N	1
SEZ		Set Zero Flag	Z ← 1	Z	1
CLZ		Clear Zero Flag	Z ← 0	Z	1
SEI		Global Interrupt Enable	I ← 1	I	1
CLI		Global Interrupt Disable	I ← 0	I	1
SES		Set Signed Test Flag	S ← 1	S	1
CLS		Clear Signed Test Flag	S ← 0	S	1
SEV		Set Twos Complement Overflow.	V ← 1	V	1
CLV		Clear Twos Complement Overflow	V ← 0	V	1
SET		Set T in SREG	T ← 1	T	1
CLT		Clear T in SREG	T ← 0	T	1
SEH		Set Half Carry Flag in SREG	H ← 1	H	1
CLH		Clear Half Carry Flag in SREG	H ← 0	H	1
DATA TRANSFER INSTRUCTIONS					
MOV	Rd, Rr	Move Between Registers	Rd ← Rr	None	1
MOVW	Rd, Rr	Copy Register Word	Rd+1:Rd ← Rr+1:Rr	None	1
LDI	Rd, K	Load Immediate	Rd ← K	None	1
LD	Rd, X	Load Indirect	Rd ← (X)	None	2
LD	Rd, X+	Load Indirect and Post-Inc.	Rd ← (X), X ← X + 1	None	2
LD	Rd, - X	Load Indirect and Pre-Dec.	X ← X - 1, Rd ← (X)	None	2
LD	Rd, Y	Load Indirect	Rd ← (Y)	None	2
LD	Rd, Y+	Load Indirect and Post-Inc.	Rd ← (Y), Y ← Y + 1	None	2
LD	Rd, - Y	Load Indirect and Pre-Dec.	Y ← Y - 1, Rd ← (Y)	None	2
LDD	Rd,Y+q	Load Indirect with Displacement	Rd ← (Y + q)	None	2
LD	Rd, Z	Load Indirect	Rd ← (Z)	None	2
LD	Rd, Z+	Load Indirect and Post-Inc.	Rd ← (Z), Z ← Z+1	None	2
LD	Rd, -Z	Load Indirect and Pre-Dec.	Z ← Z - 1, Rd ← (Z)	None	2
LDD	Rd, Z+q	Load Indirect with Displacement	Rd ← (Z + q)	None	2
LDS	Rd, k	Load Direct from SRAM	Rd ← (k)	None	2
ST	X, Rr	Store Indirect	(X) ← Rr	None	2
ST	X+, Rr	Store Indirect and Post-Inc.	(X) ← Rr, X ← X + 1	None	2
ST	- X, Rr	Store Indirect and Pre-Dec.	X ← X - 1, (X) ← Rr	None	2
ST	Y, Rr	Store Indirect	(Y) ← Rr	None	2
ST	Y+, Rr	Store Indirect and Post-Inc.	(Y) ← Rr, Y ← Y + 1	None	2
ST	- Y, Rr	Store Indirect and Pre-Dec.	Y ← Y - 1, (Y) ← Rr	None	2
STD	Y+q,Rr	Store Indirect with Displacement	(Y + q) ← Rr	None	2
ST	Z, Rr	Store Indirect	(Z) ← Rr	None	2
ST	Z+, Rr	Store Indirect and Post-Inc.	(Z) ← Rr, Z ← Z + 1	None	2
ST	-Z, Rr	Store Indirect and Pre-Dec.	Z ← Z - 1, (Z) ← Rr	None	2
STD	Z+q,Rr	Store Indirect with Displacement	(Z + q) ← Rr	None	2
STS	k, Rr	Store Direct to SRAM	(k) ← Rr	None	2
LPM		Load Program Memory	R0 ← (Z)	None	3
LPM	Rd, Z	Load Program Memory	Rd ← (Z)	None	3
LPM	Rd, Z+	Load Program Memory and Post-Inc	Rd ← (Z), Z ← Z+1	None	3
SPM		Store Program Memory	(z) ← R1:R0	None	
IN	Rd, P	In Port	Rd ← P	None	1
OUT	P, Rr	Out Port	P ← Rr	None	1
PUSH	Rr	Push Register on Stack	STACK ← Rr	None	2
POP	Rd	Pop Register from Stack	Rd ← STACK	None	2
MCU CONTROL INSTRUCTIONS					
NOP		No Operation		None	1
SLEEP		Sleep	(see specific descr. for Sleep function)	None	1
WDR		Watchdog Reset	(see specific descr. for WDR/Timer)	None	1
BREAK		Break	For On-chip Debug Only	None	N/A

6. Ordering Information

6.1 ATtiny24

Speed (MHz)	Power Supply	Ordering Code[1]	Package[2]	Operational Range
10	1.8 - 5.5V	ATtiny24V-10SSU ATtiny24V-10SSUR ATtiny24V-10PU ATtiny24V-10MU ATtiny24V-10MUR	14S1 14S1 14P3 20M1 20M1	Industrial (-40°C to +85°C)[3]
20	2.7 - 5.5V	ATtiny24-20SSU ATtiny24-20SSUR ATtiny24-20PU ATtiny24-20MU ATtiny24-20MUR	14S1 14S1 14P3 20M1 20M1	Industrial (-40°C to +85°C)[3]

Notes: 1. Code indicators:

- U: matte tin
- R: tape & reel

2. All packages are Pb-free, halide-free and fully green and they comply with the European directive for Restriction of Hazardous Substances (RoHS).
3. These devices can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.

Package Type	
14S1	14-lead, 0.150" Wide Body, Plastic Gull Wing Small Outline Package (SOIC)
14P3	14-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
20M1	20-pad, 4 x 4 x 0.8 mm Body, Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)

6.2 ATtiny44

Speed (MHz)	Power Supply	Ordering Code[1]	Package[2]	Operational Range
10	1.8 - 5.5V	ATtiny44V-10SSU ATtiny44V-10SSUR ATtiny44V-10PU ATtiny44V-10MU ATtiny44V-10MUR	14S1 14S1 14P3 20M1 20M1	Industrial (-40°C to +85°C)[3]
20	2.7 - 5.5V	ATtiny44-20SSU ATtiny44-20SSUR ATtiny44-20PU ATtiny44-20MU ATtiny44-20MUR	14S1 14S1 14P3 20M1 20M1	Industrial (-40°C to +85°C)[3]

Notes: 1. Code indicators:

- U: matte tin
- R: tape & reel

2. All packages are Pb-free, halide-free and fully green and they comply with the European directive for Restriction of Hazardous Substances (RoHS).
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Package Type	
14S1	14-lead, 0.150" Wide Body, Plastic Gull Wing Small Outline Package (SOIC)
14P3	14-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
20M1	20-pad, 4 x 4 x 0.8 mm Body, Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)

6.3 ATtiny84

Speed (MHz)	Power Supply	Ordering Code[1]	Package[2]	Operational Range
10	1.8 - 5.5V	ATtiny84V-10SSU ATtiny84V-10SSUR ATtiny84V-10PU ATtiny84V-10MU ATtiny84V-10MUR	14S1 14S1 14P3 20M1 20M1	Industrial (-40°C to +85°C)[3]
20	2.7 - 5.5V	ATtiny84-20SSU ATtiny84-20SSUR ATtiny84-20PU ATtiny84-20MU ATtiny84-20MUR	14S1 14S1 14P3 20M1 20M1	Industrial (-40°C to +85°C)[3]

Notes: 1. Code indicators:

- U: matte tin
- R: tape & reel

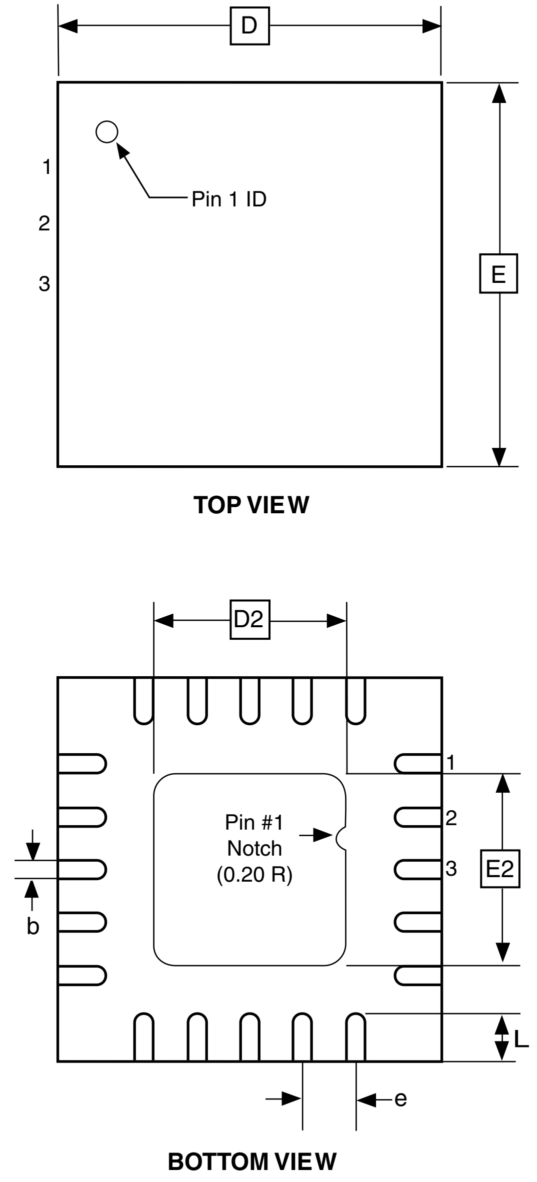
2. All packages are Pb-free, halide-free and fully green and they comply with the European directive for Restriction of Hazardous Substances (RoHS).

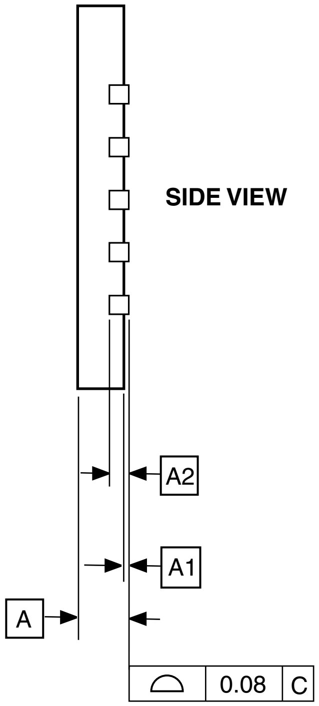
3. These devices can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.

Package Type	
14S1	14-lead, 0.150" Wide Body, Plastic Gull Wing Small Outline Package (SOIC)
14P3	14-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
20M1	20-pad, 4 x 4 x 0.8 mm Body, Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)

7. Packaging Information

7.1 20M1





Note: Reference JEDEC Standard MO-220, Fig. 1 (SAW Singulation) WGGD-5.

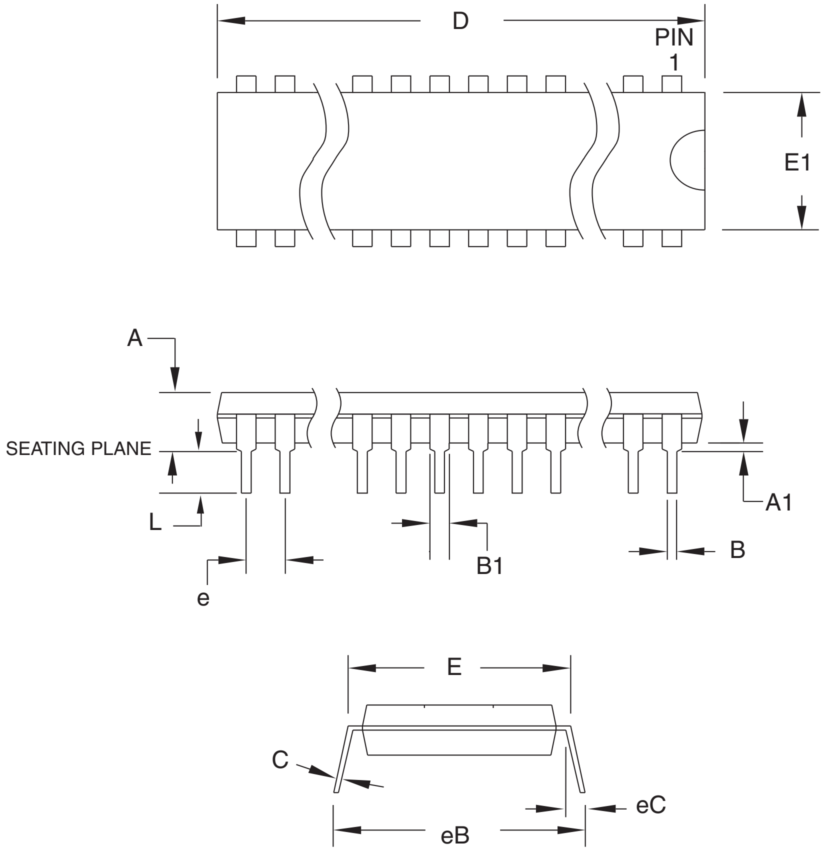
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.70	0.75	0.80	
A1	–	0.01	0.05	
A2		0.20 REF		
b	0.18	0.23	0.30	
D		4.00 BSC		
D2	2.45	2.60	2.75	
E		4.00 BSC		
E2	2.45	2.60	2.75	
e		0.50 BSC		
L	0.35	0.40	0.55	

10/27/04

2325 Orchard Parkway San Jose, CA 95131	**TITLE** **20M1**, 20-pad, 4 x 4 x 0.8 mm Body, Lead Pitch 0.50 mm, 2.6 mm Exposed Pad, Micro Lead Frame Package (MLF)	**DRAWING NO.** 20M1	**REV.** A

7.2 14P3



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	5.334	
A1	0.381	–	–	
D	18.669	–	19.685	Note 2
E	7.620	–	8.255	
E1	6.096	–	7.112	Note 2
B	0.356	–	0.559	
B1	1.143	–	1.778	
L	2.921	–	3.810	
C	0.203	–	0.356	
eB	–	–	10.922	
eC	0.000	–	1.524	
e	2.540 TYP			

Notes:
1. This package conforms to JEDEC reference MS-001, Variation AA.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

11/02/05

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**14P3**, 14-lead (0.300"/7.62 mm Wide) Plastic Dual Inline Package (PDIP)	14P3	A

8. Errata

The revision letters in this section refer to the revision of the corresponding ATtiny24/44/84 device.

8.1 ATtiny24

8.1.1 Rev. D – E

No known errata.

8.1.2 Rev. C

- **Reading EEPROM when system clock frequency is below 900 kHz may not work**

1. **Reading EEPROM when system clock frequency is below 900 kHz may not work**
   Reading data from the EEPROM at system clock frequency below 900 kHz may result in wrong data read.

   Problem Fix/Work around
   Avoid using the EEPROM at clock frequency below 900 kHz.

8.1.3 Rev. B

- **EEPROM read from application code does not work in Lock Bit Mode 3**
- **Reading EEPROM when system clock frequency is below 900 kHz may not work**

1. **EEPROM read from application code does not work in Lock Bit Mode 3**
   When the Memory Lock Bits LB2 and LB1 are programmed to mode 3, EEPROM read does not work from the application code.

   Problem Fix/Work around
   Do not set Lock Bit Protection Mode 3 when the application code needs to read from EEPROM.

2. **Reading EEPROM when system clock frequency is below 900 kHz may not work**
   Reading data from the EEPROM at system clock frequency below 900 kHz may result in wrong data read.

   Problem Fix/Work around
   Avoid using the EEPROM at clock frequency below 900 kHz.

8.1.4 Rev. A

Not sampled.

8.2 ATtiny44

8.2.1 Rev. B – D

No known errata.

8.2.2 Rev. A

- **Reading EEPROM when system clock frequency is below 900 kHz may not work**

1. **Reading EEPROM when system clock frequency is below 900 kHz may not work**
   Reading data from the EEPROM at system clock frequency below 900 kHz may result in wrong data read.

   Problem Fix/Work around
   Avoid using the EEPROM at clock frequency below 900 kHz.

8.3 ATtiny84

8.3.1 Rev. A – B

No known errata.

9. Datasheet Revision History

Please note that the referring page numbers refer to the complete document.

9.1 Rev K. - 10/10

1. Added note for Internal 1.1V Reference in Table 16-4 on page 146.
2. Added tape & reel in Section 24. “Ordering Information” on page 217.
3. Updated last page.

9.2 Rev J. - 08/10

1. Updated Section 6.4 “Clock Output Buffer” on page 30, changed CLKO to CKOUT.
2. Removed text "Not recommended for new design" from cover page.

9.3 Rev I. - 06/10

1. Removed “Preliminary” from cover page.
2. Updated notes in Table 19-16, “High-voltage Serial Programming Instruction Set for ATtiny24/44/84,” on page 171.
3. Added clarification before Table 6-8, “Capacitance for the Low-Frequency Crystal Oscillator,” on page 28.
4. Updated some table notes in Section 20. “Electrical Characteristics” on page 174.

9.4 Rev H. 10/09

1. Updated document template. Re-arranged some sections.
2. Updated “Low-Frequency Crystal Oscillator” with the Table 6-8 on page 28
3. Updated Tables:
   - “Active Clock Domains and Wake-up Sources in Different Sleep Modes” on page 33
   - “DC Characteristics” on page 174
   - “Register Summary” on page 213
4. Updated Register Description:
   - “ADMUX – ADC Multiplexer Selection Register” on page 145
5. Signature Imprint Reading Instructions updated in “Reading Device Signature Imprint Table from Firmware” on page 156.
6. Updated Section:
   - Step 1. on page 164
7. Added Table:
   - “Analog Comparator Characteristics” on page 179
8. Updated Figure:
   - “Active Supply Current vs. frequency (1 - 20 MHz)” on page 187
9. Updated Figure 21-30 on page 201 and Figure 21-33 on page 202 under “Pin Threshold and Hysteresis”.
10. Changed ATtiny24/44 device status to “Not Recommended for New Designs. Use: ATtiny24A/44A”.

9.5 Rev G. 01/08

1. Updated sections:
   - “Features” on page 1
   - “RESET” on page 3
   - “Overview” on page 4
   - “About” on page 6
   - “SPH and SPL — Stack Pointer Register” on page 11
   - “Atomic Byte Programming” on page 17
   - “Write” on page 17
   - “Clock Sources” on page 25
   - “Default Clock Source” on page 30
   - “Sleep Modes” on page 33
   - “Software BOD Disable” on page 34
   - “External Interrupts” on page 49
   - “USIBR – USI Data Buffer” on page 125
   - “USIDR – USI Data Register” on page 124
   - “DIDR0 – Digital Input Disable Register 0” on page 131
   - “Features” on page 132
   - “Prescaling and Conversion Timing” on page 135
   - “Temperature Measurement” on page 144
   - “ADMUX – ADC Multiplexer Selection Register” on page 145
   - “Limitations of debugWIRE” on page 152
   - “Reading Lock, Fuse and Signature Data from Software” on page 155
   - “Device Signature Imprint Table” on page 161
   - “Enter High-voltage Serial Programming Mode” on page 168
   - “Absolute Maximum Ratings*” on page 174
   - “DC Characteristics” on page 174
   - “Speed” on page 175
   - “Clock Characteristics” on page 176
   - “Accuracy of Calibrated Internal RC Oscillator” on page 176
   - “System and Reset Characteristics” on page 177
   - “Supply Current of I/O Modules” on page 185
   - “ATtiny24” on page 223
   - “ATtiny44” on page 224
   - “ATtiny84” on page 225
2. Updated bit definitions in sections:
   - “MCUCR – MCU Control Register” on page 36
   - “MCUCR – MCU Control Register” on page 51
   - “MCUCR – MCU Control Register” on page 67
   - “PINA – Port A Input Pins” on page 68

- “Start-up Times for the Crystal Oscillator Clock Selection” on page 29
- “Start-up Times for the Internal Calibrated RC Oscillator Clock Selection” on page 27
- “Start-up Times for the External Clock Selection” on page 26
- “Start-up Times for the 128 kHz Internal Oscillator” on page 27
- “Active Clock Domains and Wake-up Sources in Different Sleep Modes” on page 33
- “Watchdog Timer Prescale Select” on page 47
- “Reset and Interrupt Vectors” on page 48
- “Overriding Signals for Alternate Functions in PA7:PA5” on page 63
- “Overriding Signals for Alternate Functions in PA4:PA2” on page 64
- “Overriding Signals for Alternate Functions in PA1:PA0” on page 64
- “Port B Pins Alternate Functions” on page 65
- “Overriding Signals for Alternate Functions in PB3:PB2” on page 66
- “Overriding Signals for Alternate Functions in PB1:PB0” on page 67
- “Waveform Generation Modes” on page 110
- “ADC Conversion Time” on page 138
- “Temperature vs. Sensor Output Voltage (Typical Case)” on page 144
- “DC Characteristics. T_A = -40°C to +85°C” on page 174
- “Calibration Accuracy of Internal RC Oscillator” on page 176
- “Reset, Brown-out, and Internal Voltage Characteristics” on page 177
- “VBOT vs. BODLEVEL Fuse Coding” on page 179
- “ADC Characteristics, Single Ended Channels. T = -40°C to +85°C” on page 180
- “ADC Characteristics, Differential Channels (Bipolar Mode), T_A = -40°C to +85°C” on page 182
- “Serial Programming Characteristics, T_A = -40°C to +85°C, V_{CC} = 1.8 - 5.5V (Unless Otherwise Noted)” on page 183
- “High-voltage Serial Programming Characteristics T_A = 25°C, V_{CC} = 5V (Unless otherwise noted)” on page 184

6. Updated code examples in sections:
   - “Write” on page 17
   - “SPI Master Operation Example” on page 119
7. Updated “Ordering Information” in:
   - “ATtiny84” on page 219

9.6 Rev F. 02/07

1. Updated Figure 1-1 on page 2, Figure 8-7 on page 43, Figure 20-6 on page 184.
2. Updated Table 9-1 on page 48, Table 10-7 on page 65, Table 11-2 on page 80, Table 11-3 on page 81, Table 11-5 on page 81, Table 11-6 on page 82, Table 11-7 on page 82, Table 11-8 on page 83, Table 20-11 on page 182, Table 20-13 on page 184.
3. Updated table references in “TCCR0A – Timer/Counter Control Register A” on page 80.
4. Updated Port B, Bit 0 functions in “Alternate Functions of Port B” on page 65.
5. Updated WDTCR bit name to WDTCSR in assembly code examples.

6. Updated bit5 name in “TIFR1 – Timer/Counter Interrupt Flag Register 1” on page 114.
7. Updated bit5 in “TIFR1 – Timer/Counter Interrupt Flag Register 1” on page 114.
8. Updated “SPI Master Operation Example” on page 119.
9. Updated step 5 in “Enter High-voltage Serial Programming Mode” on page 168.

9.7 Rev E. 09/06

1. All characterization data moved to “Electrical Characteristics” on page 174.
2. All Register Descriptions gathered up in separate sections at the end of each chapter.
3. Updated “System Control and Reset” on page 39.
4. Updated Table 11-3 on page 81, Table 11-6 on page 82, Table 11-8 on page 83, Table 12-3 on page 109 and Table 12-5 on page 110.
5. Updated “Fast PWM Mode” on page 97.
6. Updated Figure 12-7 on page 98 and Figure 16-1 on page 133.
7. Updated “Analog Comparator Multiplexed Input” on page 129.
8. Added note in Table 19-12 on page 165.
9. Updated “Electrical Characteristics” on page 174.
10. Updated “Typical Characteristics” on page 185.

9.8 Rev D. 08/06

1. Updated “Calibrated Internal 8 MHz Oscillator” on page 26.
2. Updated “OSCCAL – Oscillator Calibration Register” on page 30.
3. Added Table 20-2 on page 176.
4. Updated code examples in “SPI Master Operation Example” on page 119.
5. Updated code examples in “SPI Slave Operation Example” on page 121.
6. Updated “Signature Bytes” on page 162.

9.9 Rev C. 07/06

1. Updated Features in “USI – Universal Serial Interface” on page 117.
2. Added “Clock speed considerations” on page 123.
3. Updated Bit description in “ADMUX – ADC Multiplexer Selection Register” on page 145.
4. Added note to Table 18-1 on page 157.

9.10 Rev B. 05/06

1. Updated “Default Clock Source” on page 30
2. Updated “Power Reduction Register” on page 35.
3. Updated Table 20-4 on page 177, Table 9-4 on page 42, Table 16-3 on page 145, Table 19-5 on page 161, Table 19-12 on page 165, Table 19-16 on page 171, Table 20-11 on page 182.
4. Updated Features in “Analog to Digital Converter” on page 132.
5. Updated Operation in “Analog to Digital Converter” on page 132.
6. Updated “Temperature Measurement” on page 144.

7. Updated DC Characteristics in “Electrical Characteristics” on page 174.
8. Updated “Typical Characteristics” on page 185.
9. Updated “Errata” on page 223.

9.11 Rev A. 12/05

Initial revision.

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