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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	AVR
Core Size	8-Bit
Speed	20MHz
Connectivity	USI
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	12
Program Memory Size	8KB (4K x 16)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	14-SOIC (0.154", 3.90mm Width)
Supplier Device Package	14-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/attiny84-20ssur

1. Pin Configurations

Figure 1-1. Pinout ATtiny24/44/84



1.1 Pin Descriptions

1.1.1 VCC

Supply voltage.

1.1.2 GND

Ground.

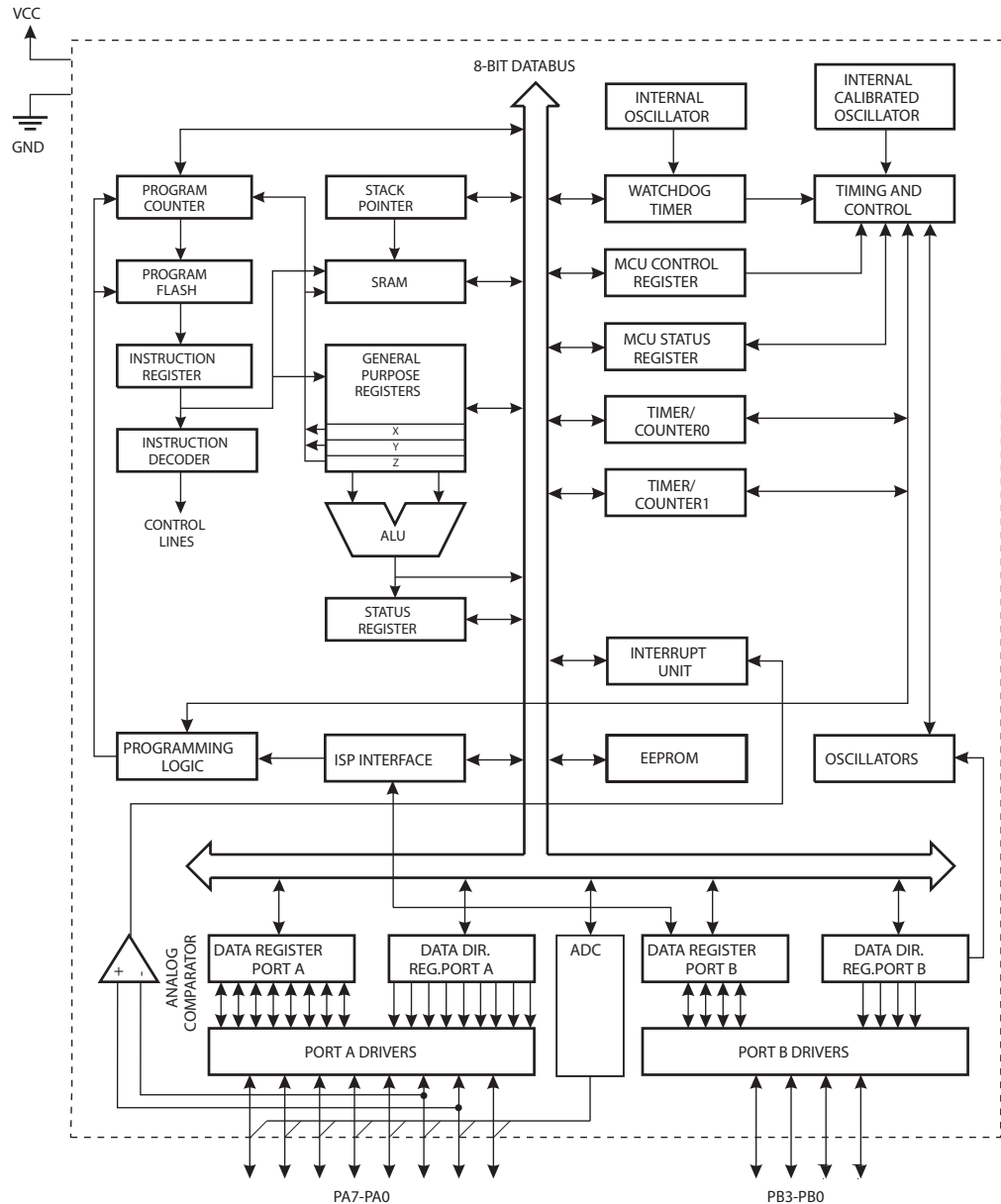
1.1.3 Port B (PB3:PB0)

Port B is a 4-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability except PB3 which has the RESET capability. To use pin PB3 as an I/O pin, instead of RESET pin, program ('0') RSTDISBL fuse. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

2. Overview

ATtiny24/44/84 is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATtiny24/44/84 achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

Figure 2-1. Block Diagram



The AVR core combines a rich instruction set with 32 general purpose working registers. All 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

3. About

3.1 Resources

A comprehensive set of drivers, application notes, data sheets and descriptions on development tools are available for download at <http://www.atmel.com/avr>.

3.2 Code Examples

This documentation contains simple code examples that briefly show how to use various parts of the device. These code examples assume that the part specific header file is included before compilation. Be aware that not all C compiler vendors include bit definitions in the header files and interrupt handling in C is compiler dependent. Please confirm with the C compiler documentation for more details.

For I/O Registers located in the extended I/O map, "IN", "OUT", "SBIS", "SBIC", "CBI", and "SBI" instructions must be replaced with instructions that allow access to extended I/O. Typically, this means "LDS" and "STS" combined with "SBRS", "SBRC", "SBR", and "CBR". Note that not all AVR devices include an extended I/O map.

3.3 Data Retention

Reliability Qualification results show that the projected data retention failure rate is much less than 1 PPM over 20 years at 85°C or 100 years at 25°C.

3.4 Disclaimer

Typical values contained in this datasheet are based on simulations and characterization of other AVR microcontrollers manufactured on the same process technology.

4. Register Summary

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
0x3F (0x5F)	SREG	I	T	H	S	V	N	Z	C	Page 8
0x3E (0x5E)	SPH	–	–	–	–	–	–	SP9	SP8	Page 11
0x3D (0x5D)	SPL	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	Page 11
0x3C (0x5C)	OCR0B	Timer/Counter0 – Output Compare Register B								Page 85
0x3B (0x5B)	GIMSK	–	INT0	PCIE1	PCIE0	–	–	–	–	Page 51
0x3A (0x5A)	GIFR	–	INTF0	PCIF1	PCIF0	–	–	–	–	Page 52
0x39 (0x59)	TIMSK0	–	–	–	–	–	OCIE0B	OCIE0A	TOIE0	Page 85
0x38 (0x58)	TIFR0	–	–	–	–	–	OCF0B	OCF0A	TOV0	Page 85
0x37 (0x57)	SPMCSR	–	–	RSIG	CTPB	RFLB	PGWRT	PGERS	SPMEN	Page 157
0x36 (0x56)	OCR0A	Timer/Counter0 – Output Compare Register A								Page 84
0x35 (0x55)	MCUCR	BODS	PUD	SE	SM1	SM0	BODSE	ISC01	ISC00	Pages 36, 51, and 67
0x34 (0x54)	MCUSR	–	–	–	–	WDRF	BORF	EXTRF	PORF	Page 45
0x33 (0x53)	TCCR0B	FOC0A	FOC0B	–	–	WGM02	CS02	CS01	CS00	Page 83
0x32 (0x52)	TCNT0	Timer/Counter0								Page 84
0x31 (0x51)	OSCCAL	CAL7	CAL6	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0	Page 30
0x30 (0x50)	TCCR0A	COM0A1	COM0A0	COM0B1	COM0B0	–	–	WGM01	WGM00	Page 80
0x2F (0x4F)	TCCR1A	COM1A1	COM1A0	COM1B1	COM1B0	–	–	WGM11	WGM10	Page 108
0x2E (0x4E)	TCCR1B	ICNC1	ICES1	–	WGM13	WGM12	CS12	CS11	CS10	Page 110
0x2D (0x4D)	TCNT1H	Timer/Counter1 – Counter Register High Byte								Page 112
0x2C (0x4C)	TCNT1L	Timer/Counter1 – Counter Register Low Byte								Page 112
0x2B (0x4B)	OCR1AH	Timer/Counter1 – Compare Register A High Byte								Page 112
0x2A (0x4A)	OCR1AL	Timer/Counter1 – Compare Register A Low Byte								Page 112
0x29 (0x49)	OCR1BH	Timer/Counter1 – Compare Register B High Byte								Page 112
0x28 (0x48)	OCR1BL	Timer/Counter1 – Compare Register B Low Byte								Page 112
0x27 (0x47)	DWDR	DWDR[7:0]								Page 152
0x26 (0x46)	CLKPR	CLKPCE	–	–	–	CLKPS3	CLKPS2	CLKPS1	CLKPS0	Page 31
0x25 (0x45)	ICR1H	Timer/Counter1 - Input Capture Register High Byte								Page 113
0x24 (0x44)	ICR1L	Timer/Counter1 - Input Capture Register Low Byte								Page 113
0x23 (0x43)	GTCCR	TSM	–	–	–	–	–	–	PSR10	Page 116
0x22 (0x42)	TCCR1C	FOC1A	FOC1B	–	–	–	–	–	–	Page 111
0x21 (0x41)	WDTCR	WDIF	WDIE	WDP3	WDCE	WDE	WDP2	WDP1	WDP0	Page 45
0x20 (0x40)	PCMSK1	–	–	–	–	PCINT11	PCINT10	PCINT9	PCINT8	Page 52
0x1F (0x3F)	EEARH	–	–	–	–	–	–	–	EEAR8	Page 20
0x1E (0x3E)	EEARL	EEAR7	EEAR6	EEAR5	EEAR4	EEAR3	EEAR2	EEAR1	EEAR0	Page 21
0x1D (0x3D)	EEDR	EEPROM Data Register								Page 21
0x1C (0x3C)	EEDR	–	–	EEDR1	EEDR0	EEDR7	EEDR6	EEDR5	EEDR4	Page 21
0x1B (0x3B)	PORTA	PORTA7	PORTA6	PORTA5	PORTA4	PORTA3	PORTA2	PORTA1	PORTA0	Page 67
0x1A (0x3A)	DDRA	DDA7	DDA6	DDA5	DDA4	DDA3	DDA2	DDA1	DDA0	Page 67
0x19 (0x39)	PINA	PINA7	PINA6	PINA5	PINA4	PINA3	PINA2	PINA1	PINA0	Page 68
0x18 (0x38)	PORTB	–	–	–	–	PORTB3	PORTB2	PORTB1	PORTB0	Page 68
0x17 (0x37)	DDRB	–	–	–	–	DDRB3	DDRB2	DDRB1	DDRB0	Page 68
0x16 (0x36)	PINB	–	–	–	–	PINB3	PINB2	PINB1	PINB0	Page 68
0x15 (0x35)	GPOR2	General Purpose I/O Register 2								Page 23
0x14 (0x34)	GPOR1	General Purpose I/O Register 1								Page 23
0x13 (0x33)	GPOR0	General Purpose I/O Register 0								Page 23
0x12 (0x32)	PCMSK0	PCINT7	PCINT6	PCINT5	PCINT4	PCINT3	PCINT2	PCINT1	PCINT0	Page 53
0x11 (0x31)	Reserved	–								
0x10 (0x30)	USIBR	USI Buffer Register								Page 125
0x0F (0x2F)	USIDR	USI Data Register								Page 124
0x0E (0x2E)	USISR	USISIF	USIOIF	USIPF	USIDC	USICNT3	USICNT2	USICNT1	USICNT0	Page 125
0x0D (0x2D)	USICR	USISIE	USIOIE	USIWM1	USIWM0	USICS1	USICS0	USICLK	USITC	Page 126
0x0C (0x2C)	TIMSK1	–	–	ICIE1	–	–	OCIE1B	OCIE1A	TOIE1	Page 113
0x0B (0x2B)	TIFR1	–	–	ICF1	–	–	OCF1B	OCF1A	TOV1	Page 114
0x0A (0x2A)	Reserved	–								
0x09 (0x29)	Reserved	–								
0x08 (0x28)	ACSR	ACD	ACBG	ACO	ACI	ACIE	ACIC	ACIS1	ACIS0	Page 130
0x07 (0x27)	ADMUX	REFS1	REFS0	MUX5	MUX4	MUX3	MUX2	MUX1	MUX0	Page 145
0x06 (0x26)	ADCSRA	ADEN	ADSC	ADATE	ADIF	ADIE	ADPS2	ADPS1	ADPS0	Page 147
0x05 (0x25)	ADCH	ADC Data Register High Byte								Page 149
0x04 (0x24)	ADCL	ADC Data Register Low Byte								Page 149
0x03 (0x23)	ADCSRB	BIN	ACME	–	ADLAR	–	ADTS2	ADTS1	ADTS0	Page 131, Page 149
0x02 (0x22)	Reserved	–								
0x01 (0x21)	DIDR0	ADC7D	ADC6D	ADC5D	ADC4D	ADC3D	ADC2D	ADC1D	ADC0D	Page 131, Page 150
0x00 (0x20)	PRR	–	–	–	–	PRTIM1	PRTIM0	PRUSI	PRADC	Page 37



- Note:
1. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.
 2. I/O Registers within the address range 0x00 - 0x1F are directly bit-accessible using the SBI and CBI instructions. In these registers, the value of single bits can be checked by using the SBIS and SBIC instructions.
 3. Some of the Status Flags are cleared by writing a logical one to them. Note that, unlike most other AVR's, the CBI and SBI instructions will only operation the specified bit, and can therefore be used on registers containing such Status Flags. The CBI and SBI instructions work with registers 0x00 to 0x1F only.

5. Instruction Set Summary

Mnemonics	Operands	Description	Operation	Flags	#Clocks
ARITHMETIC AND LOGIC INSTRUCTIONS					
ADD	Rd, Rr	Add two Registers	$Rd \leftarrow Rd + Rr$	Z,C,N,V,H	1
ADC	Rd, Rr	Add with Carry two Registers	$Rd \leftarrow Rd + Rr + C$	Z,C,N,V,H	1
ADIW	Rd,K	Add Immediate to Word	$Rdh:Rdl \leftarrow Rdh:Rdl + K$	Z,C,N,V,S	2
SUB	Rd, Rr	Subtract two Registers	$Rd \leftarrow Rd - Rr$	Z,C,N,V,H	1
SUBI	Rd, K	Subtract Constant from Register	$Rd \leftarrow Rd - K$	Z,C,N,V,H	1
SBC	Rd, Rr	Subtract with Carry two Registers	$Rd \leftarrow Rd - Rr - C$	Z,C,N,V,H	1
SBCI	Rd, K	Subtract with Carry Constant from Reg.	$Rd \leftarrow Rd - K - C$	Z,C,N,V,H	1
SBIW	Rd,K	Subtract Immediate from Word	$Rdh:Rdl \leftarrow Rdh:Rdl - K$	Z,C,N,V,S	2
AND	Rd, Rr	Logical AND Registers	$Rd \leftarrow Rd \bullet Rr$	Z,N,V	1
ANDI	Rd, K	Logical AND Register and Constant	$Rd \leftarrow Rd \bullet K$	Z,N,V	1
OR	Rd, Rr	Logical OR Registers	$Rd \leftarrow Rd \vee Rr$	Z,N,V	1
ORI	Rd, K	Logical OR Register and Constant	$Rd \leftarrow Rd \vee K$	Z,N,V	1
EOR	Rd, Rr	Exclusive OR Registers	$Rd \leftarrow Rd \oplus Rr$	Z,N,V	1
COM	Rd	One's Complement	$Rd \leftarrow 0xFF - Rd$	Z,C,N,V	1
NEG	Rd	Two's Complement	$Rd \leftarrow 0x00 - Rd$	Z,C,N,V,H	1
SBR	Rd,K	Set Bit(s) in Register	$Rd \leftarrow Rd \vee K$	Z,N,V	1
CBR	Rd,K	Clear Bit(s) in Register	$Rd \leftarrow Rd \bullet (0xFF - K)$	Z,N,V	1
INC	Rd	Increment	$Rd \leftarrow Rd + 1$	Z,N,V	1
DEC	Rd	Decrement	$Rd \leftarrow Rd - 1$	Z,N,V	1
TST	Rd	Test for Zero or Minus	$Rd \leftarrow Rd \bullet Rd$	Z,N,V	1
CLR	Rd	Clear Register	$Rd \leftarrow Rd \oplus Rd$	Z,N,V	1
SER	Rd	Set Register	$Rd \leftarrow 0xFF$	None	1
BRANCH INSTRUCTIONS					
RJMP	k	Relative Jump	$PC \leftarrow PC + k + 1$	None	2
IJMP		Indirect Jump to (Z)	$PC \leftarrow Z$	None	2
RCALL	k	Relative Subroutine Call	$PC \leftarrow PC + k + 1$	None	3
ICALL		Indirect Call to (Z)	$PC \leftarrow Z$	None	3
RET		Subroutine Return	$PC \leftarrow STACK$	None	4
RETI		Interrupt Return	$PC \leftarrow STACK$	I	4
CPSE	Rd,Rr	Compare, Skip if Equal	if (Rd = Rr) $PC \leftarrow PC + 2$ or 3	None	1/2/3
CP	Rd,Rr	Compare	$Rd - Rr$	Z, N, V, C, H	1
CPC	Rd,Rr	Compare with Carry	$Rd - Rr - C$	Z, N, V, C, H	1
CPI	Rd,K	Compare Register with Immediate	$Rd - K$	Z, N, V, C, H	1
SBRC	Rr, b	Skip if Bit in Register Cleared	if (Rr(b)=0) $PC \leftarrow PC + 2$ or 3	None	1/2/3
SBRS	Rr, b	Skip if Bit in Register is Set	if (Rr(b)=1) $PC \leftarrow PC + 2$ or 3	None	1/2/3
SBIC	P, b	Skip if Bit in I/O Register Cleared	if (P(b)=0) $PC \leftarrow PC + 2$ or 3	None	1/2/3
SBIS	P, b	Skip if Bit in I/O Register is Set	if (P(b)=1) $PC \leftarrow PC + 2$ or 3	None	1/2/3
BRBS	s, k	Branch if Status Flag Set	if (SREG(s) = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRBC	s, k	Branch if Status Flag Cleared	if (SREG(s) = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BREQ	k	Branch if Equal	if (Z = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRNE	k	Branch if Not Equal	if (Z = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BRCS	k	Branch if Carry Set	if (C = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRCC	k	Branch if Carry Cleared	if (C = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BRSH	k	Branch if Same or Higher	if (C = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BRLO	k	Branch if Lower	if (C = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRMI	k	Branch if Minus	if (N = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRPL	k	Branch if Plus	if (N = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BRGE	k	Branch if Greater or Equal, Signed	if (N \oplus V = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BRLT	k	Branch if Less Than Zero, Signed	if (N \oplus V = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRHS	k	Branch if Half Carry Flag Set	if (H = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRHC	k	Branch if Half Carry Flag Cleared	if (H = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BRTS	k	Branch if T Flag Set	if (T = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRTC	k	Branch if T Flag Cleared	if (T = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BRVS	k	Branch if Overflow Flag is Set	if (V = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRVC	k	Branch if Overflow Flag is Cleared	if (V = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BRIE	k	Branch if Interrupt Enabled	if (I = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRID	k	Branch if Interrupt Disabled	if (I = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BIT AND BIT-TEST INSTRUCTIONS					
SBI	P,b	Set Bit in I/O Register	$I/O(P,b) \leftarrow 1$	None	2
CBI	P,b	Clear Bit in I/O Register	$I/O(P,b) \leftarrow 0$	None	2
LSL	Rd	Logical Shift Left	$Rd(n+1) \leftarrow Rd(n), Rd(0) \leftarrow 0$	Z,C,N,V	1
LSR	Rd	Logical Shift Right	$Rd(n) \leftarrow Rd(n+1), Rd(7) \leftarrow 0$	Z,C,N,V	1
ROL	Rd	Rotate Left Through Carry	$Rd(0) \leftarrow C, Rd(n+1) \leftarrow Rd(n), C \leftarrow Rd(7)$	Z,C,N,V	1

Mnemonics	Operands	Description	Operation	Flags	#Clocks
ROR	Rd	Rotate Right Through Carry	$Rd(7) \leftarrow C, Rd(n) \leftarrow Rd(n+1), C \leftarrow Rd(0)$	Z,C,N,V	1
ASR	Rd	Arithmetic Shift Right	$Rd(n) \leftarrow Rd(n+1), n=0..6$	Z,C,N,V	1
SWAP	Rd	Swap Nibbles	$Rd(3..0) \leftarrow Rd(7..4), Rd(7..4) \leftarrow Rd(3..0)$	None	1
BSET	s	Flag Set	$SREG(s) \leftarrow 1$	SREG(s)	1
BCLR	s	Flag Clear	$SREG(s) \leftarrow 0$	SREG(s)	1
BST	Rr, b	Bit Store from Register to T	$T \leftarrow Rr(b)$	T	1
BLD	Rd, b	Bit load from T to Register	$Rd(b) \leftarrow T$	None	1
SEC		Set Carry	$C \leftarrow 1$	C	1
CLC		Clear Carry	$C \leftarrow 0$	C	1
SEN		Set Negative Flag	$N \leftarrow 1$	N	1
CLN		Clear Negative Flag	$N \leftarrow 0$	N	1
SEZ		Set Zero Flag	$Z \leftarrow 1$	Z	1
CLZ		Clear Zero Flag	$Z \leftarrow 0$	Z	1
SEI		Global Interrupt Enable	$I \leftarrow 1$	I	1
CLI		Global Interrupt Disable	$I \leftarrow 0$	I	1
SES		Set Signed Test Flag	$S \leftarrow 1$	S	1
CLS		Clear Signed Test Flag	$S \leftarrow 0$	S	1
SEV		Set Twos Complement Overflow	$V \leftarrow 1$	V	1
CLV		Clear Twos Complement Overflow	$V \leftarrow 0$	V	1
SET		Set T in SREG	$T \leftarrow 1$	T	1
CLT		Clear T in SREG	$T \leftarrow 0$	T	1
SEH		Set Half Carry Flag in SREG	$H \leftarrow 1$	H	1
CLH		Clear Half Carry Flag in SREG	$H \leftarrow 0$	H	1
DATA TRANSFER INSTRUCTIONS					
MOV	Rd, Rr	Move Between Registers	$Rd \leftarrow Rr$	None	1
MOVW	Rd, Rr	Copy Register Word	$Rd+1:Rd \leftarrow Rr+1:Rr$	None	1
LDI	Rd, K	Load Immediate	$Rd \leftarrow K$	None	1
LD	Rd, X	Load Indirect	$Rd \leftarrow (X)$	None	2
LD	Rd, X+	Load Indirect and Post-Inc.	$Rd \leftarrow (X), X \leftarrow X + 1$	None	2
LD	Rd, -X	Load Indirect and Pre-Dec.	$X \leftarrow X - 1, Rd \leftarrow (X)$	None	2
LD	Rd, Y	Load Indirect	$Rd \leftarrow (Y)$	None	2
LD	Rd, Y+	Load Indirect and Post-Inc.	$Rd \leftarrow (Y), Y \leftarrow Y + 1$	None	2
LD	Rd, -Y	Load Indirect and Pre-Dec.	$Y \leftarrow Y - 1, Rd \leftarrow (Y)$	None	2
LDD	Rd, Y+q	Load Indirect with Displacement	$Rd \leftarrow (Y + q)$	None	2
LD	Rd, Z	Load Indirect	$Rd \leftarrow (Z)$	None	2
LD	Rd, Z+	Load Indirect and Post-Inc.	$Rd \leftarrow (Z), Z \leftarrow Z + 1$	None	2
LD	Rd, -Z	Load Indirect and Pre-Dec.	$Z \leftarrow Z - 1, Rd \leftarrow (Z)$	None	2
LDD	Rd, Z+q	Load Indirect with Displacement	$Rd \leftarrow (Z + q)$	None	2
LDS	Rd, k	Load Direct from SRAM	$Rd \leftarrow (k)$	None	2
ST	X, Rr	Store Indirect	$(X) \leftarrow Rr$	None	2
ST	X+, Rr	Store Indirect and Post-Inc.	$(X) \leftarrow Rr, X \leftarrow X + 1$	None	2
ST	-X, Rr	Store Indirect and Pre-Dec.	$X \leftarrow X - 1, (X) \leftarrow Rr$	None	2
ST	Y, Rr	Store Indirect	$(Y) \leftarrow Rr$	None	2
ST	Y+, Rr	Store Indirect and Post-Inc.	$(Y) \leftarrow Rr, Y \leftarrow Y + 1$	None	2
ST	-Y, Rr	Store Indirect and Pre-Dec.	$Y \leftarrow Y - 1, (Y) \leftarrow Rr$	None	2
STD	Y+q, Rr	Store Indirect with Displacement	$(Y + q) \leftarrow Rr$	None	2
ST	Z, Rr	Store Indirect	$(Z) \leftarrow Rr$	None	2
ST	Z+, Rr	Store Indirect and Post-Inc.	$(Z) \leftarrow Rr, Z \leftarrow Z + 1$	None	2
ST	-Z, Rr	Store Indirect and Pre-Dec.	$Z \leftarrow Z - 1, (Z) \leftarrow Rr$	None	2
STD	Z+q, Rr	Store Indirect with Displacement	$(Z + q) \leftarrow Rr$	None	2
STS	k, Rr	Store Direct to SRAM	$(k) \leftarrow Rr$	None	2
LPM		Load Program Memory	$R0 \leftarrow (Z)$	None	3
LPM	Rd, Z	Load Program Memory	$Rd \leftarrow (Z)$	None	3
LPM	Rd, Z+	Load Program Memory and Post-Inc	$Rd \leftarrow (Z), Z \leftarrow Z + 1$	None	3
SPM		Store Program Memory	$(z) \leftarrow R1:R0$	None	
IN	Rd, P	In Port	$Rd \leftarrow P$	None	1
OUT	P, Rr	Out Port	$P \leftarrow Rr$	None	1
PUSH	Rr	Push Register on Stack	$STACK \leftarrow Rr$	None	2
POP	Rd	Pop Register from Stack	$Rd \leftarrow STACK$	None	2
MCU CONTROL INSTRUCTIONS					
NOP		No Operation		None	1
SLEEP		Sleep	(see specific descr. for Sleep function)	None	1
WDR		Watchdog Reset	(see specific descr. for WDR/Timer)	None	1
BREAK		Break	For On-chip Debug Only	None	N/A

6. Ordering Information

6.1 ATtiny24

Speed (MHz)	Power Supply	Ordering Code ⁽¹⁾	Package ⁽²⁾	Operational Range
10	1.8 - 5.5V	ATtiny24V-10SSU ATtiny24V-10SSUR ATtiny24V-10PU ATtiny24V-10MU ATtiny24V-10MUR	14S1 14S1 14P3 20M1 20M1	Industrial (-40°C to +85°C) ⁽³⁾
20	2.7 - 5.5V	ATtiny24-20SSU ATtiny24-20SSUR ATtiny24-20PU ATtiny24-20MU ATtiny24-20MUR	14S1 14S1 14P3 20M1 20M1	Industrial (-40°C to +85°C) ⁽³⁾

Notes: 1. Code indicators:

- U: matte tin
- R: tape & reel

2. All packages are Pb-free, halide-free and fully green and they comply with the European directive for Restriction of Hazardous Substances (RoHS).
3. These devices can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.

Package Type	
14S1	14-lead, 0.150" Wide Body, Plastic Gull Wing Small Outline Package (SOIC)
14P3	14-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
20M1	20-pad, 4 x 4 x 0.8 mm Body, Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)



6.2 ATtiny44

Speed (MHz)	Power Supply	Ordering Code ⁽¹⁾	Package ⁽²⁾	Operational Range
10	1.8 - 5.5V	ATtiny44V-10SSU ATtiny44V-10SSUR ATtiny44V-10PU ATtiny44V-10MU ATtiny44V-10MUR	14S1 14S1 14P3 20M1 20M1	Industrial (-40°C to +85°C) ⁽³⁾
20	2.7 - 5.5V	ATtiny44-20SSU ATtiny44-20SSUR ATtiny44-20PU ATtiny44-20MU ATtiny44-20MUR	14S1 14S1 14P3 20M1 20M1	Industrial (-40°C to +85°C) ⁽³⁾

Notes: 1. Code indicators:

- U: matte tin
- R: tape & reel

2. All packages are Pb-free, halide-free and fully green and they comply with the European directive for Restriction of Hazardous Substances (RoHS).
3. These devices can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.

Package Type	
14S1	14-lead, 0.150" Wide Body, Plastic Gull Wing Small Outline Package (SOIC)
14P3	14-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
20M1	20-pad, 4 x 4 x 0.8 mm Body, Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)

6.3 ATtiny84

Speed (MHz)	Power Supply	Ordering Code ⁽¹⁾	Package ⁽²⁾	Operational Range
10	1.8 - 5.5V	ATtiny84V-10SSU ATtiny84V-10SSUR ATtiny84V-10PU ATtiny84V-10MU ATtiny84V-10MUR	14S1 14S1 14P3 20M1 20M1	Industrial (-40°C to +85°C) ⁽³⁾
20	2.7 - 5.5V	ATtiny84-20SSU ATtiny84-20SSUR ATtiny84-20PU ATtiny84-20MU ATtiny84-20MUR	14S1 14S1 14P3 20M1 20M1	Industrial (-40°C to +85°C) ⁽³⁾

Notes: 1. Code indicators:

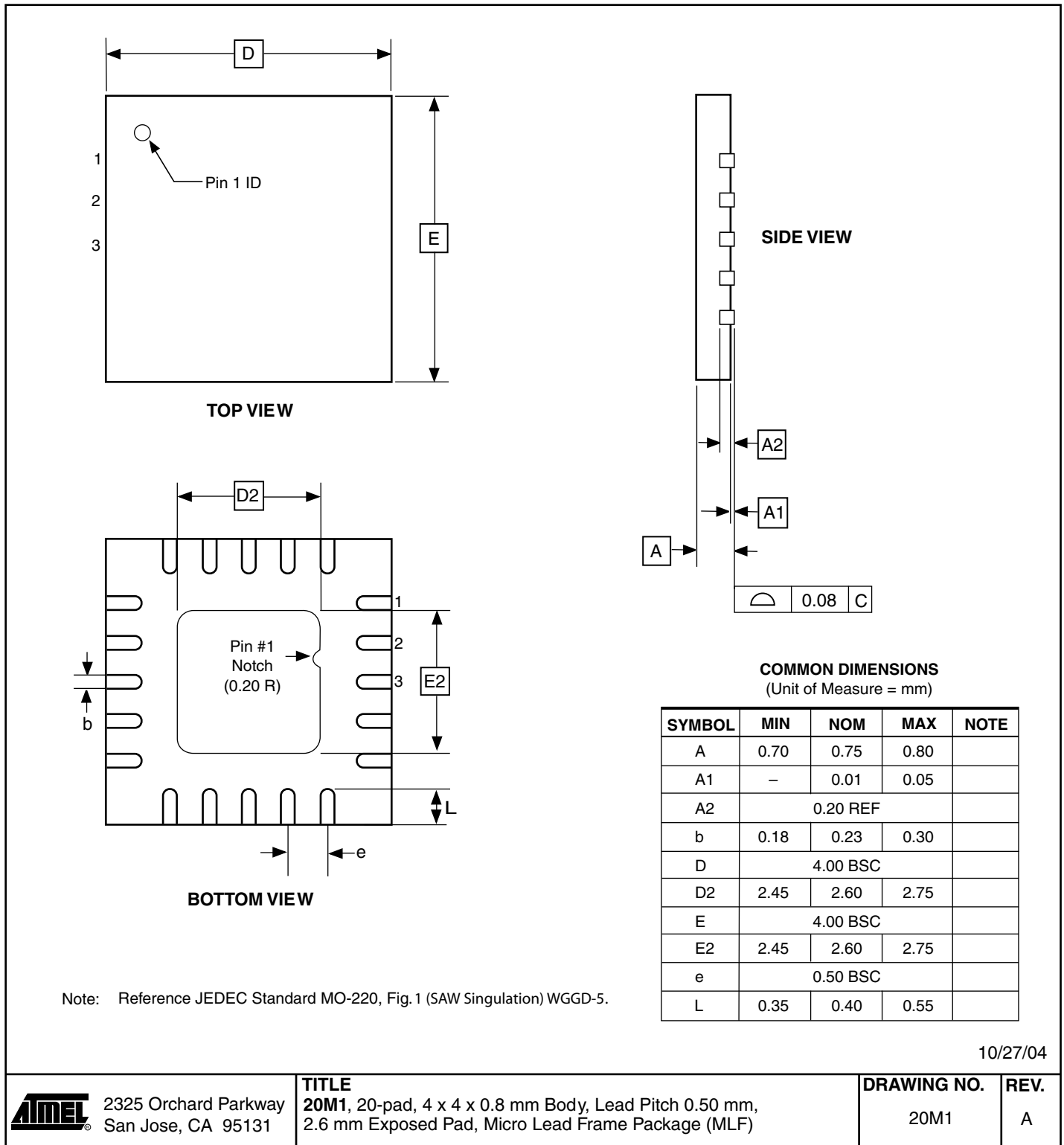
- U: matte tin
- R: tape & reel

2. All packages are Pb-free, halide-free and fully green and they comply with the European directive for Restriction of Hazardous Substances (RoHS).
3. These devices can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.

Package Type	
14S1	14-lead, 0.150" Wide Body, Plastic Gull Wing Small Outline Package (SOIC)
14P3	14-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
20M1	20-pad, 4 x 4 x 0.8 mm Body, Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)

7. Packaging Information

7.1 20M1



8. Errata

The revision letters in this section refer to the revision of the corresponding ATtiny24/44/84 device.

8.1 ATtiny24

8.1.1 Rev. D – E

No known errata.

8.1.2 Rev. C

- **Reading EEPROM when system clock frequency is below 900 kHz may not work**

1. **Reading EEPROM when system clock frequency is below 900 kHz may not work**

Reading data from the EEPROM at system clock frequency below 900 kHz may result in wrong data read.

Problem Fix/Work around

Avoid using the EEPROM at clock frequency below 900 kHz.

8.1.3 Rev. B

- **EEPROM read from application code does not work in Lock Bit Mode 3**
- **Reading EEPROM when system clock frequency is below 900 kHz may not work**

1. **EEPROM read from application code does not work in Lock Bit Mode 3**

When the Memory Lock Bits LB2 and LB1 are programmed to mode 3, EEPROM read does not work from the application code.

Problem Fix/Work around

Do not set Lock Bit Protection Mode 3 when the application code needs to read from EEPROM.

2. **Reading EEPROM when system clock frequency is below 900 kHz may not work**

Reading data from the EEPROM at system clock frequency below 900 kHz may result in wrong data read.

Problem Fix/Work around

Avoid using the EEPROM at clock frequency below 900 kHz.

8.1.4 Rev. A

Not sampled.

8.3 ATtiny84

8.3.1 Rev. A – B

No known errata.

9. Datasheet Revision History

Please note that the referring page numbers refer to the complete document.

9.1 Rev K. - 10/10

1. Added note for Internal 1.1V Reference in [Table 16-4 on page 146](#).
2. Added tape & reel in [Section 24. "Ordering Information" on page 217](#).
3. Updated last page.

9.2 Rev J. - 08/10

1. Updated [Section 6.4 "Clock Output Buffer" on page 30](#), changed CLKO to CKOUT.
2. Removed text "Not recommended for new design" from cover page.

9.3 Rev I. - 06/10

1. Removed "Preliminary" from cover page.
2. Updated notes in [Table 19-16, "High-voltage Serial Programming Instruction Set for ATtiny24/44/84," on page 171](#).
3. Added clarification before [Table 6-8, "Capacitance for the Low-Frequency Crystal Oscillator," on page 28](#).
4. Updated some table notes in [Section 20. "Electrical Characteristics" on page 174](#).

9.4 Rev H. 10/09

1. Updated document template. Re-arranged some sections.
2. Updated ["Low-Frequency Crystal Oscillator" with the Table 6-8 on page 28](#)
3. Updated Tables:
 - ["Active Clock Domains and Wake-up Sources in Different Sleep Modes" on page 33](#)
 - ["DC Characteristics" on page 174](#)
 - ["Register Summary" on page 213](#)
4. Updated Register Description:
 - ["ADMUX – ADC Multiplexer Selection Register" on page 145](#)
5. Signature Imprint Reading Instructions updated in ["Reading Device Signature Imprint Table from Firmware" on page 156](#).
6. Updated Section:
 - [Step 1. on page 164](#)
7. Added Table:
 - ["Analog Comparator Characteristics" on page 179](#)
8. Updated Figure:
 - ["Active Supply Current vs. frequency \(1 - 20 MHz\)" on page 187](#)
9. Updated [Figure 21-30 on page 201](#) and [Figure 21-33 on page 202](#) under "Pin Threshold and Hysteresis".
10. Changed ATtiny24/44 device status to "Not Recommended for New Designs. Use: ATtiny24A/44A".

9.5 Rev G. 01/08

1. Updated sections:
 - “Features” on page 1
 - “RESET” on page 3
 - “Overview” on page 4
 - “About” on page 6
 - “SPH and SPL — Stack Pointer Register” on page 11
 - “Atomic Byte Programming” on page 17
 - “Write” on page 17
 - “Clock Sources” on page 25
 - “Default Clock Source” on page 30
 - “Sleep Modes” on page 33
 - “Software BOD Disable” on page 34
 - “External Interrupts” on page 49
 - “USIBR – USI Data Buffer” on page 125
 - “USIDR – USI Data Register” on page 124
 - “DIDR0 – Digital Input Disable Register 0” on page 131
 - “Features” on page 132
 - “Prescaling and Conversion Timing” on page 135
 - “Temperature Measurement” on page 144
 - “ADMUX – ADC Multiplexer Selection Register” on page 145
 - “Limitations of debugWIRE” on page 152
 - “Reading Lock, Fuse and Signature Data from Software” on page 155
 - “Device Signature Imprint Table” on page 161
 - “Enter High-voltage Serial Programming Mode” on page 168
 - “Absolute Maximum Ratings*” on page 174
 - “DC Characteristics” on page 174
 - “Speed” on page 175
 - “Clock Characteristics” on page 176
 - “Accuracy of Calibrated Internal RC Oscillator” on page 176
 - “System and Reset Characteristics” on page 177
 - “Supply Current of I/O Modules” on page 185
 - “ATtiny24” on page 223
 - “ATtiny44” on page 224
 - “ATtiny84” on page 225
2. Updated bit definitions in sections:
 - “MCUCR – MCU Control Register” on page 36
 - “MCUCR – MCU Control Register” on page 51
 - “MCUCR – MCU Control Register” on page 67
 - “PINA – Port A Input Pins” on page 68

- “SPMCSR – Store Program Memory Control and Status Register” on page 157
 - “Register Summary” on page 213
3. Updated Figures:
- “Reset Logic” on page 39
 - “Watchdog Reset During Operation” on page 42
 - “Compare Match Output Unit, Schematic (non-PWM Mode)” on page 95
 - “Analog to Digital Converter Block Schematic” on page 133
 - “ADC Timing Diagram, Free Running Conversion” on page 137
 - “Analog Input Circuitry” on page 140
 - “High-voltage Serial Programming” on page 167
 - “Serial Programming Timing” on page 183
 - “High-voltage Serial Programming Timing” on page 184
 - “Active Supply Current vs. Low Frequency (0.1 - 1.0 MHz)” on page 186
 - “Active Supply Current vs. frequency (1 - 20 MHz)” on page 187
 - “Active Supply Current vs. V_{CC} (Internal RC Oscillator, 8 MHz)” on page 187
 - “Active Supply Current vs. V_{CC} (Internal RC Oscillator, 1 MHz)” on page 188
 - “Active Supply Current vs. V_{CC} (Internal RC Oscillator, 128 kHz)” on page 188
 - “Idle Supply Current vs. Low Frequency (0.1 - 1.0 MHz)” on page 189
 - “Idle Supply Current vs. Frequency (1 - 20 MHz)” on page 189
 - “Idle Supply Current vs. V_{CC} (Internal RC Oscillator, 8 MHz)” on page 190
 - “Idle Supply Current vs. V_{CC} (Internal RC Oscillator, 1 MHz)” on page 190
 - “Idle Supply Current vs. V_{CC} (Internal RC Oscillator, 128 kHz)” on page 191
 - “Power-down Supply Current vs. V_{CC} (Watchdog Timer Disabled)” on page 191
 - “Power-down Supply Current vs. V_{CC} (Watchdog Timer Enabled)” on page 192
 - “Reset Pin Input Hysteresis vs. V_{CC} ” on page 202
 - “Reset Pin Input Hysteresis vs. V_{CC} (Reset Pin Used as I/O)” on page 203
 - “Watchdog Oscillator Frequency vs. V_{CC} ” on page 205
 - “Watchdog Oscillator Frequency vs. Temperature” on page 205
 - “Calibrated 8 MHz RC Oscillator Frequency vs. V_{CC} ” on page 206
 - “Calibrated 8 MHz RC oscillator Frequency vs. Temperature” on page 206
 - “ADC Current vs. V_{CC} ” on page 207
 - “Programming Current vs. V_{CC} (ATtiny24)” on page 209
 - “Programming Current vs. V_{CC} (ATtiny44)” on page 209
 - “Programming Current vs. V_{CC} (ATtiny84)” on page 210
4. Added Figures:
- “Reset Pin Output Voltage vs. Sink Current ($V_{CC} = 3V$)” on page 198
 - “Reset Pin Output Voltage vs. Sink Current ($V_{CC} = 5V$)” on page 198
 - “Reset Pin Output Voltage vs. Source Current ($V_{CC} = 3V$)” on page 199
 - “Reset Pin Output Voltage vs. Source Current ($V_{CC} = 5V$)” on page 199
5. Updated Tables:
- “Device Clocking Options Select” on page 25

- “Start-up Times for the Crystal Oscillator Clock Selection” on page 29
 - “Start-up Times for the Internal Calibrated RC Oscillator Clock Selection” on page 27
 - “Start-up Times for the External Clock Selection” on page 26
 - “Start-up Times for the 128 kHz Internal Oscillator” on page 27
 - “Active Clock Domains and Wake-up Sources in Different Sleep Modes” on page 33
 - “Watchdog Timer Prescale Select” on page 47
 - “Reset and Interrupt Vectors” on page 48
 - “Overriding Signals for Alternate Functions in PA7:PA5” on page 63
 - “Overriding Signals for Alternate Functions in PA4:PA2” on page 64
 - “Overriding Signals for Alternate Functions in PA1:PA0” on page 64
 - “Port B Pins Alternate Functions” on page 65
 - “Overriding Signals for Alternate Functions in PB3:PB2” on page 66
 - “Overriding Signals for Alternate Functions in PB1:PB0” on page 67
 - “Waveform Generation Modes” on page 110
 - “ADC Conversion Time” on page 138
 - “Temperature vs. Sensor Output Voltage (Typical Case)” on page 144
 - “DC Characteristics. $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ ” on page 174
 - “Calibration Accuracy of Internal RC Oscillator” on page 176
 - “Reset, Brown-out, and Internal Voltage Characteristics” on page 177
 - “VBOT vs. BODLEVEL Fuse Coding” on page 179
 - “ADC Characteristics, Single Ended Channels. $T = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ ” on page 180
 - “ADC Characteristics, Differential Channels (Bipolar Mode), $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ ” on page 182
 - “Serial Programming Characteristics, $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 1.8 - 5.5\text{V}$ (Unless Otherwise Noted)” on page 183
 - “High-voltage Serial Programming Characteristics $T_A = 25^{\circ}\text{C}$, $V_{CC} = 5\text{V}$ (Unless otherwise noted)” on page 184
6. Updated code examples in sections:
 - “Write” on page 17
 - “SPI Master Operation Example” on page 119
 7. Updated “Ordering Information” in:
 - “ATtiny84” on page 219

9.6 Rev F. 02/07

1. Updated Figure 1-1 on page 2, Figure 8-7 on page 43, Figure 20-6 on page 184.
2. Updated Table 9-1 on page 48, Table 10-7 on page 65, Table 11-2 on page 80, Table 11-3 on page 81, Table 11-5 on page 81, Table 11-6 on page 82, Table 11-7 on page 82, Table 11-8 on page 83, Table 20-11 on page 182, Table 20-13 on page 184.
3. Updated table references in “TCCR0A – Timer/Counter Control Register A” on page 80.
4. Updated Port B, Bit 0 functions in “Alternate Functions of Port B” on page 65.
5. Updated WDTCSR bit name to WDTCSR in assembly code examples.

6. Updated bit5 name in “TIFR1 – Timer/Counter Interrupt Flag Register 1” on page 114.
7. Updated bit5 in “TIFR1 – Timer/Counter Interrupt Flag Register 1” on page 114.
8. Updated “SPI Master Operation Example” on page 119.
9. Updated step 5 in “Enter High-voltage Serial Programming Mode” on page 168.

9.7 Rev E. 09/06

1. All characterization data moved to “Electrical Characteristics” on page 174.
2. All Register Descriptions gathered up in separate sections at the end of each chapter.
3. Updated “System Control and Reset” on page 39.
4. Updated Table 11-3 on page 81, Table 11-6 on page 82, Table 11-8 on page 83, Table 12-3 on page 109 and Table 12-5 on page 110.
5. Updated “Fast PWM Mode” on page 97.
6. Updated Figure 12-7 on page 98 and Figure 16-1 on page 133.
7. Updated “Analog Comparator Multiplexed Input” on page 129.
8. Added note in Table 19-12 on page 165.
9. Updated “Electrical Characteristics” on page 174.
10. Updated “Typical Characteristics” on page 185.

9.8 Rev D. 08/06

1. Updated “Calibrated Internal 8 MHz Oscillator” on page 26.
2. Updated “OSCCAL – Oscillator Calibration Register” on page 30.
3. Added Table 20-2 on page 176.
4. Updated code examples in “SPI Master Operation Example” on page 119.
5. Updated code examples in “SPI Slave Operation Example” on page 121.
6. Updated “Signature Bytes” on page 162.

9.9 Rev C. 07/06

1. Updated Features in “USI – Universal Serial Interface” on page 117.
2. Added “Clock speed considerations” on page 123.
3. Updated Bit description in “ADMUX – ADC Multiplexer Selection Register” on page 145.
4. Added note to Table 18-1 on page 157.

9.10 Rev B. 05/06

1. Updated “Default Clock Source” on page 30
2. Updated “Power Reduction Register” on page 35.
3. Updated Table 20-4 on page 177, Table 9-4 on page 42, Table 16-3 on page 145, Table 19-5 on page 161, Table 19-12 on page 165, Table 19-16 on page 171, Table 20-11 on page 182.
4. Updated Features in “Analog to Digital Converter” on page 132.
5. Updated Operation in “Analog to Digital Converter” on page 132.
6. Updated “Temperature Measurement” on page 144.

7. Updated DC Characteristics in “Electrical Characteristics” on page 174.
8. Updated “Typical Characteristics” on page 185.
9. Updated “Errata” on page 223.

9.11 Rev A. 12/05

Initial revision.



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