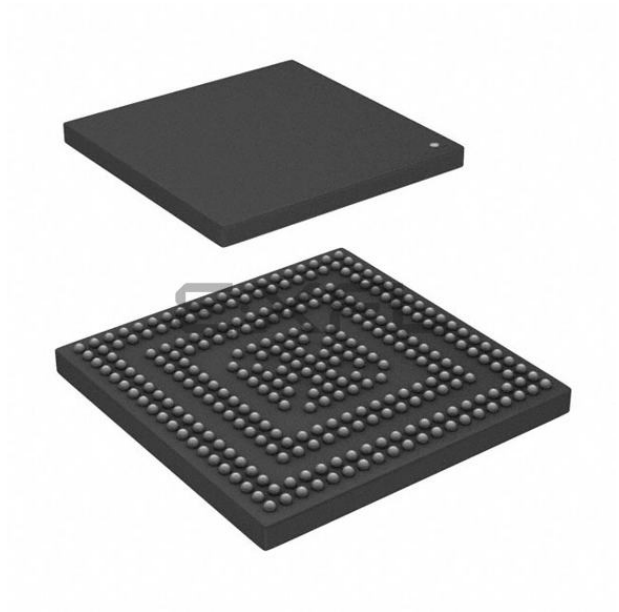
Infineon Technologies - TC297TA128F300SBBKXUMA1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	TriCore™
Core Size	32-Bit Tri-Core
Speed	300MHz
Connectivity	ASC, CANbus, Ethernet, FlexRay, HSSL, I²C, LINbus, MSC, PSI5, QSPI, SENT
Peripherals	DMA, WDT
Number of I/O	169
Program Memory Size	8MB (8M x 8)
Program Memory Type	FLASH
EEPROM Size	384K x 8
RAM Size	2.75M x 8
Voltage - Supply (Vcc/Vdd)	3.3V, 5V
Data Converters	A/D 60x12b, 10 x Sigma-Delta
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	292-LFBGA
Supplier Device Package	PG-LFBGA-292-6
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/tc297ta128f300sbbkxuma1

Table 2-1 Port 00 Functions (cont'd)

Pin	Symbol	Ctrl	Type	Function
N7	P00.3	I	**LP / PU1 / VEXT**	General-purpose input
	TIN12			GTM input
	RXDCAN3A			CAN node 3 input
	RXDCANr1A			CAN node 1 input (MultiCANr+)
	PSIRX1A			PSI5 input
	PSISRXA			PSI5-S input
	SENT2B			SENT input
	CC61INB			CCU60 input
	CC61INA			CCU61 input
	DSCIN3A			DSADC channel 3 input
	VADCG7.3			VADC analog input channel 3 of group 7
	DSITR5F			DSADC channel 5 input
	CIFD12			CIF input
	P00.3	O0		General-purpose output
	TOUT12	O1		GTM output
	ASLSO3	O2		ASCLIN3 output
	–	O3		Reserved
	DSCOUT3	O4		DSADC channel 3 output
	–	O5		Reserved
	SPC2	O6		SENT output
	CC61	O7		CCU61 output
P6	P00.4	I	**LP / PU1 / VEXT**	General-purpose input
	TIN13			GTM input
	REQ7			SCU input
	SENT3B			SENT input
	DSDIN3A			DSADC channel 3 input
	DSSGNA			DSADC channel input
	VADCG7.2			VADC analog input channel 2 of group 7 (MD)
	CIFD13			CIF input
	P00.4	O0		General-purpose output
	TOUT13	O1		GTM output
	PSISTX	O2		PSI5-S output
	–	O3		Reserved
	PSITX1	O4		PSI5 output
	VADCG4BFL0	O5		VADC output
	SPC3	O6		SENT output
	COUT61	O7		CCU61 output

Table 2-3 Port 02 Functions (cont'd)

Pin	Symbol	Ctrl	Type	Function
L7	P02.7	I	**MP / PU1 / VEXT**	General-purpose input
	TIN7			GTM input
	SCLK3A			QSPI3 input
	PSIRX2B			PSI5 input
	SENT1C			SENT input
	CC61INC			CCU60 input
	CCPOS1A			CCU60 input
	T13HRB			CCU61 input
	T3EUDA			GPT120 input
	CIFD7			CIF input
	DSCIN3B			DSADC channel 3 input B
	DSITR4E			DSADC channel 4 input E
	P02.7	O0		General-purpose output
	TOUT7	O1		GTM output
	–	O2		Reserved
	SCLK3	O3		QSPI3 output
	DSCOUT3	O4		DSADC channel 3 output
	VADCEMUX01	O5		VADC output
	SPC1	O6		SENT output
	CC61	O7		CCU60 output

Table 2-7 Port 13 Functions (cont'd)

Pin	Symbol	Ctrl	Type	Function
A13	P13.11	I	**LP / PU1 / VEXT**	General-purpose input
	TIN250			GTM input
	ARX0E			ASCLIN0 input
	P13.11	O0		General-purpose output
	TOUT250	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	–	O4		Reserved
	PSITX3	O5		PSI5 output
	–	O6		Reserved
	–	O7		Reserved
B12	P13.12	I	**LP / PU1 / VEXT**	General-purpose input
	TIN249			GTM input
	ARX3H			ASCLIN3 input
	RXDCANr1B			CAN node 1 input (MultiCANr+)
	SDA1B			I2C1 input
	P13.12	O0		General-purpose output
	TOUT249	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	–	O4		Reserved
	–	O5		Reserved
	SDA1	O6		I2C1 output
	–	O7		Reserved
A12	P13.13	I	**LP / PU1 / VEXT**	General-purpose input
	TIN262			GTM input
	PSIRX3B			PSI5 input
	INJ20			MSC2 input
	P13.13	O0		General-purpose output
	TOUT262	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	–	O4		Reserved
	–	O5		Reserved
	–	O6		Reserved
	–	O7		Reserved

Table 2-8 Port 14 Functions (cont'd)

Pin	Symbol	Ctrl	Type	Function
F18	P14.8	I	**LP / PU1 / VEXT**	General-purpose input
	TIN88			GTM input
	ARX1D			ASCLIN1 input
	RXDCAN2D			CAN node 2 input
	RXD0A0			ERAY0 input
	RXD1A0			ERAY1 input
	P14.8	O0		General-purpose output
	TOUT88	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	–	O4		Reserved
	–	O5		Reserved
	–	O6		Reserved
	–	O7		Reserved
J17	P14.9	I	**MP+ / PU1 / VEXT**	General-purpose input
	TIN89			GTM input
	ACTS0A			ASCLIN0 input
	P14.9	O0		General-purpose output
	TOUT89	O1		GTM output
	END03	O2		MSC0 output
	EN01	O3		MSC0 output
	–	O4		Reserved
	$\overline{\text{TXEN0B}}$	O5		ERAY0 output
	$\overline{\text{TXEN0A}}$	O6		ERAY0 output
	$\overline{\text{TXEN1A}}$	O7		ERAY1 output
J16	P14.10	I	**MP+ / PU1 / VEXT**	General-purpose input
	TIN90			GTM input
	P14.10	O0		General-purpose output
	TOUT90	O1		GTM output
	END02	O2		MSC0 output
	EN00	O3		MSC0 output
	ATX1	O4		ASCLIN1 output
	TXDCAN2	O5		CAN node 2 output
	TXD0A	O6		ERAY0 output
	TXD1A	O7		ERAY1 output

Table 2-14 Port 24 Functions (cont'd)

Pin	Symbol	Ctrl	Type	Function
K29	P24.14	I	**A2 / PU1 / VEBU**	General-purpose input
	TIN236			GTM input
	P24.14	O0		General-purpose output
	TOUT236	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	–	O4		Reserved
	–	O5		Reserved
	–	O6		Reserved
	–	O7		Reserved
	DQ0	HWOUT		EBU Data Bus Line (SDRAM)
	A0			EBU output
K30	P24.15	I	**A2 / PU1 / VEBU**	General-purpose input
	TIN237			GTM input
	P24.15	O0		General-purpose output
	TOUT237	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	–	O4		Reserved
	–	O5		Reserved
	–	O6		Reserved
	–	O7		Reserved
	DQ7	HWOUT		EBU Data Bus Line (SDRAM)
	A7			EBU output

Table 2-15 Port 25 Functions (cont'd)

Pin	Symbol	Ctrl	Type	Function
W29	P25.6	I	**A2 / PU1 / VEBU**	General-purpose input
	P25.6	O0		General-purpose output
	TOUT212	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	–	O4		Reserved
	–	O5		Reserved
	–	O6		Reserved
	–	O7		Reserved
	CKE	HWOUT		EBU output
AD29	P25.7	I	**A2 / PU1 / VEBU**	General-purpose input
	TIN213			GTM input
	P25.7	O0		General-purpose output
	TOUT213	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	–	O4		Reserved
	–	O5		Reserved
	–	O6		Reserved
	–	O7		Reserved
	$\overline{\text{ADV}}$	HWOUT		EBU output
	$\overline{\text{CAS}}$			EBU output
AC29	P25.8	I	**A2 / PU1 / VEBU**	General-purpose input
	TIN214			GTM input
	P25.8	O0		General-purpose output
	TOUT214	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	–	O4		Reserved
	A23	O5		EBU output
	SDRAMA0	O6		EBU output
	–	O7		Reserved
	$\overline{\text{BC0}}$	HWOUT		EBU output

Table 2-19 Port 32 Functions

Pin	Symbol	Ctrl	Type	Function
AE22	P32.0	I	**LP / PX/ VEXT**	General-purpose input
	TIN36			GTM input
	FDEST			PMU input
	VGATE1N			SMPS mode: analog output. External Pass Device gate control for EVR13
	P32.0	O0		General-purpose output
	TOUT36	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	–	O4		Reserved
	–	O5		Reserved
	–	O6		Reserved
	–	O7		Reserved
AE23	P32.2	I	**LP / PU1 / VEXT**	General-purpose input
	TIN38			GTM input
	ARX3D			ASCLIN3 input
	RXDCAN3B			CAN node 3 input
	RXDCANr1D			CAN node 1 input (MultiCANr+)
	P32.2	O0		General-purpose output
	TOUT38	O1		GTM output
	ATX3	O2		ASCLIN3 output
	–	O3		Reserved
	–	O4		Reserved
	–	O5		Reserved
	DCDCSYNC	O6		SCU output
	–	O7		Reserved
AE24	P32.3	I	**LP / PU1 / VEXT**	General-purpose input
	TIN39			GTM input
	P32.3	O0		General-purpose output
	TOUT39	O1		GTM output
	ATX3	O2		ASCLIN3 output
	–	O3		Reserved
	ASCLK3	O4		ASCLIN3 output
	TXDCAN3	O5		CAN node 3 output
	TXDCANr1	O6		CAN node 1 output (MultiCANr+)
	–	O7		Reserved

Table 2-20 Port 33 Functions (cont'd)

Pin	Symbol	Ctrl	Type	Function
AE15	P33.1	I	**LP / PU1 / VEXT**	General-purpose input
	TIN23			GTM input
	PSIRX0C			PSI5 input
	SENT9C			SENT input
	DSCIN2B			DSADC channel 2 input B
	DSITR1E			DSADC channel 1 input E
	P33.1	O0		General-purpose output
	TOUT23	O1		GTM output
	ASLSO3	O2		ASCLIN3 output
	SCLK2	O3		QSPI2 output
	DSCOUT2	O4		DSADC channel 2 output
	VADCEMUX02	O5		VADC output
	VADCG2BFL1	O6		VADC output
	–	O7		Reserved
AD16	P33.2	I	**LP / PU1 / VEXT**	General-purpose input
	TIN24			GTM input
	SENT8C			SENT input
	DSDIN2B			DSADC channel 2 input B
	DSITR2E			DSADC channel 2 input E
	P33.2	O0		General-purpose output
	TOUT24	O1		GTM output
	ASCLK3	O2		ASCLIN3 output
	SLSO210	O3		QSPI2 output
	PSITX0	O4		PSI5 output
	VADCEMUX01	O5		VADC output
	VADCG2BFL2	O6		VADC output
	–	O7		Reserved

Table 2-20 Port 33 Functions (cont'd)

Pin	Symbol	Ctrl	Type	Function
AD20	P33.10	I	**MP / PU1 / VEXT**	General-purpose input
	TIN32			GTM input
	$\overline{\text{SLSI4A}}$			QSPI4 input
	HSIC3INB			QSPI3 input
	P33.10	O0		General-purpose output
	TOUT32	O1		GTM output
	SLSO16	O2		QSPI1 output
	SLSO40	O3		QSPI4 output
	ASLSO1	O4		ASCLIN1 output
	PSISCLK	O5		PSI5-S output
	–	O6		Reserved
	COUT61	O7		CCU61 output
AE20	P33.11	I	**MP / PU1 / VEXT**	General-purpose input
	TIN33			GTM input
	SCLK4A			QSPI4 input
	P33.11	O0		General-purpose output
	TOUT33	O1		GTM output
	ASCLK1	O2		ASCLIN1 output
	SCLK4	O3		QSPI4 output
	–	O4		Reserved
	–	O5		Reserved
	DSCGPWMN	O6		DSADC channel output
	CC61	O7		CCU61 output
AD21	P33.12	I	**MP / PU1 / VEXT**	General-purpose input
	TIN34			GTM input
	MTSR4A			QSPI4 input
	P33.12	O0		General-purpose output
	TOUT34	O1		GTM output
	ATX1	O2		ASCLIN1 output
	MTSR4	O3		QSPI4 output
	ASCLK1	O4		ASCLIN1 output
	–	O5		Reserved
	DSCGPWMP	O6		DSADC output
	COUT60	O7		CCU61 output

Table 2-22 Port 40 Functions (cont'd)

Pin	Symbol	Ctrl	Type	Function
V10	P40.8	I	**S / HighZ / VDDM**	General-purpose input
	VADCG4.6			VADC analog input channel 6 of group 4
	DS3PB			DSADC: positive analog input of channel 3, pin B
	CCPOS2B			CCU61 input
	SENT8A			SENT input
W6	P40.9	I	**S / HighZ / VDDM**	General-purpose input
	VADCG4.7			VADC analog input channel 7 of group 4
	DS3NB			DSADC: negative analog input channel 3, pin B
	CCPOS2D			CCU61 input
	SENT9A			SENT input
AA1	P40.10	I	**S / HighZ / VDDM**	General-purpose input
	VADCG10.3			VADC analog input channel 3 of group 10 (with pull down diagnostics)
	DS8NB			DSADC: negative analog input channel 8, pin B
	SENT10A			SENT input
Y1	P40.11	I	**S / HighZ / VDDM**	General-purpose input
	VADCG10.4			VADC analog input channel 4 of group 10
	DS8PA			DSADC: positive analog input of channel 8, pin A
	SENT11A			SENT input
Y2	P40.12	I	**S / HighZ / VDDM**	General-purpose input
	VADCG10.5			VADC analog input channel 5 of group 10
	DS8NA			DSADC: positive analog input of channel 8, pin A
	SENT12A			SENT input
W1	P40.13	I	**S / HighZ / VDDM**	General-purpose input
	VADCG10.6			VADC analog input channel 6 of group 10
	DS9PA			DSADC: positive analog input of channel 9, pin A
	SENT13A			SENT input
W2	P40.14	I	**S / HighZ / VDDM**	General-purpose input
	VADCG10.7			VADC analog input channel 7 of group 10
	DS9NA			DSADC: positive analog input of channel 9, pin A
	SENT14A			SENT input

Table 2-23 Analog Inputs

Pin	Symbol	Ctrl	Type	Function
AA15	AN0	I	**D / HighZ / VDDM**	Analog input 0
	VADCG0.0			VADC analog input channel 0 of group 0
	DS1PA			DSADC: positive analog input of channel 1, pin A

Table 2-23 Analog Inputs (cont'd)

Pin	Symbol	Ctrl	Type	Function
W2	AN71	I	**S / HighZ / VDDM**	Analog input 71
	VADCG10.7			VADC analog input channel 7 of group 10
	DS9NA			DSADC: negative analog input channel 9, pin A
	SENT14A			SENT input channel 14, pin A

Table 2-24 System I/O

Pin	Symbol	Ctrl	Type	Function
M22	$\overline{\text{PORST}}$	I	**PORST / PD / VEXT**	Power On Reset Input Additional strong PD in case of power fail.
L21	$\overline{\text{ESR0}}$	I/O	**MP / OD / VEXT**	External System Request Reset 0 Default configuration during and after reset is open-drain driver. The driver drives low during power-on reset. This is valid additionally after deactivation of PORST until the internal reset phase has finished. See also SCU chapter for details. Default after power-on can be different. See also SCU chapter ´Reset Control Unit´ and SCU_IOCR register description.
	EVRWUP	I		EVR Wakeup Pin
M21	$\overline{\text{ESR1}}$	I/O	**MP / PU1 / VEXT**	External System Request Reset 1 Default NMI function. See also SCU chapter ´Reset Control Unit´ and SCU_IOCR register description.
	EVRWUP	I		EVR Wakeup Pin
AD22	VGATE1P	O	**VGATE1P / - / VEXT**	External Pass Device gate control for EVR13
AJ20	VGATE3P	O	**VGATE3P / - / VEXT**	External Pass Device gate control for EVR33
R21	TMS	I	**A2 / PD / VDDP3**	JTAG Module State Machine Control Input
	DAP1	I/O		Device Access Port Line 1
T24	$\overline{\text{TRST}}$	I	**A2 / PD / VDDP3**	JTAG Module Reset/Enable Input
P21	TCK	I	**A2 / PD / VDDP3**	JTAG Module Clock Input
	DAP0	I		Device Access Port Line 0

Table 2-27 Port 00 Functions (cont'd)

Pin	Symbol	Ctrl	Type	Function
N3	P00.5	I	**LP / PU1 / VEXT**	General-purpose input
	TIN14			GTM input
	PSIRX2A			PSI5 input
	SENT4B			SENT input
	CC62INB			CCU60 input
	CC62INA			CCU61 input
	DSCIN2A			DSADC channel 2 input
	VADCG7.1			VADC analog input channel 1 of group 7 (MD)
	CIFD14			CIF input
	P00.5	O0		General-purpose output
	TOUT14	O1		GTM output
	DSCGPWMN	O2		DSADC output
	SLSO33	O3		QSPI3 output
	DSCOUT2	O4		DSADC channel 2 output
	VADCG4BFL1	O5		VADC output
	SPC4	O6		SENT output
	CC62	O7		CCU61 output
R3	P00.6	I	**LP / PU1 / VEXT**	General-purpose input
	TIN15			GTM input
	SENT5B			SENT input
	DSDIN2A			DSADC channel 2 input A
	VADCG7.0			VADC analog input channel 0 of group 7 (with pull down diagnostics)
	DSITR4F			DSADC channel 4 input F
	CIFD15			CIF input
	P00.6	O0		General-purpose output
	TOUT15	O1		GTM output
	DSCGPWMP	O2		DSADC output
	VADCG4BFL2	O3		VADC output
	PSITX2	O4		PSI5 output
	VADCEMUX10	O5		VADC output
	SPC5	O6		SENT output
	COUT62	O7		CCU61 output

Table 2-74 TC29x Bare Die Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
128	P02.7	MP / PU1 / VEXT	4419500	-2310000	GPIO
129	P02.11	LP / PU1 / VEXT	4528000	-2240000	GPIO
130	P02.8	LP / PU1 / VEXT	4419500	-2180000	GPIO
131	VDD	Vx	4528000	-2095000	Must be bonded to VDD
132	VSS	Vx	4528000	-1995000	Must be bonded to VSS
133	P01.0	LP / PU1 / VEXT	4419500	-1937500	GPIO
134	VSS	Vx	4528000	-1910000	Must be bonded to VSS (Double Pad / Center of Elephant Pad Opening)
135	VDD	Vx	4528000	-1780000	Must be bonded to VDD
136	P01.2	LP / PU1 / VEXT	4419500	-1715000	GPIO
137	VSS	Vx	4528000	-1660000	Must be bonded to VSS
138	P01.1	LP / PU1 / VEXT	4419500	-1605000	GPIO
139	P01.3	LP / PU1 / VEXT	4528000	-1545000	GPIO
140	P01.8	LP / PU1 / VEXT	4419500	-1485000	GPIO
141	P01.4	LP / PU1 / VEXT	4528000	-1425000	GPIO
142	P01.9	LP / PU1 / VEXT	4419500	-1365000	GPIO
143	P01.5	LP / PU1 / VEXT	4528000	-1305000	GPIO
144	P01.10	LP / PU1 / VEXT	4419500	-1245000	GPIO
145	VEXT	Vx	4528000	-1190000	Must be bonded to VEXT
146	P01.11	LP / PU1 / VEXT	4419500	-1135000	GPIO
147	P01.6	MP / PU1 / VEXT	4528000	-1065000	GPIO
148	P01.12	MP+ / PU1 / VEXT	4419500	-975000	GPIO
149	P01.7	MP / PU1 / VEXT	4528000	-885000	GPIO
150	VDD	Vx	4528000	-785000	Must be bonded to VDD
151	VSS	Vx	4528000	-685000	Must be bonded to VSS
152	P01.13	MP+ / PU1 / VEXT	4419500	-610000	GPIO
153	VSS	Vx	4528000	-535000	Must be bonded to VSS
154	P01.14	MP+ / PU1 / VEXT	4419500	-460000	GPIO
155	Reserved	Vx	4528000	-385000	Must be bonded to VSS
156	P01.15	LP / PU1 / VEXT	4419500	-330000	GPIO
157	VEXT	Vx	4528000	-265000	Must be bonded to VEXT
158	P00.13	MP+ / PU1 / VEXT	4419500	-190000	GPIO
159	P00.0	MP / PU1 / VEXT	4528000	-100000	GPIO
160	P00.14	LP / PU1 / VEXT	4419500	-30000	GPIO
161	VSS	Vx	4528000	25000	Must be bonded to VSS

Table 2-74 TC29x Bare Die Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
206	VDDM	Vx	4528000	2735000	Must be bonded to VEXT
207	AN67 (VADC10.3 / DS8NB), P40.10 (SENT10A)	S	4419500	2685000	Analog input, GPI (SENT)
208	VSSM	Vx	4528000	2835000	Must be bonded to VSS
209	VSS	Vx	4419500	2785000	Must be bonded to VSS
210	AN65 (VADC10.1)	D	4528000	2935000	Analog input
211	AN66 (VADC10.2 / DS8PB	D	4419500	2885000	Analog input
212	AN63 (VADC9.7 / DS7NB)	D	4528000	3035000	Analog input
213	AN64 (VADC10.0)	D	4419500	2985000	Analog input
214	AN61 (VADC9.5 / DS7NA)	D	4528000	3135000	Analog input
215	AN62 (VADC9.6 / DS7PB)	D	4419500	3085000	Analog input
216	AN59 (VADC9.3)	D	4528000	3235000	Analog input
217	AN60 (VADC9.4 / DS7PA)	D	4419500	3185000	Analog input
218	AN57 (VADC9.1)	D	4528000	3335000	Analog input
219	AN58 (VADC9.2)	D	4419500	3285000	Analog input
220	VAREF3	Vx	4528000	3435000	Positive Analog Reference Voltage 3
221	AN56 (VADC9.0)	D	4419500	3385000	Analog input
222	VAGND3	Vx	4528000	3535000	Negative Analog Reference Voltage 3
223	VAREF2	Vx	4419500	3485000	Positive Analog Reference Voltage 2
224	AN55 (VADC8.7 / DS6NB)	D	4528000	3635000	Analog input
225	VAGND2	Vx	4419500	3585000	Negative Analog Reference Voltage 2
226	AN53 (VADC8.5 / DS6NA)	D	4528000	3735000	Analog input
227	AN54 (VADC8.6 / DS6PB)	D	4419500	3685000	Analog input
228	AN51 (VADC8.3)	D	4528000	3835000	Analog input

Table 2-74 TC29x Bare Die Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
340	P30.0	MP / PU1 / VFLEXE	-2483000	4295000	GPIO
341	P30.1	MP / PU1 / VFLEXE	-2563000	4186500	GPIO
342	P30.2	MP / PU1 / VFLEXE	-2643000	4295000	GPIO
343	VFLEXE	Vx	-2788000	4295000	Must be bonded to VEXT or VDDP3
344	P30.3	MP / PU1 / VFLEXE	-2723000	4186500	GPIO
345	VSS	Vx	-2918000	4295000	Must be bonded to VSS
346	P30.4	MP / PU1 / VFLEXE	-2853000	4186500	GPIO
347	P30.5	MP / PU1 / VFLEXE	-2983000	4186500	GPIO
348	P30.6	MP / PU1 / VFLEXE	-3063000	4295000	GPIO
349	P30.8	MP / PU1 / VFLEXE	-3223000	4295000	GPIO
350	P30.7	MP / PU1 / VFLEXE	-3143000	4186500	GPIO
351	VFLEXE	Vx	-3368000	4295000	Must be bonded to VEXT or VDDP3
352	P30.9	MP / PU1 / VFLEXE	-3303000	4186500	GPIO
353	P30.11	MP / PU1 / VFLEXE	-3513000	4295000	GPIO
354	P30.10	MP / PU1 / VFLEXE	-3433000	4186500	GPIO
355	P30.15	MP / PU1 / VFLEXE	-3673000	4295000	GPIO
356	P30.12	MP / PU1 / VFLEXE	-3593000	4186500	GPIO
357	VSS	Vx	-3818000	4295000	Must be bonded to VSS
358	P30.13	MP / PU1 / VFLEXE	-3753000	4186500	GPIO
359	P26.0	LP / PU1 / VFLEXE	-3953000	4295000	GPIO
360	P30.14	MP / PU1 / VFLEXE	-3883000	4186500	GPIO
361	VSS	Vx	-4098000	4295000	Must be bonded to VSS (Double Pad / Center of Elephant Pad Opening)

Table 3-30 DSADC_33V (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Pass band ripple [8]	df_{PB} CC	-1	-	1	%	
Output sampling rate	f_D CC	30	-	330	kHz	
DC compensation factor	DCF CC	-3	-	-	dB	10^{-5} f_D
Positive reference V_{AREF1} pin leakage	I_{OZ5} CC	-2	-	2	µA	
Negative reference V_{AGND1} pin leakage	I_{OZ6} CC	-3	-	2	µA	
Stop band attenuation [8]	SBA CC	40	-	-	dB	0.5 ... 1 f_D
		45	-	-	dB	1 ... 1.5 f_D
		50	-	-	dB	1.5 ... 2 f_D
		55	-	-	dB	2 ... 2.5 f_D
		60	-	-	dB	2.5 ... OSR/2 f_D
Reference ground voltage	V_{AGND} SR	V_{SSM} - 0.05	-	V_{SSM} + 0.05	V	
Positive reference voltage	V_{AREF} SR	V_{DDMnom} * 0.9	-	V_{DDM} + 0.05	V	
Common mode voltage accuracy	dV_{CM} CC	-100	-	100	mV	from selected voltage
Common mode hold voltage deviation [12]	dV_{CMH} CC	-200	-	200	mV	From common mode voltage
Analog filter settling time	t_{AFSET} CC	-	2	4	µs	If enabled
Modulator recovery time	t_{MREC} CC	-	3.5	-	µs	After leaving overdrive state
Modulator settling time [13]	t_{MSET} CC	-	1	-	µs	After switching on, voltage regulator already running
Spurious Free Dynamic Range [7][14]	SFDR CC	52	-	-	dB	V_{CM} = 2.2 V, DC coupled; V_{DDM} = ±10%
		60	-	-	dB	V_{CM} = 2.2 V, DC coupled; V_{DDM} = ±5%

1) The maximum input range for symmetrical signals (e.g. AC-coupled inputs) depends on the selected internal/external common mode voltage. In this case the Amplitude is limited to V_{CM} * 2.
2) All modulators must run on the same frequency.
3) The calibration sequence must be executed once after an Application Reset
4) The total DC error for the uncalibrated case can be calculated by the geometric addition of ED_{GAIN} and ED_{OFF}
5) Recalibration needed in case of a temperature change > 20ºC.
6) The variation of the impedance between different channels is < 1.5%.
7) Derating factors:
-2 dB in standard-performance mode.
-3 dB for CMV = 10_B, i.e. V_{CM} = (V_{AREF}±2%) / 2.0.
8) CIC3, FIR0, FIR1 filters enabled.
9) Single-ended mode reduces the SNR by 6 dB if the unused input is grounded, by 3 dB if the unused input connects to V_{CM} (GAIN = 2).

Table 3-70 Master Mode timing MPss output pads (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
MRST setup to SCLK latching edge [4]	t_{52} SR	50 [4)5)]	-	-	ns	C_L=25pF
MRST hold from SCLK latching edge	t_{53} SR	-6 [4)5)]	-	-	ns	C_L=25pF

1) Documented value is valid for master transmit or slave receive only. For full duplex the external SPI counterpart timing has to be taken into account.
2) The PLL jitter is not included. It should be considered additionally, corresponding to the used baudrate. The duty cycle can be adjusted using the bit fields ECONz.A, B and C with the finest granularity of T_{MAX} = 1 / f_{MAX}.
3) Positive deviation lenghtens the high time and shortens the low time of a clock period. Negative deviation does the opposite.
4) For compensation of the average on-chip delay the QSPI module provides the bit fields ECONz.A, B and C.
5) The setup and hold times are valid for both settings of the input pads thresholds: TTL and AL.

Table 3-71 Master Mode timing MPsm output pads

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCLKO clock period [1]	t_{50} CC	200	-	-	ns	C_L=50pF
Deviation from the ideal duty cycle [2) 3)]	t_{500} CC	-5	-	9+0.06 * C_L	ns	0 < C_L < 200pF
MTSR delay from SCLKO shifting edge	t_{51} CC	-19	-	19	ns	C_L=50pF
SLSOn deviation from the ideal programmed position	t_{510} CC	-19	-	17	ns	C_L=50pF
MRST setup to SCLK latching edge [4]	t_{52} SR	100 [4)5)]	-	-	ns	C_L=50pF
MRST hold from SCLK latching edge	t_{53} SR	-13 [4)5)]	-	-	ns	C_L=50pF

1) Documented value is valid for master transmit or slave receive only. For full duplex the external SPI counterpart timing has to be taken into account.
2) The PLL jitter is not included. It should be considered additionally, corresponding to the used baudrate. The duty cycle can be adjusted using the bit fields ECONz.A, B and C with the finest granularity of T_{MAX} = 1 / f_{MAX}.
3) Positive deviation lenghtens the high time and shortens the low time of a clock period. Negative deviation does the opposite.
4) For compensation of the average on-chip delay the QSPI module provides the bit fields ECONz.A, B and C.
5) The setup and hold times are valid for both settings of the input pads thresholds: TTL and AL.

Table 3-72 Master Mode timing MPRm/MP+m/MPm/LPm output pads

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCLKO clock period [1]	t_{50} CC	400	-	-	ns	C_L=50pF
Deviation from the ideal duty cycle [2) 3)]	t_{500} CC	-6-0.07 * C_L	-	6+0.095 * C_L	ns	0 < C_L < 200pF

Table 3-90 LVDSH - Reduced TX and RX (RED) (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Receiver differential input impedance	R_{in} CC	90	100	110	Ohm	0 V < V_I < 1.6V
		80	100	120	Ohm	1.6 V < V_I < 2.0V
Slew rate	$SRtx$ CC	-	-	2	V/ns	
Change in VOS between 0 and 1	$dVOS$ CC	-	-	50	mV	Peak to peak (including DC transients).
Change in Vod between 0 and 1	$dVod$ CC	-	-	50	mV	Peak to peak (including DC transients)
Fall time [1]	t_{fall} CC	0.26	-	1.2	ns	Rt = 100 Ohm ±20% @2pF
Rise time [1]	t_{rise} CC	0.26	-	1.2	ns	Rt = 100 Ohm ±20% @2pF

1) Rise / fall times are defined for 10% - 90% of V_{OD}

Table 3-91 HSCT PLL

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
PLL frequency range	f_{PLL} CC	12.5	320	320	MHz	
PLL input frequency	f_{REF} CC	10	-	20	MHz	
PLL lock-in time	t_{LOCK} CC	-	-	50	µs	
Bit Error Rate based on 10 MHz reference clock at Slave PLL side	BER_{10} CC	-	-	10EXP-9	-	Bit Error Rate based on Slave interface reference clock at 10 MHz
Bit Error Rate based on 20 MHz reference clock at Slave PLL side	BER_{20} CC	-	-	10EXP-12	-	Bit Error Rate based on Slave interface reference clock at 20 MHz
Absolute RMS Jitter (TX out)	J_{ABS10} CC	-125	-	125	ps	Measured at link TX out; valid for Reference frequency at 10 MHz
Absolute RMS Jitter (TX out)	J_{ABS20} CC	-85	-	85	ps	Measured at link TX out; valid for Reference frequency at 20 MHz

- Add 'V_{AREFx} = V_{AREF2}' T_J=150 °C to T_J
- Add max 2 µA to I_{OZ2}
- Change note of I_{OZ2} from '' to 'V_{AREFx} = V_{AREF2}'
- Add footnote 'This parameter is valid for soldered devices and requires careful analog board design.' to $ENRMS$
- Change note of TUE from '12-bit resolution' to '12-bit Resolution; T_J ≤ 150 °C'
- Change note of TUE from '12-bit resolution' to '12-bit Resolution; T_J ≤ 150 °C'
- Change note of EA_{DNL} from '' to '12-bit resolution'
- Change note of EA_{DNL} from '' to '12-bit resolution'
- Change note of EA_{INL} from '' to '12-bit Resolution; T_J ≤ 150 °C'
- Change note of EA_{INL} from '' to '12-bit Resolution; T_J ≤ 150 °C'
- Change note of EA_{OFF} from '' to '12-bit Resolution; T_J ≤ 150 °C'
- Change note of EA_{OFF} from '' to '12-bit Resolution; T_J ≤ 150 °C'
- Change note of EA_{GAIN} from '' to '12-bit Resolution; T_J ≤ 150 °C'
- Change note of EA_{GAIN} from '' to '12-bit Resolution; T_J ≤ 150 °C'
- Change note of Q_{CONV} from 'V_{AIN} = 3.3V, charge consumed from reference pin, precharging disabled' to 'V_{AIN} = 3.3 V, charge consumed from reference pin, precharging disabled'
- Change note of Q_{CONV} from 'V_{AIN} = 3.3V, charge consumed from reference pin, precharging enabled' to 'V_{AIN} = 3.3 V, charge consumed from reference pin, precharging enabled'
- Add min -12 LSB to TUE
- Add max 12 LSB to TUE
- Add min -12 LSB to EA_{INL}
- Add max 12 LSB to EA_{INL}
- Add min -6 LSB to EA_{OFF}
- Add max 6 LSB to EA_{OFF}
- Add min -6 LSB to EA_{GAIN}
- Add max 6 LSB to EA_{GAIN}
- Add min -6 µA to I_{OZ2}
- Add min -3.5 µA to I_{OZ2}
- Add max 6 µA to I_{OZ2}
- Add max 3.5 µA to I_{OZ2}
- Add min -6.5 µA to I_{OZ3}
- Add min -12 µA to I_{OZ3}
- Add max 6.5 µA to I_{OZ3}
- Add max 12 µA to I_{OZ3}
- Add max 10 % to $dVCSD$
- Add max 28 kOhm to R_{CSD}
- Add min V_{SSM} V to V_{AGND}
- Add min V_{SSM} V to V_{AGND}

• EVR/DCDC
  - Update footnote of $DCDC$ to 'Incase of TC29x running with fSRI = 300 MHz, it shall be ensured that the VDD operating range is limited to 1.235V upto 1.430V. The DCDC may be configured in this case with a

  - Remove footnote 'Derating factors:
    -2 dB in standard-performance mode.
    -3 dB for CMV = 10_B, i.e. V_{CM} = (V_{AREF}±2%) / 2.0.' from *SFDR*
  - Add footnote 'SFDR = 20 * log(INL / 2^N)' to *SFDR*
  - Change description of *dVCM* from 'Common Mode Voltage Accuracy' to 'Common mode voltage accuracy'
  - Change description of *dVCMH* from 'Commom mode hold voltage deviation' to 'Common mode hold voltage deviation'
  - Change min value of *SNR* from 70 dB to 74 dB
  - Change min value of *SNR* from 65 dB to 70 dB
  - Change min value of *SNR* from 72 dB to 76 dB
  - Add typ 100 kHz to f_{PB}
  - Add typ 30 kHz to f_{PB}
- EVR/LDO/1.3V
  - Change note of *dVout/dIout* from '*dI*=-150*mA*; *Tsettle*=20*µs*; pass device=off chip' to '*dI*=-150*mA*; *Tsettle*=20*µs*; pass device=off chip'
  - Change note of *dVout/dIout* from '*dI*=100*mA*; *Tsettle*=20*µs*; pass device=off chip' to '*dI*=100*mA*; *Tsettle*=20*µs*; pass device=off chip'
  - Add max 6.3 µF to C_{OUT}
  - Add min 3 µF to C_{OUT}
- EVR/LDO/3.3V
  - Change note of *dVout/dIout* from '*dI*=100*mA*; *Tsettle*=20*µs*' to '*dI*=50*mA*/20*ns*; *Tsettle*=20*us*'
  - Change note of *dVout/dIout* from '*dI*=-100*mA*; *Tsettle*=20*µs*' to '*dI*=-70*mA*/20*ns*; *Tsettle*=20*us*'
- FLASH
  - Change max value of t_{PRD} from 75 µs to 50 + 2500/(f_{FSI} [MHz]) µs
  - Change note of t_{MERP} from 'For consecutive logical sectors in a physical sector' to 'For consecutive logical sectors in a physical sector, cycle count < 1000'
  - Change max value of t_{PRP5} from 80 µs to 50 + 3000/(f_{FSI} [MHz]) µs
  - Change max value of t_{PRP3} from 115 µs to 81 + 3400/(f_{FSI} [MHz]) µs
  - Change max value of t_{PRPB5} from 220 µs to 125 + 9500/(f_{FSI} [MHz]) µs
  - Change note of t_{PRPB5_1MB} from 'Derived value for documentation purpose' to 'Derived value for documentation purpose, valid for f_{FSI} = 100MHz'
  - Change note of t_{PRPB5_PF} from 'Derived value for documentation purpose' to 'Derived value for documentation purpose, valid for f_{FSI} = 100MHz'
  - Change note of t_{MERD} from 'For consecutive logical sectors' to 'For consecutive logical sector range of size S, cycle count < 125000'
  - Change max value of t_{MERD} from 1 s to 0.928 + 0.019 * (S [KByte]) / (f_{FSI} [MHz]) s
  - Change max value of t_{PRDB} from 140 µs to 96 + 4400/(f_{FSI} [MHz]) µs
  - Change max value of t_{SPNDD} from 120 µs to 12000/(f_{FSI} [MHz]) µs
  - Change max value of t_{PRPB3} from 530 µs to 410 + 12000/(f_{FSI} [MHz]) µs
  - Change max value of t_{ADD} from 20 µs to 15 + 500/(f_{FSI} [MHz]) µs
  - Change max value of t_{SPNDP} from 120 µs to 12000/(f_{FSI} [MHz]) µs
  - Change note of t_{ERD} from '' to 'cycle count < 125000'
  - Change max value of t_{ERD} from 1 s to 0.928 + 0.15/(f_{FSI} [MHz]) s