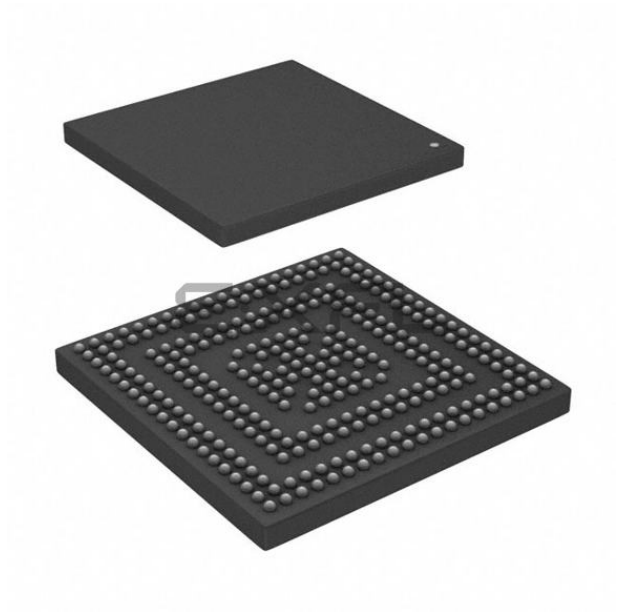
Infineon Technologies - TC297TX128F300SBBKXUMA1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	TriCore™
Core Size	32-Bit Tri-Core
Speed	300MHz
Connectivity	ASC, CANbus, Ethernet, FlexRay, HSSL, I²C, LINbus, MSC, PSI5, QSPI, SENT
Peripherals	DMA, WDT
Number of I/O	263
Program Memory Size	8MB (8M x 8)
Program Memory Type	FLASH
EEPROM Size	384K x 8
RAM Size	2.75M x 8
Voltage - Supply (Vcc/Vdd)	3.3V, 5V
Data Converters	A/D 60x12b, 10 x Sigma-Delta
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	292-LFBGA
Supplier Device Package	PG-LFBGA-292-6
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/tc297tx128f300sbbkxuma1

Edition 2015-05

Published by
Infineon Technologies AG
81726 Munich, Germany

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Table 2-7 Port 13 Functions (cont'd)

Pin	Symbol	Ctrl	Type	Function
B16	P13.4	I	**LVDSM_N / PU1 / VEXT**	General-purpose input
	TIN253			GTM input
	PSIRX4A			PSI5 input
	P13.4	O0		General-purpose output
	TOUT253	O1		GTM output
	END22	O2		MSC2 output
	–	O3		Reserved
	EN20	O4		MSC2 output
	FCLN2	O5		MSC2 output (LVDS)
	FCLND2	O6		MSC2 output (LVDS)
	–	O7		Reserved
A16	P13.5	I	**LVDSM_P / PU1 / VEXT**	General-purpose input
	TIN254			GTM input
	P13.5	O0		General-purpose output
	TOUT254	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	–	O4		Reserved
	FCLP2	O5		MSC2 output (LVDS)
	–	O6		Reserved
	–	O7		Reserved
B15	P13.6	I	**LVDSM_N / PU1 / VEXT**	General-purpose input
	TIN255			GTM input
	P13.6	O0		General-purpose output
	TOUT255	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	–	O4		Reserved
	SON2	O5		MSC2 output (LVDS)
	SOND2	O6		MSC2 output (LVDS)
	–	O7		Reserved

Table 2-8 Port 14 Functions (cont'd)

Pin	Symbol	Ctrl	Type	Function
F18	P14.8	I	**LP / PU1 / VEXT**	General-purpose input
	TIN88			GTM input
	ARX1D			ASCLIN1 input
	RXDCAN2D			CAN node 2 input
	RXD0A0			ERAY0 input
	RXD1A0			ERAY1 input
	P14.8	O0		General-purpose output
	TOUT88	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	–	O4		Reserved
	–	O5		Reserved
	–	O6		Reserved
	–	O7		Reserved
J17	P14.9	I	**MP+ / PU1 / VEXT**	General-purpose input
	TIN89			GTM input
	ACTS0A			ASCLIN0 input
	P14.9	O0		General-purpose output
	TOUT89	O1		GTM output
	END03	O2		MSC0 output
	EN01	O3		MSC0 output
	–	O4		Reserved
	$\overline{\text{TXEN0B}}$	O5		ERAY0 output
	$\overline{\text{TXEN0A}}$	O6		ERAY0 output
	$\overline{\text{TXEN1A}}$	O7		ERAY1 output
J16	P14.10	I	**MP+ / PU1 / VEXT**	General-purpose input
	TIN90			GTM input
	P14.10	O0		General-purpose output
	TOUT90	O1		GTM output
	END02	O2		MSC0 output
	EN00	O3		MSC0 output
	ATX1	O4		ASCLIN1 output
	TXDCAN2	O5		CAN node 2 output
	TXD0A	O6		ERAY0 output
	TXD1A	O7		ERAY1 output

Table 2-9 Port 15 Functions (cont'd)

Pin	Symbol	Ctrl	Type	Function
A22	P15.15	I	**MP / PU1 / VEXT**	General-purpose input
	TIN247			GTM input
	SCLK5A			QSPI5 input
	P15.15	O0		General-purpose output
	TOUT247	O1		GTM output
	–	O2		Reserved
	SCLK5	O3		QSPI5 output
	–	O4		Reserved
	–	O5		Reserved
	–	O6		Reserved
	–	O7		Reserved

Table 2-10 Port 20 Functions

Pin	Symbol	Ctrl	Type	Function
N25	P20.0	I	**MP / PU1 / VEXT**	General-purpose input
	TIN59			GTM input
	RXDCAN3C			CAN node 3 input
	RXDCANr1C			CAN node 1 input (MultiCANr+)
	T6EUDA			GPT120 input
	REQ9			SCU input
	SYSCLK			HSCT input
	$\overline{\text{TGI0}}$			OCDS input
	P20.0	O0		General-purpose output
	TOUT59	O1		GTM output
	ATX3	O2		ASCLIN3 output
	ASCLK3	O3		ASCLIN3 output
	–	O4		Reserved
	SYSCLK	O5		HSCT output
	–	O6		Reserved
	–	O7		Reserved
	$\overline{\text{TGO0}}$	HWOUT		OCDS; ENx

Table 2-10 Port 20 Functions (cont'd)

Pin	Symbol	Ctrl	Type	Function
L22	P20.6	I	**LP / PU1 / VEXT**	General-purpose input
	TIN62			GTM input
	P20.6	O0		General-purpose output
	TOUT62	O1		GTM output
	ARTS1	O2		ASCLIN1 output
	SLSO08	O3		QSPI0 output
	SLSO28	O4		QSPI2 output
	–	O5		Reserved
	WDT2LCK	O6		SCU output
	–	O7		Reserved
L24	P20.7	I	**LP / PU1 / VEXT**	General-purpose input
	TIN63			GTM input
	ACTS1A			ASCLIN1 input
	RXDCAN0B			CAN node 0 input
	P20.7	O0		General-purpose output
	TOUT63	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	–	O4		Reserved
	–	O5		Reserved
	WDT1LCK	O6		SCU output
	COUT63	O7		CCU61 output
L25	P20.8	I	**MP / PU1 / VEXT**	General-purpose input
	TIN64			GTM input
	P20.8	O0		General-purpose output
	TOUT64	O1		GTM output
	ASLSO1	O2		ASCLIN1 output
	SLSO00	O3		QSPI0 output
	SLSO10	O4		QSPI1 output
	TXDCAN0	O5		CAN node 0 output
	WDT0LCK	O6		SCU output
	CC60	O7		CCU61 output

Table 2-11 Port 21 Functions (cont'd)

Pin	Symbol	Ctrl	Type	Function
R25	P21.4	I	LVDSH_N/ PU1 / VDDP3	General-purpose input
	TIN55			GTM input
	P21.4	O0		General-purpose output
	TOUT55	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	–	O4		Reserved
	–	O5		Reserved
	SDRAMA10	O6		EBU output
	–	O7		Reserved
	TXDN	HSCT		HSCT output (LVDS)
P25	P21.5	I	LVDSH_P/ PU1 / VDDP3	General-purpose input
	TIN56			GTM input
	P21.5	O0		General-purpose output
	TOUT56	O1		GTM output
	ASCLK3	O2		ASCLIN3 output
	–	O3		Reserved
	–	O4		Reserved
	–	O5		Reserved
	SDRAMA11	O6		EBU output
	–	O7		Reserved
	TXDP	HSCT		HSCT output (LVDS)
N22	P21.6	I	**A2 / PU / VDDP3**	General-purpose input
	TIN57			GTM input
	ARX3F			ASCLIN3 input
	$\overline{\text{TGI2}}$			OCDS input
	TDI			OCDS (JTAG) input
	T5EUDA			GPT120 input
	P21.6	O0		General-purpose output
	TOUT57	O1		GTM output
	ASLSO3	O2		ASCLIN3 output
	–	O3		Reserved
	–	O4		Reserved
	SYSCLK	O5		HSCT output
	SDRAMA12	O6		EBU output
	T3OUT	O7		GPT120 output
	$\overline{\text{TGO2}}$	HWOUT		OCDS; ENx

Table 2-14 Port 24 Functions (cont'd)

Pin	Symbol	Ctrl	Type	Function
T29	P24.2	I	**A2 / PU1 / VEBU**	General-purpose input
	TIN224			GTM input
	P24.2	O0		General-purpose output
	TOUT224	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	–	O4		Reserved
	–	O5		Reserved
	–	O6		Reserved
	–	O7		Reserved
	DQ14	HWOUT		EBU Data Bus Line (SDRAM)
	A14			EBU output
T30	P24.3	I	**A2 / PU1 / VEBU**	General-purpose input
	TIN225			GTM input
	P24.3	O0		General-purpose output
	TOUT225	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	–	O4		Reserved
	–	O5		Reserved
	–	O6		Reserved
	–	O7		Reserved
	DQ13	HWOUT		EBU Data Bus Line (SDRAM)
	A13			EBU output
R29	P24.4	I	**A2 / PU1 / VEBU**	General-purpose input
	TIN226			GTM input
	P24.4	O0		General-purpose output
	TOUT226	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	–	O4		Reserved
	–	O5		Reserved
	–	O6		Reserved
	–	O7		Reserved
	DQ9	HWOUT		EBU Data Bus Line (SDRAM)
	A9			EBU output

Table 2-15 Port 25 Functions (cont'd)

Pin	Symbol	Ctrl	Type	Function
AC30	P25.9	I	**A2 / PU1 / VEBU**	General-purpose input
	TIN215			GTM input
	P25.9	O0		General-purpose output
	TOUT215	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	–	O4		Reserved
	A22	O5		EBU output
	SDRAMA1	O6		EBU output
	–	O7		Reserved
	$\overline{BC1}$	HWOUT		EBU output
AB29	P25.10	I	**A2 / PU1 / VEBU**	General-purpose input
	TIN216			GTM input
	P25.10	O0		General-purpose output
	TOUT216	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	–	O4		Reserved
	A21	O5		EBU output
	SDRAMA2	O6		EBU output
	–	O7		Reserved
	$\overline{BC2}$	HWOUT		EBU output
AB30	P25.11	I	**A2 / PU1 / VEBU**	General-purpose input
	TIN217			GTM input
	P25.11	O0		General-purpose output
	TOUT217	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	–	O4		Reserved
	A20	O5		EBU output
	SDRAMA3	O6		EBU output
	–	O7		Reserved
	$\overline{BC3}$	HWOUT		EBU output

Table 2-17 Port 30 Functions (cont'd)

Pin	Symbol	Ctrl	Type	Function
AK22	P30.3	I	**MP / PU1 / VFLEXE**	General-purpose input
	TIN193			GTM input
	P30.3	O0		General-purpose output
	TOUT193	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	–	O4		Reserved
	–	O5		Reserved
	–	O6		Reserved
	–	O7		Reserved
	AD15	HWOUT		EBU Address / Data Bus Line
AJ23	P30.4	I	**MP / PU1 / VFLEXE**	General-purpose input
	TIN194			GTM input
	P30.4	O0		General-purpose output
	TOUT194	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	–	O4		Reserved
	–	O5		Reserved
	–	O6		Reserved
	–	O7		Reserved
	AD8	HWOUT		EBU Address / Data Bus Line
AK23	P30.5	I	**MP / PU1 / VFLEXE**	General-purpose input
	TIN195			GTM input
	P30.5	O0		General-purpose output
	TOUT195	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	–	O4		Reserved
	–	O5		Reserved
	–	O6		Reserved
	–	O7		Reserved
	AD13	HWOUT		EBU Address / Data Bus Line

Table 2-18 Port 31 Functions (cont'd)

Pin	Symbol	Ctrl	Type	Function
AJ19	P31.14	I	**MP / PU1 / VFLEXE**	General-purpose input
	TIN188			GTM input
	P31.14	O0		General-purpose output
	TOUT188	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	–	O4		Reserved
	–	O5		Reserved
	–	O6		Reserved
	–	O7		Reserved
	AD18	HWOUT		EBU Address / Data Bus Line
AK19	P31.15	I	**MP / PU1 / VFLEXE**	General-purpose input
	TIN189			GTM input
	P31.15	O0		General-purpose output
	TOUT189	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	–	O4		Reserved
	–	O5		Reserved
	–	O6		Reserved
	–	O7		Reserved
	AD17	HWOUT		EBU Address / Data Bus Line

LVDSM = Pad class LVDSM (5V/3.3V)
LVDSH = Pad class LVDSH (3.3V)
S = Pad class S (Class S parameters for digital input and class D parameters for analog input function)
D = Pad class D (VADC / DSADC)
PU = with pull-up device connected during reset ($\overline{\text{PORST}}$ = 0)
PU1 = with pull-up device connected during reset ($\overline{\text{PORST}}$ = 0)[1) 2) 3)]
PD = with pull-down device connected during reset ($\overline{\text{PORST}}$ = 0)
PD1 = with pull-down device connected during reset ($\overline{\text{PORST}}$ = 0)[1) 2) 3)]
PX = Behavior depends on usage: PD in EVR13 SMPS Mode and PU1 in GPIO Mode
OD = open drain during reset ($\overline{\text{PORST}}$ = 0)
HighZ = tri-state during reset ($\overline{\text{PORST}}$ = 0)
PORST = PORST input pad
XTAL1 = XTAL1 input pad
XTAL2 = XTAL2 input pad
VGATE1P = VGATE1P
VGATE3P = VGATE3P
Vx = Supply
NC = These pins are reserved for future extensions and shall not be connected externally
NC1 = These pins are not connected on package level and will not be used for future extensions
NCVDDPSB = This pin has a different functionality in an Production Device and an Emulation Device. For details pls. see Pin/Ball description of this pin.
NCVDDSB = This pin has a different functionality in an Production Device and an Emulation Device. For details pls. see Pin/Ball description of this pin.

2.1.2 Emergency Stop Function

The Emergency Stop function can be used to force GPIOs (General Purpose Inputs/Outputs) via an external input signal (EMGSTOPA or EMGSTOPB) into a defined state:

- Input state and
- PU or High-Z depending on HWCFG[6] level latched during Porst active

Control of the Emergency Stop function:

- The Emergency Stop function can be enabled/disabled in the SCU (see chapter “SCU”, “Emergency Stop Control”)
- The Emergency Stop input signal, EMGSTOPA (P33.8) / EMGSTOPB (P21.2) , can selected in the SCU (see chapter “SCU”, “Emergency Stop Control”)
- On port level, each GPIO can be enabled/disabled for the Emergency Stop function via the Px_ESR (Port x Emergency Stop) registers in the port control logic (see chapter “General Purpose I/O Ports and Peripheral I/O Lines”, “Emergency Stop Register”).

The Emergency Stop function is available for all GPIO Ports with the following exceptions:

- Not available for P20.2 (General Purpose Input/GPI only, overlayed with Testmode)
- Not available for P40.x (analoge input ANx overlayed with GPI)
- Not available for P32.0 EVR13 SMPS mode.

1) The default state of GPIOs (Px.y) during and after PORST active is controllled via HWCFG[6] (P14.4). HWCFG[6] has a weak internal pull-up active at start-up if the pin is left unconnected.See also User´s Manual, “Introduction Chapter”, “General Purpose I/O Ports and Peripheral I/O Lines”, Figure: “Default state of port pins during and after reset”.
2) If HWCFG[6] is left unconnected or is externally pulled high, weak internal pull-ups (PU1) / pull-downs (PD1) are active during and after reset.
3) If HWCFG[6] is connected to ground, the PD1 / PU1 pins are predominantly in HighZ during and after reset.

Table 2-27 Port 00 Functions (cont'd)

Pin	Symbol	Ctrl	Type	Function
R2	P00.14	I	**LP / PU1 / VEXT**	General-purpose input
	TIN166			GTM input
	DSCIN6A			DSADC channel 6 input A
	P00.14	O0		General-purpose output
	TOUT166	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	DSCOUT6	O4		DSADC channel 6 output
	–	O5		Reserved
	–	O6		Reserved
	–	O7		Reserved
P4	P00.15	I	**MP+ / PU1 / VEXT**	General-purpose input
	TIN168			GTM input
	DSITR6F			DSADC channel 6 input F
	P00.15	O0		General-purpose output
	TOUT168	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	EXTCLK0	O4		SCU output
	–	O5		Reserved
	–	O6		Reserved
	–	O7		Reserved

Table 2-28 Port 01 Functions

Pin	Symbol	Ctrl	Type	Function
F1	P01.0	I	**LP / PU1 / VEXT**	General-purpose input
	TIN155			GTM input
	DSITR6E			DSADC channel 6 input E
	RXDCAN3F			CAN node 3 input
	RXDCANr1E			CAN node 1 input (MultiCANr+)
	P01.0	O0		General-purpose output
	TOUT155	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	–	O4		Reserved
	–	O5		Reserved
	–	O6		Reserved
	–	O7		Reserved

Table 2-35 Port 15 Functions

Pin	Symbol	Ctrl	Type	Function
C22	P15.1	I	**LP / PU1 / VEXT**	General-purpose input
	TIN72			GTM input
	REQ16			SCU input
	ARX1A			ASCLIN1 input
	RXDCAN2A			CAN node 2 input
	$\overline{\text{SLSI2B}}$			QSPI2 input
	EVRWUPB			SCU input
	P15.1	O0		General-purpose output
	TOUT72	O1		GTM output
	ATX1	O2		ASCLIN1 output
	SLSO25	O3		QSPI2 output
	–	O4		Reserved
	–	O5		Reserved
	–	O6		Reserved
	–	O7		Reserved
B21	P15.2	I	**MP / PU1 / VEXT**	General-purpose input
	TIN73			GTM input
	$\overline{\text{SLSI2A}}$			QSPI2 input
	MRST2E			QSPI2 input
	SENT10D			SENT input
	HSIC2INA			QSPI2 input
	P15.2	O0		General-purpose output
	TOUT73	O1		GTM output
	ATX0	O2		ASCLIN0 output
	SLSO20	O3		QSPI2 output
	–	O4		Reserved
	TXDCAN1	O5		CAN node 1 output
	ASCLK0	O6		ASCLIN0 output
	–	O7		Reserved

Table 2-43 Port 30 Functions (cont'd)

Pin	Symbol	Ctrl	Type	Function
AC25	P30.8	I	**MP / PU1 / VFLEXE**	General-purpose input
	TIN198			GTM input
	P30.8	O0		General-purpose output
	TOUT198	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	–	O4		Reserved
	–	O5		Reserved
	–	O6		Reserved
	–	O7		Reserved
	AD3	HWOUT		EBU Address / Data Bus Line
AD25	P30.9	I	**MP / PU1 / VFLEXE**	General-purpose input
	TIN199			GTM input
	P30.9	O0		General-purpose output
	TOUT199	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	–	O4		Reserved
	–	O5		Reserved
	–	O6		Reserved
	–	O7		Reserved
	AD0	HWOUT		EBU Address / Data Bus Line
AE25	P30.10	I	**MP / PU1 / VFLEXE**	General-purpose input
	TIN200			GTM input
	P30.10	O0		General-purpose output
	TOUT200	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	–	O4		Reserved
	–	O5		Reserved
	–	O6		Reserved
	–	O7		Reserved
	AD5	HWOUT		EBU Address / Data Bus Line

LP = Pad class LP (5V/3.3V, Class LP parameters for digital input / output and class D parameters for analog input function)
MP = Pad class MP (5V/3.3V)
MP+ = Pad class MP+ (5V/3.3V)
MPR = Pad class MPR (5V/3.3V)
A2 = Pad class A2 (3.3V)
LVDSM = Pad class LVDSM (5V/3.3V)
LVDSH = Pad class LVDSH (3.3V)
S = Pad class S (Class S parameters for digital input and class D parameters for analog input function)
D = Pad class D (VADC / DSADC)
PU = with pull-up device connected during reset ($\overline{\text{PORST}}$ = 0)
PU1 = with pull-up device connected during reset ($\overline{\text{PORST}}$ = 0)[1) 2) 3)]
PD = with pull-down device connected during reset ($\overline{\text{PORST}}$ = 0)
PD1 = with pull-down device connected during reset ($\overline{\text{PORST}}$ = 0)[1) 2) 3)]
PX = Behavior depends on usage: PD in EVR13 SMPS Mode and PU1 in GPIO Mode
OD = open drain during reset ($\overline{\text{PORST}}$ = 0)
HighZ = tri-state during reset ($\overline{\text{PORST}}$ = 0)
PORST = PORST input pad
XTAL1 = XTAL1 input pad
XTAL2 = XTAL2 input pad
VGATE1P = VGATE1P
VGATE3P = VGATE3P
Vx = Supply
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NCVDDSB = This pin has a different functionality in an Production Device and an Emulation Device. For details pls. see Pin/Ball description of this pin.

2.2.2 Emergency Stop Function

The Emergency Stop function can be used to force GPIOs (General Purpose Inputs/Outputs) via an external input signal (EMGSTOPA or EMGSTOPB) into a defined state:

- Input state and
- PU or High-Z depending on HWCFG[6] level latched during Porst active

Control of the Emergency Stop function:

- The Emergency Stop function can be enabled/disabled in the SCU (see chapter “SCU”, “Emergency Stop Control”)
- The Emergency Stop input signal, EMGSTOPA (P33.8) / EMGSTOPB (P21.2) , can selected in the SCU (see chapter “SCU”, “Emergency Stop Control”)

1) The default state of GPIOs (Px.y) during and after PORST active is controllled via HWCFG[6] (P14.4). HWCFG[6] has a weak internal pull-up active at start-up if the pin is left unconnected.See also User´s Manual, “Introduction Chapter”, “General Purpose I/O Ports and Peripheral I/O Lines”, Figure: “Default state of port pins during and after reset”.
2) If HWCFG[6] is left unconnected or is externally pulled high, weak internal pull-ups (PU1) / pull-downs (PD1) are active during and after reset.
3) If HWCFG[6] is connected to ground, the PD1 / PU1 pins are predominantly in HighZ during and after reset.

Table 2-56 Port 10 Functions (cont'd)

Pin	Symbol	Ctrl	Type	Function
A3	P10.7	I	**LP / PU1 / VEXT**	General-purpose input
	TIN109			GTM input
	ACTS2A			ASCLIN2 input
	MRST3B			QSPI3 input
	REQ4			SCU input
	CCPOS1C			CCU60 input
	T3EUDB			GPT120 input
	P10.7	O0		General-purpose output
	TOUT109	O1		GTM output
	–	O2		Reserved
	MRST3	O3		QSPI3 output
	VADCG7BFL1	O4		VADC output
	TXDCANr0	O5		CAN node 0 output (MultiCANr+)
	–	O6		Reserved
	–	O7		Reserved
B4	P10.8	I	**LP / PU1 / VEXT**	General-purpose input
	TIN110			GTM input
	SCLK3B			QSPI3 input
	REQ5			SCU input
	CCPOS2C			CCU60 input
	T4INB			GPT120 input
	RXDCANr0B			CAN node 0 input (MultiCANr+)
	P10.8	O0		General-purpose output
	TOUT110	O1		GTM output
	ARTS2	O2		ASCLIN2 output
	SCLK3	O3		QSPI3 output
	–	O4		Reserved
	–	O5		Reserved
	–	O6		Reserved
	–	O7		Reserved

Table 2-67 Port 33 Functions

Pin	Symbol	Ctrl	Type	Function
W10	P33.0	I	**LP / PU1 / VEXT**	General-purpose input
	TIN22			GTM input
	DSITR0E			DSADC channel 0 input E
	P33.0	O0		General-purpose output
	TOUT22	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	–	O4		Reserved
	–	O5		Reserved
	VADCG2BFL0	O6		VADC output
	–	O7		Reserved
Y10	P33.1	I	**LP / PU1 / VEXT**	General-purpose input
	TIN23			GTM input
	PSIRX0C			PSI5 input
	SENT9C			SENT input
	DSCIN2B			DSADC channel 2 input B
	DSITR1E			DSADC channel 1 input E
	P33.1	O0		General-purpose output
	TOUT23	O1		GTM output
	ASLSO3	O2		ASCLIN3 output
	SCLK2	O3		QSPI2 output
	DSCOUT2	O4		DSADC channel 2 output
	VADCEMUX02	O5		VADC output
	VADCG2BFL1	O6		VADC output
	–	O7		Reserved
W11	P33.2	I	**LP / PU1 / VEXT**	General-purpose input
	TIN24			GTM input
	SENT8C			SENT input
	DSDIN2B			DSADC channel 2 input B
	DSITR2E			DSADC channel 2 input E
	P33.2	O0		General-purpose output
	TOUT24	O1		GTM output
	ASCLK3	O2		ASCLIN3 output
	SLSO210	O3		QSPI2 output
	PSITX0	O4		PSI5 output
	VADCEMUX01	O5		VADC output
	VADCG2BFL2	O6		VADC output
	–	O7		Reserved

2.3.2 Emergency Stop Function

The Emergency Stop function can be used to force GPIOs (General Purpose Inputs/Outputs) via an external input signal (EMGSTOPA or EMGSTOPB) into a defined state:

- Input state and
- PU or High-Z depending on HWCFG[6] level latched during Porst active

Control of the Emergency Stop function:

- The Emergency Stop function can be enabled/disabled in the SCU (see chapter “SCU”, “Emergency Stop Control”)
- The Emergency Stop input signal, EMGSTOPA (P33.8) / EMGSTOPB (P21.2) , can selected in the SCU (see chapter “SCU”, “Emergency Stop Control”)
- On port level, each GPIO can be enabled/disabled for the Emergency Stop function via the Px_ESR (Port x Emergency Stop) registers in the port control logic (see chapter “General Purpose I/O Ports and Peripheral I/O Lines”, “Emergency Stop Register”).

The Emergency Stop function is available for all GPIO Ports with the following exceptions:

- Not available for P20.2 (General Purpose Input/GPI only, overlayed with Testmode)
- Not available for P40.x (analoge input ANx overlayed with GPI)
- Not available for P32.0 EVR13 SMPS mode.
- Not available for dedicated I/O without General Purpose Output function (e.g ESRx, TMS, TCK)

The Emergency Stop function can be overruled on the following GPIO Ports:

- P00.x and P02.x: Emergency Stop can be overruled by the 8-Bit Standby Controller (SBR), if implemented. Overruling can be disabled via the control registers P00_SCR / P02_SCR (see chapter “General Purpose I/O Ports and Peripheral I/O Lines”, P00 / P01)
- P00.x: Emergency Stop can be overruled by the VADC. Overruling can be disabled via the control register P00_SCR (see chapter “General Purpose I/O Ports and Peripheral I/O Lines”, P00)
- P14.0 and P14.1: Emergency Stop can be overruled in the DXCPL mode (DAP over can physical layer mode). No Overruling in the DXCM (Debug over can message) mode
- P21.6: Emergency Stop can be overruled in JTAG mode if this pin is used as TDI
- P21.7: Emergency Stop can be overruled in JTAG or Three Pin DAP mode
- P20.0: Emergency Stop can be overruled in JTAG mode if this GPIO is used as TDI
- P33.8: Emergency Stop can be overruled if this pin is used as safety output pin (SMUFSP)

2.3.3 Pull-Up/Pull-Down Reset Behavior of the Pins

Table 2-73 List of Pull-Up/Pull-Down Reset Behavior of the Pins

Pins	$\overline{\text{PORST}}$ = 0	$\overline{\text{PORST}}$ = 1
all GPIOs	Pull-up if HWCFG[6] = 1 or High-Z if HWCFG[6] = 0	
$\overline{\text{TDI}}$, $\overline{\text{TESTMODE}}$	Pull-up	
$\overline{\text{PORST}}$[1)]	Pull-down with I_{PORST} relevant	Pull-down with I_{PDLI} relevant
$\overline{\text{TRST}}$, TCK, TMS	Pull-down	
$\overline{\text{ESR0}}$	The open-drain driver is used to drive low.[2)]	Pull-up[3)]

Table 2-74 TC29x Bare Die Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
189	AN44 (VADC5.4 / DS3PC)	S	4528000	1835000	Analog input
190	AN43 (VADC5.3)	D	4419500	1885000	Analog input (with pull down diagnostics)
191	AN42 (VADC5.2)	D	4528000	1935000	Analog input
192	AN41 (VADC5.1)	D	4419500	1985000	Analog input
193	AN40 (VADC5.0)	D	4528000	2035000	Analog input
194	AN38 (VADC4.6 / DS3PB), P40.8 (SENT8A)	S	4528000	2135000	Analog input, GPI (SENT)
195	AN39 (VADC4.7 / DS3NB), P40.9 (SENT9A)	S	4419500	2085000	Analog input, GPI (SENT)
196	AN36 (VADC4.4 / DS3PA), P40.6 (SENT6A)	S	4528000	2235000	Analog input, GPI (SENT)
197	AN37 (VADC4.5 / DS3NA), P40.7 (SENT7A)	S	4419500	2185000	Analog input, GPI (SENT)
198	AN34 (VADC4.2)	D	4528000	2335000	Analog input
199	AN35 (VADC4.3)	D	4419500	2285000	Analog input (with pull down diagnostics)
200	AN32 (VADC4.0), P40.4 (SENT4A)	S	4528000	2435000	Analog input, GPI (SENT)
201	AN33 (VADC4.1), P40.5 (SENT5A)	S	4419500	2385000	Analog input, GPI (SENT)
202	AN70 (VADC10.6 / DS9PA), P40.13 (SENT13A)	S	4528000	2535000	Analog input, GPI (SENT)
203	AN71 (VADC10.7 / DS9NA), P40.14 (SENT14A)	S	4419500	2485000	Analog input, GPI (SENT)
204	AN68 (VADC10.4 / DS8PA), P40.11 (SENT11A)	S	4528000	2635000	Analog input, GPI (SENT)
205	AN69 (VADC10.5 / DS8NA), P40.12 (SENT12A)	S	4419500	2585000	Analog input, GPI (SENT)

  - Change description of $t_{dCCTxAsymAccept25}$ from 'Acceptance of asymmetriy at receiving part' to 'Acceptance of asymmetry at receiving part'
- Absolute Maximum Ratings
  - Change note of T_{ST} from 'upto 65h @ T_J = 150°C' to 'upto 65h @ T_J = 150°C; upto 15h @ T_J = 170°C'
  - Change max value of T_{ST} from 150 °C to 170 °C
- Reset Timings
  - Add footnote 'The timing values assumes programmed BMI with ESR0CNT inactive.' to t_{BP}
  - Add footnote 'The timing values assumes programmed BMI with ESR0CNT inactive.' to t_B
- Changes in table 'Overload Parameters' of Overload
  - Change note of K_{OVDN} from 'Overload injected on LVDS pad and affecting neighbor LVDS pad' to 'Overload injected on LVDS pad and affecting neighbor LVDS pads'
  - Change note of K_{OVDN} from 'Overload injected on GPIO non LVDS pad and affecting neighbor GPIO non LVDS pad' to 'Overload injected on GPIO non LVDS pad and affecting neighbor LP and A2 (exept P24.x and P25.x) pads; -2mA < I_{IN} < 0mA'
  - Change note of K_{OVDP} from 'Overload injected on LVDS pad and affecting neighbor LVDS pad' to 'Overload injected on LVDS pad and affecting neighbor LVDS pads'
  - Change note of K_{OVDP} from 'Overload injected on GPIO non LVDS pad and affecting neighbor GPIO non LVDS pad' to 'Overload injected on GPIO non LVDS pad and affecting neighbor GPIO non LVDS pads'
  - Change max value of K_{OVDN} from 0.9 to 0.93
  - Change note of K_{OVDN} from 'coupling between pads 21.2 and 21.3' to 'coupling between pads 21.0, 21.1,21.2 and 21.3'
  - Change note of K_{OVDN} from 'Overload injected on GPIO non LVDS pad and affecting neighbor GPIO non LVDS pad' to 'Overload injected on GPIO non LVDS pad and affecting neighbor LP and A2 pads; -2mA < I_{IN} < 0mA'
  - Change max value of K_{OVDN} from 1.5*10^{-3} to 6*10^{-4}
  - Add max 1.7*10^{-3} to K_{OVDN}
  - Add max 2*10^{-2} to K_{OVDN}
  - Add max 1*10^{-2} to K_{OVDN}
  - Change note of K_{OVDN} from 'Overload injected on GPIO non LVDS pad and affecting neighbor LP and A2 pads; -5mA < I_{IN} < -2mA' to 'Overload injected on GPIO non LVDS pad and affecting neighbor LP and A2 pads (exept P25.2 and P25.4); -5mA < I_{IN} < -2mA'
  - Add max 1.6*10^{-4} to K_{OVDP}
  - Change max value of K_{OVDP} from 1*10^{-4} to 1.6*10^{-4}
  - Change note of V_{OUS} from 'Valid for LP, MP, MP+, and MPR pads' to 'limited to 60h over lifetime; Valid for LP, MP, MP+, and MPR pads'
  - Change note of K_{OVAP} from 'else' to ''
  - Change max value of K_{OVAN} from 1*10^{-3} to 6*10^{-4}
  - Add max 1*10^{-4} to K_{OVDP}
  - Change note of K_{OVDP} from 'Overload injected on GPIO pad and affecting neighbor P32.4 pad' to 'Overload injected on GPIO pad and affecting neighbor P32.4 and P33.12 pad'
  - Add max 1.4*10^{-2} to K_{OVDN}
  - Add max 4*10^{-3} to K_{OVDN}
  - Add 3*10^{-3} NOUNIT to Overload Parameters
  - Change note of K_{OVAN} from 'else' to 'else; -1mA < I_{IN} < 0mA'