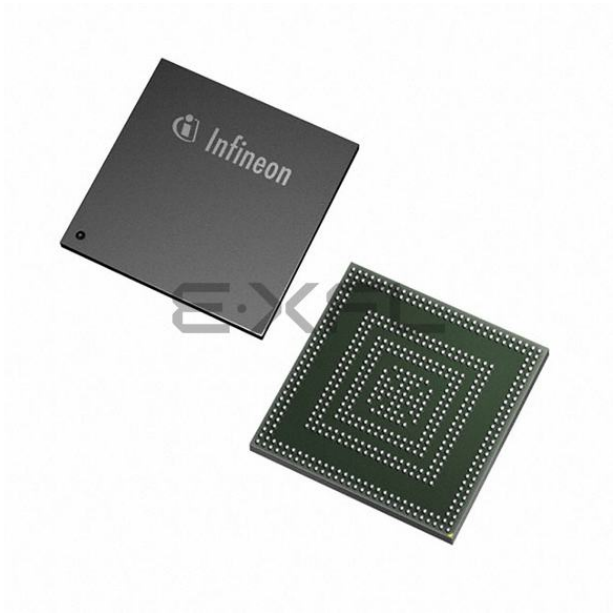
Infineon Technologies - TC299TP128F300NBCLXUMA1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	TriCore™
Core Size	32-Bit Tri-Core
Speed	300MHz
Connectivity	ASC, CANbus, Ethernet, FlexRay, HSSL, I²C, LINbus, MSC, PSI5, QSPI, SENT
Peripherals	DMA, WDT
Number of I/O	263
Program Memory Size	8MB (8M x 8)
Program Memory Type	FLASH
EEPROM Size	384K x 8
RAM Size	728K x 8
Voltage - Supply (Vcc/Vdd)	3.3V, 5V
Data Converters	A/D 84x12b, 10 x Sigma-Delta
Oscillator Type	External
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	516-LFBGA
Supplier Device Package	PG-LFBGA-516-5
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/tc299tp128f300nbclxuma1

Table 2-4 Port 10 Functions (cont'd)

Pin	Symbol	Ctrl	Type	Function
F8	P10.7	I	**LP / PU1 / VEXT**	General-purpose input
	TIN109			GTM input
	ACTS2A			ASCLIN2 input
	MRST3B			QSPI3 input
	REQ4			SCU input
	CCPOS1C			CCU60 input
	T3EUDB			GPT120 input
	P10.7	O0		General-purpose output
	TOUT109	O1		GTM output
	–	O2		Reserved
	MRST3	O3		QSPI3 output
	VADCG7BFL1	O4		VADC output
	TXDCANr0	O5		CAN node 0 output (MultiCANr+)
	–	O6		Reserved
	–	O7		Reserved
G9	P10.8	I	**LP / PU1 / VEXT**	General-purpose input
	TIN110			GTM input
	SCLK3B			QSPI3 input
	REQ5			SCU input
	CCPOS2C			CCU60 input
	T4INB			GPT120 input
	RXDCANr0B			CAN node 0 input (MultiCANr+)
	P10.8	O0		General-purpose output
	TOUT110	O1		GTM output
	ARTS2	O2		ASCLIN2 output
	SCLK3	O3		QSPI3 output
	–	O4		Reserved
	–	O5		Reserved
	–	O6		Reserved
	–	O7		Reserved

Table 2-13 Port 23 Functions (cont'd)

Pin	Symbol	Ctrl	Type	Function
AB24	P23.1	I	**MP+ / PU1 / VEXT**	General-purpose input
	TIN42			GTM input
	SDI10			MSC1 input
	P23.1	O0		General-purpose output
	TOUT42	O1		GTM output
	ARTS1	O2		ASCLIN1 output
	SLSO46	O3		QSPI4 output
	GTMCLK0	O4		GTM output
	–	O5		Reserved
	EXTCLK0	O6		SCU output
	–	O7		Reserved
AB25	P23.2	I	**LP / PU1 / VEXT**	General-purpose input
	TIN43			GTM input
	P23.2	O0		General-purpose output
	TOUT43	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	–	O4		Reserved
	–	O5		Reserved
	–	O6		Reserved
	–	O7		Reserved
AA24	P23.3	I	**LP / PU1 / VEXT**	General-purpose input
	TIN44			GTM input
	INJ10			MSC1 input
	P23.3	O0		General-purpose output
	TOUT44	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	–	O4		Reserved
	–	O5		Reserved
	–	O6		Reserved
	–	O7		Reserved

Table 2-27 Port 00 Functions (cont'd)

Pin	Symbol	Ctrl	Type	Function
T3	P00.7	I	**LP / PU1 / VEXT**	General-purpose input
	TIN16			GTM input
	SENT6B			SENT input
	CC60INC			CCU61 input
	CCPOS0A			CCU61 input
	T12HRB			CCU60 input
	T2INA			GPT120 input
	DSCIN4A			DSADC channel 4 input A
	DS4NA			DSADC negative analog input channel 4, pin A
	VADCG6.5			VADC analog input channel 5 of group 6
	CIFCLK			CIF input
	P00.7	O0		General-purpose output
	TOUT16	O1		GTM output
	–	O2		Reserved
	VADCG4BFL3	O3		VADC output
	DSCOUT4	O4		DSADC channel 4 output
	VADCEMUX11	O5		VADC output
	SPC6	O6		SENT output
	CC60	O7		CCU61 output
T2	P00.8	I	**LP / PU1 / VEXT**	General-purpose input
	TIN17			GTM input
	SENT7B			SENT input
	CC61INC			CCU61 input
	CCPOS1A			CCU61 input
	T13HRB			CCU60 input
	T2EUDA			GPT120 input
	DSDIN4A			DSADC channel 4 input A
	DS4PA			DSADC positive analog input of channel 4, pin A
	VADCG6.4			VADC analog input channel 4 of group 6
	CIFVSNC			CIF input
	P00.8	O0		General-purpose output
	TOUT17	O1		GTM output
	SLSO36	O2		QSPI3 output
	–	O3		Reserved
	–	O4		Reserved
	VADCEMUX12	O5		VADC output
	SPC7	O6		SENT output
	CC61	O7		CCU61 output

Table 2-35 Port 15 Functions

Pin	Symbol	Ctrl	Type	Function
C22	P15.1	I	**LP / PU1 / VEXT**	General-purpose input
	TIN72			GTM input
	REQ16			SCU input
	ARX1A			ASCLIN1 input
	RXDCAN2A			CAN node 2 input
	$\overline{\text{SLSI2B}}$			QSPI2 input
	EVRWUPB			SCU input
	P15.1	O0		General-purpose output
	TOUT72	O1		GTM output
	ATX1	O2		ASCLIN1 output
	SLSO25	O3		QSPI2 output
	–	O4		Reserved
	–	O5		Reserved
	–	O6		Reserved
	–	O7		Reserved
B21	P15.2	I	**MP / PU1 / VEXT**	General-purpose input
	TIN73			GTM input
	$\overline{\text{SLSI2A}}$			QSPI2 input
	MRST2E			QSPI2 input
	SENT10D			SENT input
	HSIC2INA			QSPI2 input
	P15.2	O0		General-purpose output
	TOUT73	O1		GTM output
	ATX0	O2		ASCLIN0 output
	SLSO20	O3		QSPI2 output
	–	O4		Reserved
	TXDCAN1	O5		CAN node 1 output
	ASCLK0	O6		ASCLIN0 output
	–	O7		Reserved

Table 2-44 Port 31 Functions (cont'd)

Pin	Symbol	Ctrl	Type	Function
AE19	P31.4	I	**MP / PU1 / VFLEXE**	General-purpose input
	TIN178			GTM input
	P31.4	O0		General-purpose output
	TOUT178	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	–	O4		Reserved
	–	O5		Reserved
	–	O6		Reserved
	–	O7		Reserved
	AD24	HWOUT		EBU Address / Data Bus Line
AF19	P31.5	I	**MP / PU1 / VFLEXE**	General-purpose input
	TIN179			GTM input
	P31.5	O0		General-purpose output
	TOUT179	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	–	O4		Reserved
	–	O5		Reserved
	–	O6		Reserved
	–	O7		Reserved
	AD23	HWOUT		EBU Address / Data Bus Line
AD20	P31.6	I	**MP / PU1 / VFLEXE**	General-purpose input
	TIN180			GTM input
	P31.6	O0		General-purpose output
	TOUT180	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	–	O4		Reserved
	–	O5		Reserved
	–	O6		Reserved
	–	O7		Reserved
	AD20	HWOUT		EBU Address / Data Bus Line

Table 2-55 Port 02 Functions (cont'd)

Pin	Symbol	Ctrl	Type	Function
D1	P02.4	I	**MP+ / PU1 / VEXT**	General-purpose input
	TIN4			GTM input
	SLSI3A			QSPI3 input
	ECTT1			TTCAN input
	RXDCAN0D			CAN node 0 input
	CC62INA			CCU60 input
	CC62INB			CCU61 input
	DSDIN5B			DSADC channel 5 input B
	SDA0A			I2C0 input
	CIFD4			CIF input
	P02.4	O0		General-purpose output
	TOUT4	O1		GTM output
	ASCLK2	O2		ASCLIN2 output
	SLSO30	O3		QSPI3 output
	PSISCLK	O4		PSI5-S output
	SDA0	O5		I2C0 output
	TXEN0A	O6		ERAY0 output
	CC62	O7		CCU60 output
E2	P02.5	I	**MP+ / PU1 / VEXT**	General-purpose input
	TIN5			GTM input
	MRST3A			QSPI3 input
	ECTT2			TTCAN input
	PSIRX1B			PSI5 input
	PSISRXB			PSI5-S input
	SENT3C			SENT input
	DSCIN4B			DSADC channel 4 input B
	SCL0A			I2C0 input
	CIFD5			CIF input
	P02.5	O0		General-purpose output
	TOUT5	O1		GTM output
	TXDCAN0	O2		CAN node 0 output
	MRST3	O3		QSPI3 output
	DSCOUT4	O4		DSADC channel 4 output
	SCL0	O5		I2C0 output
	TXEN0B	O6		ERAY0 output
	COUT62	O7		CCU60 output

Table 2-57 Port 11 Functions (cont'd)

Pin	Symbol	Ctrl	Type	Function
A8	P11.11	I	**MP+ / PU1 / VFLEX**	General-purpose input
	TIN100			GTM input
	ETHCRSDVA			ETH input
	ETHRXDVA			ETH input
	ETHCRSB			ETH input
	P11.11	O0		General-purpose output
	TOUT100	O1		GTM output
	END02	O2		MSC0 output
	SLSO04	O3		QSPI0 output
	SLSO14	O4		QSPI1 output
	EN00	O5		MSC0 output
	$\overline{\text{TXEN0B}}$	O6		ERAY0 output
	CC61	O7		CCU60 output
B8	P11.12	I	**MPR / PU1 / VFLEX**	General-purpose input
	TIN101			GTM input
	ETHREFCLK			ETH input
	ETHTXCLKB			ETH input (Not for productive purposes)
	ETHRXCLKA			ETH input (Not for productive purposes)
	P11.12	O0		General-purpose output
	TOUT101	O1		GTM output
	ATX1	O2		ASCLIN1 output
	GTMCLK2	O3		GTM output
	TXD0B	O4		ERAY0 output
	TXDCAN3	O5		CAN node 3 output
	EXTCLK1	O6		SCU output
	CC60	O7		CCU60 output

Table 2-63 Port 21 Functions (cont'd)

Pin	Symbol	Ctrl	Type	Function
J17	P21.1	I	**LVDSH_P/ PU1 / VDDP3**	General-purpose input
	TIN52			GTM input
	ETHMDIOB			ETH input (Not for production purposes)
	MRST4DP			QSPI4 input (LVDS)
	WAIT			EBU input
	P21.1	O0		General-purpose output
	TOUT52	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	–	O4		Reserved
	–	O5		Reserved
	ETHMDIO	O6		ETH output (Not for production purposes)
	BREQBA1	O7		EBU output (combined for BREQ and BA1)
	HSM2	O		HSM output
K19	P21.2	I	**LVDSH_N/ PU1 / VDDP3**	General-purpose input
	TIN53			GTM input
	MRST2CN			QSPI2 input (LVDS)
	MRST4CN			QSPI4 input (LVDS)
	ARX3GN			ASCLIN3 input (LVDS)
	EMGSTOPB			SCU input
	RXDN			HSCT input (LVDS)
	P21.2	O0		General-purpose output
	TOUT53	O1		GTM output
	ASLSO3	O2		ASCLIN3 output
	–	O3		Reserved
	–	O4		Reserved
	ETHMDC	O5		ETH output
	SDRAMA8	O6		EBU output
	–	O7		Reserved

Table 2-75 List of Pull-Up/Pull-Down Reset Behavior of the Pins

Pins	$\overline{\text{PORST}}$ = 0	$\overline{\text{PORST}}$ = 1
$\overline{\text{all GPIOs}}$	Pull-up if HWCFG[6] = 1 or High-Z if HWCFG[6] = 0	
$\overline{\text{TDI}}$, $\overline{\text{TESTMODE}}$	Pull-up	
$\overline{\text{PORST}}$[1]	Pull-down with I_{PORST} relevant	Pull-down with I_{PDLI} relevant
$\overline{\text{TRST}}$, TCK, TMS	Pull-down	
$\overline{\text{ESR0}}$	The open-drain driver is used to drive low.[2]	Pull-up[3]
$\overline{\text{ESR1}}$	Pull-up[3]	
TDO	Pull-up	High-Z/Pull-up[4]

1) Pull-down with I_{PORST} relevant is always activated when a primary supply monitor detects a violation.
2) Valid additionally after deactivation of PORST until the internal reset phase has finished. See the SCU chapter for details.
3) See the SCU_IOCR register description.
4) Depends on JTAG/DAP selection with $\overline{\text{TRST}}$.

In case of leakage test ($\overline{\text{PORST}}$ = 0 and $\overline{\text{TESTMODE}}$ = 0), the pull-down of the $\overline{\text{TRST}}$ pin is switched off. In case of an user application ($\overline{\text{TESTMODE}}$ = 1), the pull-down of the $\overline{\text{TRST}}$ is always switched on.

3.5 5 V / 3.3 V switchable Pads

Pad classes LP, MP and MP+ support both Automotive Level (AL) or TTL level (TTL) operation. Parameters are defined for AL operation and degrade in TTL operation.

Table 3-6 Standard_Pads

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Pin capacitance (digital inputs/outputs)	C_{IO} CC	-	6	10	pF	
Spike filter always blocked pulse duration	t_{SF1} CC	-	-	80	ns	PORST only
Spike filter pass-through pulse duration	t_{SF2} CC	220	-	-	ns	PORST only
PORST pad output current [1]	I_{PORST} CC	11	-	-	mA	V_{EXT} = 3.0V; V_{PORST} = 0.9V; T_J = 165°C
		13	-	-	mA	V_{EXT} = 4.5V; V_{PORST} = 1.0V

1) Pull-down with I_{PORST} relevant is always activated when a primary supply monitor detects a violation.

Table 3-7 Class LP 5V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input frequency	f_{IN} SR	-	-	75	MHz	Hysteresis active
		-	-	150	MHz	Hysteresis inactive
Input Hysteresis for LP pad [1]	$HYSLP$ CC	0.09 * $V_{EXT/FLEX}$	-	-	V	AL
		0.075 * $V_{EXT/FLEX}$	-	-	V	TTL
Input Leakage current for LP pad	I_{OZLP} CC	-150	-	150	nA	(0.1*$V_{EXT/FLEX}$) < V_{IN} < (0.9*$V_{EXT/FLEX}$)
		-350	-	350	nA	else
Input leakage current for P32.0	I_{OZP320} CC	-4900	-	4900	nA	(0.1*$V_{EXT/FLEX}$) < V_{IN} < (0.9*$V_{EXT/FLEX}$)
		-9400	-	9400	nA	(0.1*$V_{EXT/FLEX}$) < V_{IN} < (0.9*$V_{EXT/FLEX}$); for T_J > 150°C
		-5800	-	5800	nA	else
		-12000	-	12000	nA	else; for T_J > 150°C
Pull-up current for LP pad	I_{PUHLP} CC	|30|	-	-	µA	V_{IHmin}; AL
		|43|	-	-	µA	V_{IHmin}; TTL
		-	-	|107|	µA	V_{ILmax}; AL and TTL

Table 3-10 Class MP 3.3V (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input high voltage for MP pad	V_{IHMP} SR	(0.73*$V_{EXT/FLEX}$)-0.25	-	-	V	Hysteresis active, AL
		1.6 [4]	-	-	V	Hysteresis active, TTL
Input low voltage for MP pad	V_{ILMP} SR	-	-	(0.52*$V_{EXT/FLEX}$)-0.25	V	Hysteresis active, AL
		-	-	0.5 [5]	V	Hysteresis active, TTL
Input low / high voltage for MP pad	V_{ILHMP} CC	1.1	-	1.9	V	Hysteresis inactive
Pad set-up time for MP pad	t_{SET_MP} CC	-	-	100	ns	
Short Circuit current for MP pad [6]	I_{SC} SR	-10	-	10	mA	absolute max value (PSI5)
Deviation of symmetry for rising and falling edges	SYM CC	-	-	20	%	

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.
2) For currents smaller than the $I_{OL/OH}$ from the test condition the defined Max. value stays unchanged.
3) Rise / fall times are defined 10% - 90% of $V_{EXT/FLEX}$.
4) V_{IHx} = 0.27 * $V_{EXT/FLEX}$ + 0.545V
5) V_{ILx} = 0.17 * $V_{EXT/FLEX}$
6) The values are only valid if the pad is not used during operation, otherwise I_{SC} defines the limits for operation.

Table 3-11 Class MP+ 5V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input frequency	f_{IN} SR	-	-	75	MHz	Hysteresis active
		-	-	150	MHz	Hysteresis inactive
Input hysteresis for MP+ pad [1]	$HYSMPP$ CC	0.09 * $V_{EXT/FLEX}$	-	-	V	AL
		0.075 * $V_{EXT/FLEX}$	-	-	V	TTL
Input leakage current for MP+ pad	I_{OZMPP} CC	-750	-	750	nA	(0.1*$V_{EXT/FLEX}$) < V_{IN} < (0.9*$V_{EXT/FLEX}$)
		-1500	-	1500	nA	else
Pull-up current for MP+ pad	I_{PUHMPP} CC	|30|	-	-	µA	V_{IHmin}; AL
		|43|	-	-	µA	V_{IHmin}; TTL
		-	-	|107|	µA	V_{ILmax}; AL and TTL
Pull-down current for MP+ pad	I_{PDLMPP} CC	-	-	|100|	µA	V_{IHmin}; AL and TTL
		|46|	-	-	µA	V_{ILmax}; AL
		|21|	-	-	µA	V_{ILmax}; TTL

Table 3-16 Class I 5V (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Pull-down current for I pad	I_{PDLI} CC	-	-	|100|	µA	V_{IHmin}; AL and TTL
		|46|	-	-	µA	V_{ILmax}; AL
		|21|	-	-	µA	V_{ILmax}; TTL
Input Leakage Current for I pad	I_{OZI} CC	-150	-	150	nA	$(0.1*V_{EXT/FLEX}) < V_{IN} < (0.9*V_{EXT/FLEX})$
		-350	-	350	nA	else
Input high voltage for I pad	V_{IHI} SR	2.03 [2]	-	-	V	Hysteresis active, TTL
		$(0.73*V_{EXT/FLEX})$-0.25	-	-	V	Hysteresis active; AL; not available for the $\overline{\text{PORST}}$ pad
Input low voltage for I pad	V_{ILI} SR	-	-	0.8 [3]	V	Hysteresis active, TTL
		-	-	$(0.52*V_{EXT/FLEX})$-0.25	V	Hysteresis active; AL; not available for the $\overline{\text{PORST}}$ pad
Input low / high voltage for I pad	V_{ILHI} CC	1.85	-	3.0	V	Hysteresis inactive
Pad set-up time for I pad	t_{SETI} CC	-	-	100	ns	

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.

2) $V_{IHx} = 0.27 * V_{EXT/FLEX} + 0.545V$

3) $V_{ILx} = 0.17 * V_{EXT/FLEX}$

Table 3-17 Class I 3.3V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input frequency	f_{IN} SR	-	-	50	MHz	Hysteresis active
		-	-	100	MHz	Hysteresis inactive
Input Hysteresis for I pad [1]	*HYSI* CC	0.045 * $V_{EXT/FLEX}$	-	-	V	$\overline{\text{PORST}}$ pad only
		0.05 * $V_{EXT/FLEX}$	-	-	V	AL and TTL
Pull-up current for I pad	I_{PUHI} CC	|17|	-	-	µA	V_{IHmin}; AL
		|19|	-	-	µA	V_{IHmin}; TTL
		-	-	|75|	µA	V_{ILmax}; AL and TTL
Pull-down current for I pad	I_{PDLI} CC	-	-	|75|	µA	V_{IHmin}; AL and TTL
		|22|	-	-	µA	V_{ILmax}; AL
		|11|	-	-	µA	V_{ILmax}; TTL
Input Leakage Current for I pad	I_{OZI} CC	-150	-	150	nA	$(0.1*V_{EXT/FLEX}) < V_{IN} < (0.9*V_{EXT/FLEX})$
		-350	-	350	nA	else

Table 3-25 LVDSH - IEEE standard LVDS reduced link (REDL) (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input differential threshold	V_{idth} SR	-100	-	100	mV	Driver ground potential difference < 50 mV
Change in VOS between 0 and 1	*dVOS* CC	-	-	25	mV	RT = 100 Ohm ±5%
Change in Vod between 0 and 1	*dVod* CC	-	-	25	mV	RT = 100 Ohm ±5%
Duty cycle	t_{duty} CC	45	-	55	%	
V_{OD} Fall time 1)	t_{fall10} CC	-	-	0.5	ns	ZL = 100 Ohm ±5% @ 2pF
V_{OD} Rise time 1)	t_{rise10} CC	-	-	0.5	ns	ZL = 100 Ohm ±5% @ 2pF

1) Rise / fall times are defined for 10% - 90% of V_{OD}

default after start-up = CMOS function

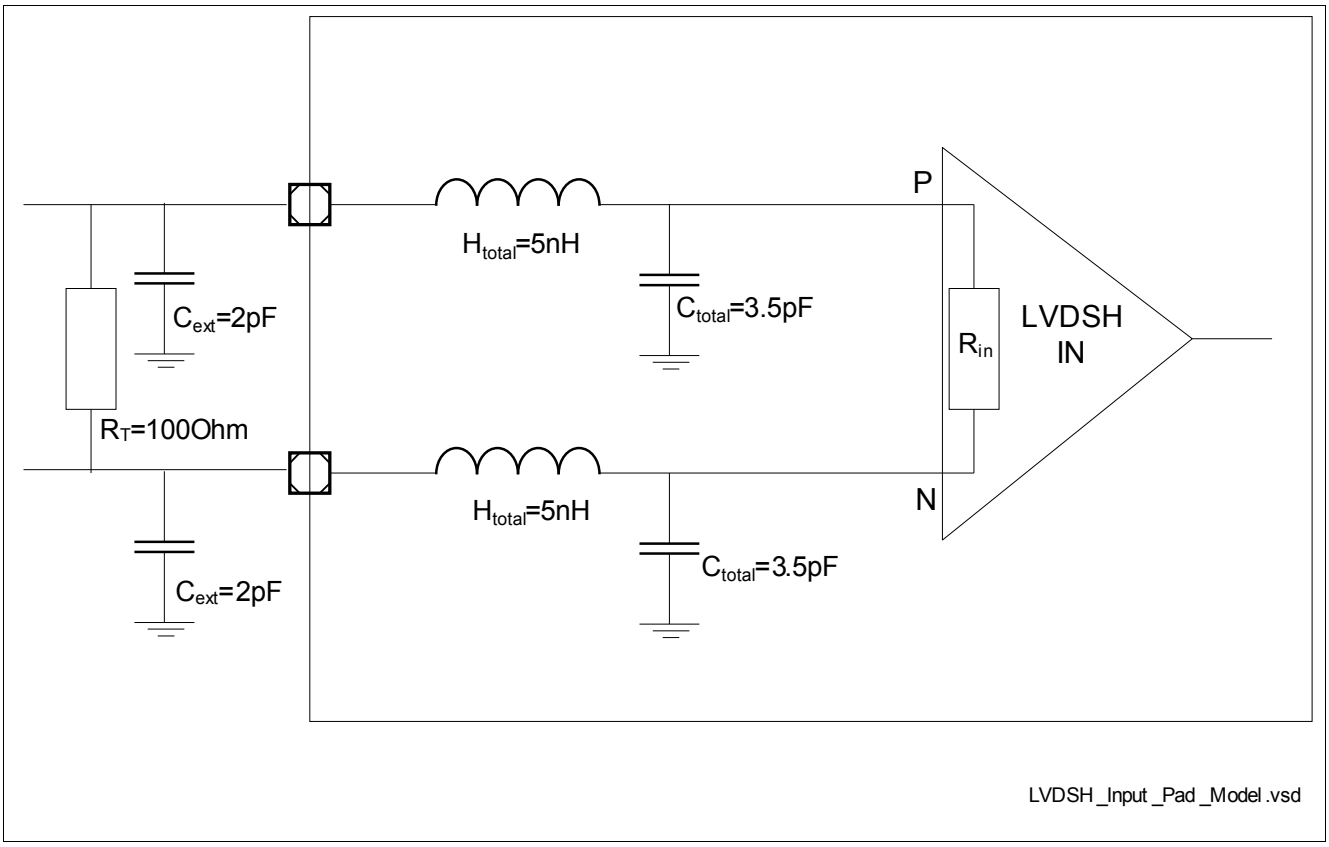

Figure 3-1 LVDSH pad Input model

4) The regulator that supplies V_{EXT} should ensure that V_{EXT} is in the operational region before PORST is externally released by the regulator. Incase of 5V nominal supply, it should be ensured that V_{EXT} > 4V before PORST is released. Incase of 3.3V nominal supply , it should be ensured that V_{EXT} > 3V before PORST is released. The additional minimum PORST hold time is required as an additional mechanism to avoid consecutive PORST toggling owing to slow supply slopes or residual supply ramp-ups. It is also required to activate external PORST atleast 100us before power-fail is recognised to avoid consecutive PORST toggling on a power fail event.
5) This parameter includes the delay of the analog spike filter in the $\overline{\text{PORST}}$ pad.

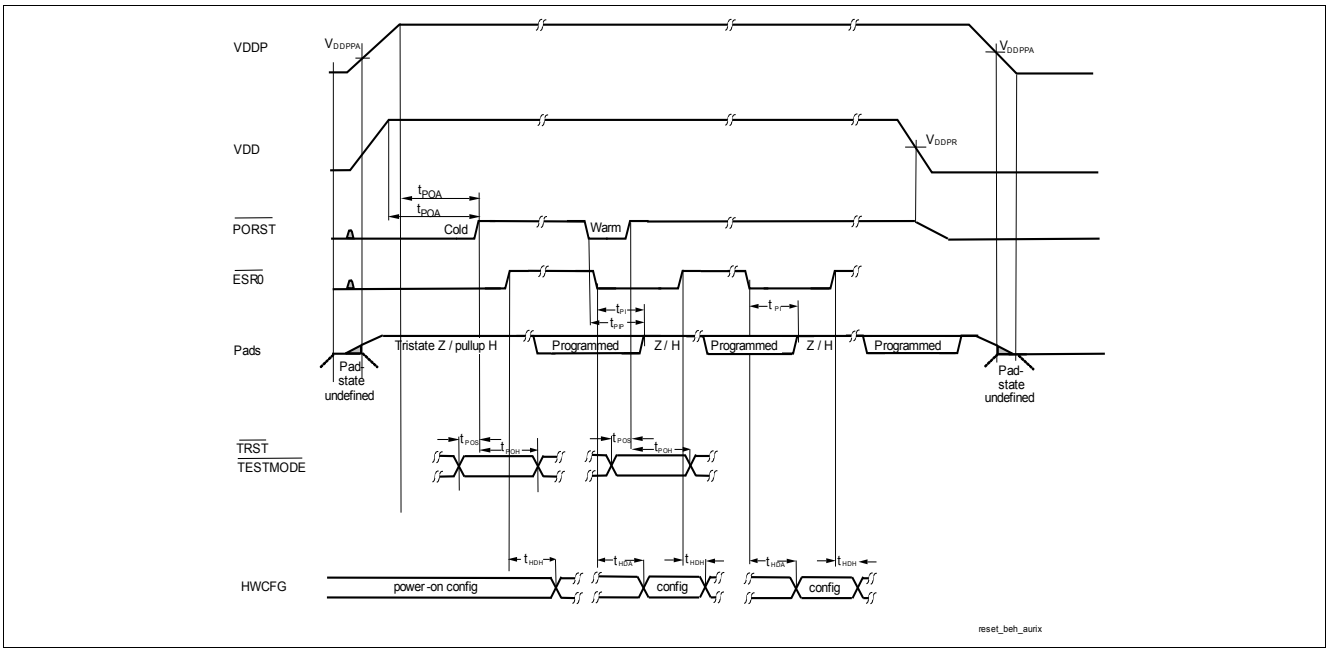

Figure 3-8 Power, Pad and Reset Timing

4) For compensation of the average on-chip delay the QSPI module provides the bit fields ECONz.A, B and C.
5) The setup and hold times are valid for both settings of the input pads thresholds: TTL and AL.

Table 3-62 Master Mode timing MPss output pads for data and clock, CL=50pF

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCLKO clock period [1]	t_{50} CC	40	-	-	ns	C_L=50pF
Deviation from the ideal duty cycle [2] [3]	t_{500} CC	-2	-	3.5+0.035 * C_L	ns	0 < C_L < 200pF
MTSR delay from SCLKO shifting edge	t_{51} CC	-8	-	8	ns	C_L=50pF
SLSOn deviation from the ideal programmed position	t_{510} CC	-8	-	8	ns	MPss; C_L=50pF
		-1	-	15	ns	MP+sm; C_L=50pF
		0	-	50	ns	MP+m, MPm, LPm; C_L=50pF
MRST setup to SCLK latching edge [4]	t_{52} SR	40 [4][5]	-	-	ns	C_L=50pF
MRST hold from SCLK latching edge	t_{53} SR	-5 [4][5]	-	-	ns	C_L=50pF

1) Documented value is valid for master transmit or slave receive only. For full duplex the external SPI counterpart timing has to be taken into account.
2) The PLL jitter is not included. It should be considered additionally, corresponding to the used baudrate. The duty cycle can be adjusted using the bit fields ECONz.A, B and C with the finest granularity of T_{MAX} = 1 / f_{MAX}.
3) Positive deviation lenghtens the high time and shortens the low time of a clock period. Negative deviation does the opposite.
4) For compensation of the average on-chip delay the QSPI module provides the bit fields ECONz.A, B and C.
5) The setup and hold times are valid for both settings of the input pads thresholds: TTL and AL.

Table 3-63 Master Mode timing MPsm output pads

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCLKO clock period [1]	t_{50} CC	100	-	-	ns	C_L=50pF
Deviation from the ideal duty cycle [2] [3]	t_{500} CC	-3	-	4+0.04 * C_L	ns	0 < C_L < 200pF
MTSR delay from SCLKO shifting edge	t_{51} CC	-11	-	10	ns	C_L=50pF
SLSOn deviation from the ideal programmed position	t_{510} CC	-11	-	10	ns	C_L=50pF
MRST setup to SCLK latching edge [4]	t_{52} SR	60 [4][5]	-	-	ns	C_L=50pF
MRST hold from SCLK latching edge	t_{53} SR	-10 [4][5]	-	-	ns	C_L=50pF

1) Documented value is valid for master transmit or slave receive only. For full duplex the external SPI counterpart timing has to be taken into account.

Table 3-76 MPss clock/data (LVDS pads in CMOS mode, option EN01) (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SOPx output delay 6)	t_{44} CC	-4	-	7	ns	MPss; C_L=50pF
ENx output delay 6)	t_{45} CC	-6	-	7	ns	MP+ss/MPRss; C_L=50pF
		-2	-	16.5	ns	MP+sm/MPRsm; C_L=50pF
		-4	-	10	ns	MPss; C_L=50pF
		0	-	32	ns	MPsm; C_L=50pF; except pin P13.0
		0	-	32	ns	MPsm; C_L=50pF; pin P13.0
		5	-	45	ns	MPm/MP+m/MPRm; C_L=50pF
		-11	-	7.5	ns	MP+ss/MPRss; C_L=0pF
		-4	-	13	ns	MP+sm/MPRsm; C_L=0pF
		-10	-	7	ns	MPss; C_L=0pF
		-1	-	22	ns	MPsm; C_L=0pF
		-2	-	25	ns	MP+m/MPm/MPRm; C_L=0pF
SDI bit time	t_{46} CC	8 * t_{MSC}	-	-	ns	Upstream Timing
SDI rise time 7)	t_{48} SR	-	-	200	ns	Upstream Timing
SDI fall time 7)	t_{49} SR	-	-	200	ns	Upstream Timing

1) FCLP signal rise/fall times are the rise/fall times of the LVDSM pads, and the high/low times are min 1 * T_A.
2) T_A depends on the clock source selected for baud rate generation in the ABRA block of the MSC.
3) FCLP signal high and low can be minimum 1 * T_{MSC}.
4) The PLL jitter is not included. It should be considered additionally, corresponding to the used baudrate. The duty cycle can be adjusted if the ABRA block is used.
5) Positive deviation lenghtens the high time and shortens the low time of a clock period. Negative deviation does the opposite.
6) From FCLP rising edge.
7) When using slow and asymmetrical edges, like in case of open drain upstream connection, the application must take care that the bit is long enough (the baud rate is low enough) so that under worst case conditions the three sampling points in the middle of the bit are not violated.

Table 3-77 MP+sm/MPRsm clock/data

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
FCLPx clock period 1)	t_{40} CC	2 * T_A	-	-	ns	MP+sm/MPRsm; C_L=50pF
Deviation from ideal duty cycle 2) 3)	t_{400} CC	-3	-	3+0.01 * C_L	ns	MP+sm/MPRsm; 0 < C_L < 200pF

3.28.4 ETH RMII Parameters

In the following, the parameters of the RMII (Reduced Media Independent Interface) are described.

Table 3-85 ETH RMII Signal Timing Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
ETH_RMII_REF_CL clock period	t_{13} CC	20	-	-	ns	C_L=25pF; 50ppm
ETH_RMII_REF_CL clock high time	t_{14} CC	7 [1]	-	13 [2]	ns	C_L=25pF
ETH_RMII_REF_CL clock low time	t_{15} CC	7 [1]	-	13 [2]	ns	C_L=25pF
ETHTXEN, ETHTXD[1:0], ETHRXD[1:0], ETHCRSDV, ETHRXER; setup time	t_{16} CC	4	-	-	ns	C_L=25pF
ETHTXEN, ETHTXD[1:0], ETHRXD[1:0], ETHCRSDV, ETHRXER; hold time	t_{17} CC	2	-	-	ns	C_L=25pF

1) Defined by 35% of clock period.

2) Defined by 65% of clock period.

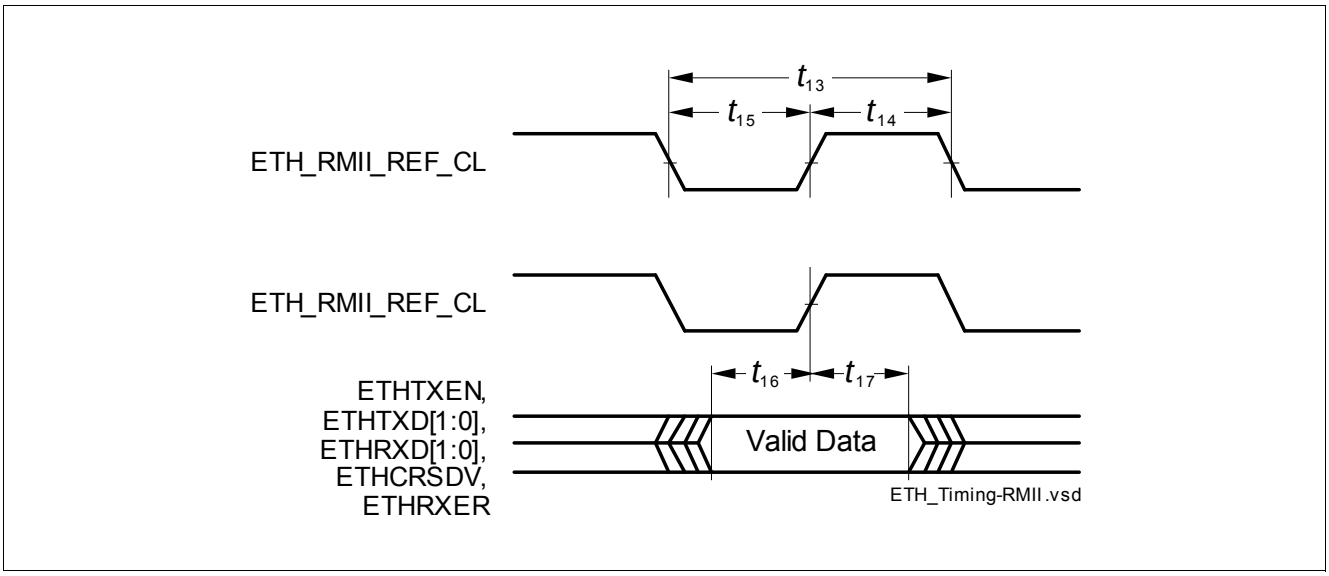

Figure 3-28 ETH RMII Signal Timing

4 History

Version 0.6 is the first version of this document.

4.1 Changes from version version 0.6 to 0.71

- Changes in table 'Timings for 1.8V imager, 3.3V+-5% pad power supply, TTL input level' of CIF
  - Add min 3.5 ns to t_{72}
  - Add min 3.5 ns to t_{74}
  - Add min 3 ns to t_{71}
  - Add min 3 ns to t_{73}
  - Add min 3.5 ns to t_{71}
  - Add min 3.5 ns to t_{73}
  - Add min 4 ns to t_{74}
  - Add min 5 ns to t_{72}
  - Add min 4 ns to t_{72}
  - Add min 5 ns to t_{74}
  - Add min 10.42 ns to t_{70}
  - Add min 9 ns to t_{71}
  - Add min 10 ns to t_{72}
  - Add min 9 ns to t_{73}
  - Add min 10 ns to t_{74}
  - Add min 4.5 ns to t_{71}
  - Add min 4.5 ns to t_{73}
- Changes in table 'Timings for 0.4V to 2.4V input signals (2.8V imager), +-5% pad power supply' of CIF
  - Add min 3.5 ns to t_{74}
  - Add min 3 ns to t_{71}
  - Add min 3 ns to t_{73}
  - Add min 3.5 ns to t_{72}
  - Add min 5 ns to t_{74}
  - Add min 10.42 ns to t_{70}
  - Add min 9 ns to t_{71}
  - Add min 10 ns to t_{72}
  - Add min 9 ns to t_{73}
  - Add min 10 ns to t_{74}
  - Add min 4.5 ns to t_{71}
  - Add min 4.5 ns to t_{73}
  - Add min 5 ns to t_{72}
- Changes in table 'Timings for 1.8V imager, TTL input level' of CIF
  - Add min 3 ns to t_{71}
  - Add min 3.5 ns to t_{74}
  - Add min 3.5 ns to t_{72}

  - Change note of K_{OVAP} from '' to '5mA < I_{IN} < 0mA'
  - Change note of K_{OVAN} from 'Analog Inputs overlaid with class LP pads or pull down diagnostics' to 'Analog Inputs overlaid with class LP pads or pull down diagnostics; -1mA < I_{IN} < 0mA'
  - Change max value of K_{OVDN} from 1.4*10^{-2} to 1.5*10^{-2}
  - Add max 3*10^{-3} to K_{OVAN}
- DSADC
  - Change description of I_{OZ5} from 'Positive reference pin leakage' to 'Positive reference V_{AREF1} pin leakage'
  - Change description of I_{OZ6} from 'Negative reference pin leakage' to 'Negative reference V_{AGND1} pin leakage'
  - Change min value of ED_{GAIN} from -0.1 % to -0.2 %
  - Change max value of ED_{GAIN} from 0.1 % to 0.2 %
  - Change min value of ED_{OFF} from -350 mV to -100 mV
  - Add max 100 mV to ED_{OFF}
  - Change typ value of ED_{OFF} from -150 mV to mV
  - Change note of SNR from 'f_{PB} = 30kHz' to 'f_{PB} = 30 kHz; V_{DDM} = ±5%'
  - Change min value of SNR from 76 dB to 80 dB
  - Change note of SNR from 'f_{PB} = 50kHz' to 'f_{PB} = 50 kHz; V_{DDM} = ±5%'
  - Change min value of SNR from 74 dB to 78 dB
  - Add footnote 'Single-ended mode reduces the SNR by 6 dB if the unused input is grounded, by 3 dB if the unused input connects to V_{CM} (GAIN = 2).' to SNR
  - Remove footnote 'Single-ended mode reduces the SNR by 6 dB if the unused input is grounded, by 3 dB if the unused input connects to V_{CM} (GAIN = 2).' from SNR
  - Change min value of ED_{GAIN} from -5 % to -3.5 %
  - Change max value of ED_{GAIN} from 5 % to 3.5 %
  - Change note of R_{DAIN} from 'Exact value (+-1%) available in UCB' to 'Exact value (±1%) available in UCB'
  - Add footnote 'The variation of the impedance between different channels is < 1.5%.' to R_{DAIN}
  - Change note of R_{DAIN} from 'Exact value (+-1%) available in UCB' to 'Exact value (±1%) available in UCB'
  - Change note of R_{DAIN} from 'Exact value (+-1%) available in UCB' to 'Exact value (±1%) available in UCB'
  - Change note of SNR from 'f_{PB} = 100kHz' to 'f_{PB} = 100 kHz; V_{DDM} = ±5%'
  - Change min value of SNR from 69 dB to 74 dB
  - Remove footnote '10 kHz only with 10MHz Modulator clock frequency reachable' from f_{PB}
  - Add footnote '10 kHz only reachable with 10 MHz modulator clock frequency.' to f_{PB}
  - Change note of SBA from '1,5 ... 2 f_D' to '1.5 ... 2 f_D'
  - Remove footnote 'Derating factors:
-2 dB in standard-performance mode.
-3 dB for CMV = 10$_B$, i.e. V_{CM} = (V_{AREF}±2%) / 2.0.' from SBA
  - Add footnote 'CIC3, FIR0, FIR1 filters enabled.' to SBA
  - Change note of SBA from '2,5 ... OSR/2 f_D' to '2.5 ... OSR/2 f_D'
  - Change note of SBA from '0,5 ... 1 f_D' to '0.5 ... 1 f_D'
  - Change note of SFDR from 'VCM = 2.2V, DC coupled' to 'V_{CM} = 2.2 V, DC coupled; V_{DDM} = ±10%'
  - Add footnote 'Derating factors:
-2 dB in standard-performance mode.
-3 dB for CMV = 10$_B$, i.e. V_{CM} = (V_{AREF}±2%) / 2.0.' to $SFDR$

  - Add typ 0.207 + 0.003 * (S [KByte]) / (f_{FSI} [MHz]) s to t_{ERP}
  - Add typ 0.12 + 0.08/(f_{FSI} [MHz]) s to t_{ERD}
  - Add typ 0.207 + 0.003 * (S [KByte]) / (f_{FSI} [MHz]) s to t_{MERP}
  - Add typ 0.12 + 0.01 * (S [KByte]) / (f_{FSI} [MHz]) s to t_{MERD}
  - Add typ 0.57 + 0.15/(f_{FSI} [MHz]) s to t_{ERD}
  - Add typ 0.57 + 0.019 * (S [KByte]) / (f_{FSI} [MHz]) s to t_{MERD}
- Changes in table 'Class MP+ 3.3V' of Standard_Pads
  - Add 5.42 ns to Class MP+ 3.3V
  - Add 5.9 ns to Class MP+ 3.3V
  - Add 7.65 ns to Class MP+ 3.3V
  - Add 7.36 ns to Class MP+ 3.3V
  - Add 4.8 ns to Class MP+ 3.3V
  - Add 5.32 ns to Class MP+ 3.3V
  - Add max 5.42 ns to t_{MPP}
  - Add max 5.9 ns to t_{MPP}
  - Add max 7.65 ns to t_{MPP}
  - Add max 7.36 ns to t_{MPP}
  - Add max 4.8 ns to t_{MPP}
  - Add max 5.32 ns to t_{MPP}

4.2 Changes from version version 0.71 to 1.0

- DSADC
  - Change min value of I_{OZ6} from -2 % to -3 µA %
- DSADC_33V
  - Change min value of ED_{GAIN} from -0.2 % to -0.3 %
  - Change max value of ED_{GAIN} from 0.2 % to 0.3 %
  - Change min value of I_{OZ6} from -2 % to -3 µA %
- Changes in table 'Overload Parameters' of Overload
  - Change min value of I_{INANA} from -1 mA to -3 mA
  - Change note of K_{OVAN} from 'else; -1mA < I_{IN} < 0mA' to 'else; -5mA < I_{IN} < 0mA'
  - Change note of K_{OVAN} from '-5mA < I_{IN} < -1mA' to 'Analog Inputs overlaid with class LP pads or pull down diagnostics; -5mA < I_{IN} < -1mA'
  - Change max value of K_{OVAN} from $3*10^{-3}$ to $1*10^{-2}$
- Reset Timings
  - Change max value of t_{BP} from 1.1 ms to 1.11 ms
- VADC
  - Change typ value of Q_{CONV} from 3 pC to 10 pC
  - Change typ value of Q_{CONV} from 14 pC to 50 pC
  - Change min value of I_{OZ3} from -1 µA to -2.5 µA
  - Change note of EN_{RMS} from 'target' to ''
  - Change max value of Q_{CONV} from 20 pC to 75 pC