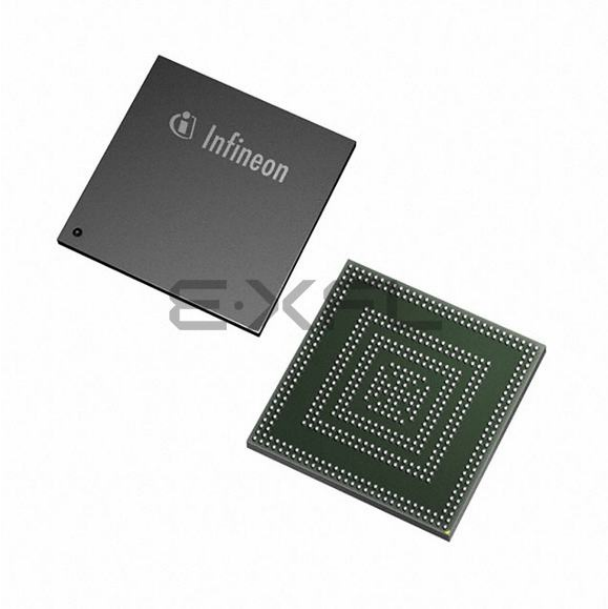
Infineon Technologies - TC299TX128F300SBBKXUMA1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	TriCore™
Core Size	32-Bit Tri-Core
Speed	300MHz
Connectivity	ASC, CANbus, Ethernet, FlexRay, HSSL, I²C, LINbus, MSC, PSI5, QSPI, SENT
Peripherals	DMA, WDT
Number of I/O	263
Program Memory Size	8MB (8M x 8)
Program Memory Type	FLASH
EEPROM Size	384K x 8
RAM Size	728K x 8
Voltage - Supply (Vcc/Vdd)	3.3V, 5V
Data Converters	A/D 84x12b, 10 x Sigma-Delta
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	516-LFBGA
Supplier Device Package	PG-LFBGA-516-5
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/tc299tx128f300sbbkxuma1

Table 2-2 Port 01 Functions (cont'd)

Pin	Symbol	Ctrl	Type	Function
P10	P01.7	I	**MP / PU1 / VEXT**	General-purpose input
	TIN115			GTM input
	SCLK3C			QSPI3 input
	DSITR8F			DSADC channel 8 input F
	P01.7	O0		General-purpose output
	TOUT115	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	SCLK3	O4		QSPI3 output
	–	O5		Reserved
	–	O6		Reserved
	–	O7		Reserved
L1	P01.8	I	**LP / PU1 / VEXT**	General-purpose input
	TIN162			GTM input
	DSDIN9A			DSADC channel 9 input A
	SENT12B			SENT input
	ARX0C			ASCLIN0 input
	RXDCAN0F			CAN node 0 input
	RXDCANr0E			CAN node 0 input (MultiCANr+)
	RXD1B1			ERAY1 input
	P01.8	O0		General-purpose output
	TOUT162	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	–	O4		Reserved
	–	O5		Reserved
	–	O6		Reserved
	–	O7		Reserved

Table 2-4 Port 10 Functions (cont'd)

Pin	Symbol	Ctrl	Type	Function
A6	P10.13	I	**LP / PU1 / VEXT**	General-purpose input
	TIN268			GTM input
	SENT13C			SENT input
	P10.13	O0		General-purpose output
	TOUT268	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	–	O4		Reserved
	–	O5		Reserved
	–	O6		Reserved
	–	O7		Reserved
B5	P10.14	I	**LP / PU1 / VEXT**	General-purpose input
	TIN267			GTM input
	SENT12C			SENT input
	P10.14	O0		General-purpose output
	TOUT267	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	–	O4		Reserved
	–	O5		Reserved
	–	O6		Reserved
	–	O7		Reserved
A5	P10.15	I	**LP / PU1 / VEXT**	General-purpose input
	TIN270			GTM input
	P10.15	O0		General-purpose output
	TOUT270	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	–	O4		Reserved
	–	O5		Reserved
	–	O6		Reserved
	–	O7		Reserved

Table 2-8 Port 14 Functions (cont'd)

Pin	Symbol	Ctrl	Type	Function
A20	P14.11	I	**LP / PU1 / VEXT**	General-purpose input
	TIN258			GTM input
	P14.11	O0		General-purpose output
	TOUT258	O1		GTM output
	END20	O2		MSC2 output
	PSITX4	O3		PSI5 output
	EN22	O4		MSC2 output
	SOP2	O5		MSC2 output
	–	O6		Reserved
	–	O7		Reserved
B19	P14.12	I	**LP / PU1 / VEXT**	General-purpose input
	TIN261			GTM input
	SDI20			MSC2 input
	P14.12	O0		General-purpose output
	TOUT261	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	–	O4		Reserved
	–	O5		Reserved
	–	O6		Reserved
	–	O7		Reserved
A19	P14.13	I	**MP+ / PU1 / VEXT**	General-purpose input
	TIN260			GTM input
	P14.13	O0		General-purpose output
	TOUT260	O1		GTM output
	END23	O2		MSC2 output
	–	O3		Reserved
	EN21	O4		MSC2 output
	–	O5		Reserved
	–	O6		Reserved
	–	O7		Reserved

Table 2-11 Port 21 Functions (cont'd)

Pin	Symbol	Ctrl	Type	Function
R24	P21.2	I	**LVDSH_N/ PU1 / VDDP3**	General-purpose input
	TIN53			GTM input
	MRST2CN			QSPI2 input (LVDS)
	MRST4CN			QSPI4 input (LVDS)
	ARX3GN			ASCLIN3 input (LVDS)
	EMGSTOPB			SCU input
	RXDN			HSCT input (LVDS)
	P21.2	O0		General-purpose output
	TOUT53	O1		GTM output
	ASLSO3	O2		ASCLIN3 output
	–	O3		Reserved
	–	O4		Reserved
	ETHMDC	O5		ETH output
	SDRAMA8	O6		EBU output
	–	O7		Reserved
P24	P21.3	I	**LVDSH_P/ PU1 / VDDP3**	General-purpose input
	TIN54			GTM input
	MRST2CP			QSPI2 input (LVDS)
	MRST4CP			QSPI4 input (LVDS)
	ARX3GP			ASCLIN3 input (LVDS)
	RXDP			HSCT input (LVDS)
	P21.3	O0		General-purpose output
	TOUT54	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	–	O4		Reserved
	–	O5		Reserved
	SDRAMA9	O6		EBU output
	–	O7		Reserved
	ETHMDIOD	HWOUT		ETH input/output

Table 2-15 Port 25 Functions (cont'd)

Pin	Symbol	Ctrl	Type	Function
W29	P25.6	I	**A2 / PU1 / VEBU**	General-purpose input
	P25.6	O0		General-purpose output
	TOUT212	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	–	O4		Reserved
	–	O5		Reserved
	–	O6		Reserved
	–	O7		Reserved
	CKE	HWOUT		EBU output
AD29	P25.7	I	**A2 / PU1 / VEBU**	General-purpose input
	TIN213			GTM input
	P25.7	O0		General-purpose output
	TOUT213	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	–	O4		Reserved
	–	O5		Reserved
	–	O6		Reserved
	–	O7		Reserved
	$\overline{\text{ADV}}$	HWOUT		EBU output
	$\overline{\text{CAS}}$			EBU output
AC29	P25.8	I	**A2 / PU1 / VEBU**	General-purpose input
	TIN214			GTM input
	P25.8	O0		General-purpose output
	TOUT214	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	–	O4		Reserved
	A23	O5		EBU output
	SDRAMA0	O6		EBU output
	–	O7		Reserved
	$\overline{\text{BC0}}$	HWOUT		EBU output

Table 2-28 Port 01 Functions (cont'd)

Pin	Symbol	Ctrl	Type	Function
J1	P01.9	I	**LP / PU1 / VEXT**	General-purpose input
	TIN160			GTM input
	DSCIN9A			DSADC channel 9 input A
	SENT11B			SENT input
	P01.9	O0		General-purpose output
	TOUT160	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	–	O4		Reserved
	–	O5		Reserved
	DSCOUT9	O6		DSADC channel 9 output
	–	O7		Reserved
K2	P01.10	I	**LP / PU1 / VEXT**	General-purpose input
	TIN163			GTM input
	DSITR9F			DSADC channel 9 input F
	SENT13B			SENT input
	P01.10	O0		General-purpose output
	TOUT163	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	–	O4		Reserved
	–	O5		Reserved
	–	O6		Reserved
	–	O7		Reserved
K1	P01.11	I	**LP / PU1 / VEXT**	General-purpose input
	TIN165			GTM input
	DSITR9E			DSADC channel 9 input E
	SENT14B			SENT input
	P01.11	O0		General-purpose output
	TOUT165	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	–	O4		Reserved
	–	O5		Reserved
	–	O6		Reserved
	–	O7		Reserved

Table 2-31 Port 11 Functions (cont'd)

Pin	Symbol	Ctrl	Type	Function
B9	P11.13	I	**LP / PU1 / VFLEX**	General-purpose input
	TIN125			GTM input
	ETHRXERA			ETH input
	SDA1A			I2C1 input
	P11.13	O0		General-purpose output
	TOUT125	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	–	O4		Reserved
	–	O5		Reserved
	SDA1	O6		I2C1 output
	–	O7		Reserved
C8	P11.14	I	**LP / PU1 / VFLEX**	General-purpose input
	TIN126			GTM input
	ETHCRSDVB			ETH input
	ETHRXDVB			ETH input
	ETHCRSA			ETH input
	SCL1A			I2C1 input
	P11.14	O0		General-purpose output
	TOUT126	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	–	O4		Reserved
	–	O5		Reserved
	SCL1	O6		I2C1 output
	–	O7		Reserved
C7	P11.15	I	**LP / PU1 / VFLEX**	General-purpose input
	TIN127			GTM input
	ETHCOL			ETH input
	P11.15	O0		General-purpose output
	TOUT127	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	–	O4		Reserved
	–	O5		Reserved
	–	O6		Reserved
	–	O7		Reserved

Table 2-47 Port 34 Functions (cont'd)

Pin	Symbol	Ctrl	Type	Function
AF10	P34.3	I	**LP / PU1 / VEXT**	General-purpose input
	TIN148			GTM input
	P34.3	O0		General-purpose output
	TOUT148	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	SLSO210	O4		QSPI2 output
	–	O5		Reserved
	–	O6		Reserved
	COUT60	O7		CCU60 output
AD10	P34.4	I	**LP / PU1 / VEXT**	General-purpose input
	TIN149			GTM input
	MRST2D			QSPI2 input
	P34.4	O0		General-purpose output
	TOUT149	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	MRST2	O4		QSPI2 output
	–	O5		Reserved
	–	O6		Reserved
	CC61	O7		CCU60 output
AE10	P34.5	I	**LP / PU1 / VEXT**	General-purpose input
	TIN150			GTM input
	MTSR2D			QSPI2 input
	P34.5	O0		General-purpose output
	TOUT150	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	MTSR2	O4		QSPI2 output
	–	O5		Reserved
	–	O6		Reserved
	COUT61	O7		CCU60 output

Table 2-49 Analog Inputs (cont'd)

Pin	Symbol	Ctrl	Type	Function
AA2	AN26	I	**S / HighZ / VDDM**	Analog input 26
	VADCG3.2			VADC analog input channel 2 of group 3 (MD)
	SENT2A			SENT input channel 2, pin A
AB2	AN27	I	**S / HighZ / VDDM**	Analog input 27
	VADCG3.3			VADC analog input channel 3 of group 3 (with pull down diagnostics)
	SENT3A			SENT input channel 3, pin A
AB1	AN28	I	**D / HighZ / VDDM**	Analog input 28
	VADCG3.4			VADC analog input channel 4 of group 3 (with pull down diagnostics)
AC1	AN29	I	**D / HighZ / VDDM**	Analog input 29
	VADCG3.5			VADC analog input channel 5 of group 3 (with pull down diagnostics)
W3	AN32	I	**S / HighZ / VDDM**	Analog input 32
	VADCG4.0			VADC analog input channel 0 of group 4
	SENT4A			SENT input channel 4, pin A
Y3	AN33	I	**S / HighZ / VDDM**	Analog input 33
	VADCG4.1			VADC analog input channel 1 of group 4 (MD)
	SENT5A			SENT input channel 5, pin A
V4	AN36	I	**S / HighZ / VDDM**	Analog input 34
	VADCG4.4			VADC analog input channel 4 of group 4
	DS3PA			DSADC: positive analog input of channel 3, pin A
	SENT6A			SENT input channel 6, pin A
V3	AN37	I	**S / HighZ / VDDM**	Analog input 37
	VADCG4.5			VADC analog input channel 5 of group 4
	DS3NA			DSADC: negative analog input channel 3, pin A
	SENT7A			SENT input channel 7, pin A
U4	AN40	I	**D / HighZ / VDDM**	Analog input 40
	VADCG5.0			VADC analog input channel 0 of group 5
U3	AN41	I	**D / HighZ / VDDM**	Analog input 41
	VADCG5.1			VADC analog input channel 1 of group 5 (MD)
T1	AN42	I	**D / HighZ / VDDM**	Analog input 42
	VADCG5.2			VADC analog input channel 2 of group 5 (MD)
U1	AN43	I	**D / HighZ / VDDM**	Analog input 43
	VADCG5.3			VADC analog input channel 3 of group 5 (with pull down diagnostics)
AD2	AN48	I	**D / HighZ / VDDM**	Analog input 48
	VADCG8.0			VADC analog input channel 0 of group 8

Table 2-60 Port 14 Functions

Pin	Symbol	Ctrl	Type	Function
B16	P14.0	I	**MP+ / PU1 / VEXT**	General-purpose input
	TIN80			GTM input
	SENT12D			SENT input
	P14.0	O0		General-purpose output
	TOUT80	O1		GTM output
	ATX0	O2		ASCLIN0 output Recommended as Boot loader pin
	TXD0A	O3		ERAY0 output
	TXD0B	O4		ERAY0 output
	TXDCAN1	O5		CAN node 1 output Used for single pin DAP (SPD) function
	ASCLK0	O6		ASCLIN0 output
	COUT62	O7		CCU60 output
A15	P14.1	I	**MP / PU1 / VEXT**	General-purpose input
	TIN81			GTM input
	REQ15			SCU input
	SENT13D			SENT input
	ARX0A			ASCLIN0 input Recommended as Boot loader pin
	RXDCAN1B			CAN node 1 input Used for single pin DAP (SPD) function
	RXD0A3			ERAY0 input
	RXD0B3			ERAY0 input
	EVRWUPA			SCU input
	P14.1	O0		General-purpose output
	TOUT81	O1		GTM output
	ATX0	O2		ASCLIN0 output Recommended as Boot loader pin.
	–	O3		Reserved
	–	O4		Reserved
	–	O5		Reserved
	–	O6		Reserved
	COUT63	O7		CCU60 output

Table 2-67 Port 33 Functions

Pin	Symbol	Ctrl	Type	Function
W10	P33.0	I	**LP / PU1 / VEXT**	General-purpose input
	TIN22			GTM input
	DSITR0E			DSADC channel 0 input E
	P33.0	O0		General-purpose output
	TOUT22	O1		GTM output
	–	O2		Reserved
	–	O3		Reserved
	–	O4		Reserved
	–	O5		Reserved
	VADCG2BFL0	O6		VADC output
	–	O7		Reserved
Y10	P33.1	I	**LP / PU1 / VEXT**	General-purpose input
	TIN23			GTM input
	PSIRX0C			PSI5 input
	SENT9C			SENT input
	DSCIN2B			DSADC channel 2 input B
	DSITR1E			DSADC channel 1 input E
	P33.1	O0		General-purpose output
	TOUT23	O1		GTM output
	ASLSO3	O2		ASCLIN3 output
	SCLK2	O3		QSPI2 output
	DSCOUT2	O4		DSADC channel 2 output
	VADCEMUX02	O5		VADC output
	VADCG2BFL1	O6		VADC output
	–	O7		Reserved
W11	P33.2	I	**LP / PU1 / VEXT**	General-purpose input
	TIN24			GTM input
	SENT8C			SENT input
	DSDIN2B			DSADC channel 2 input B
	DSITR2E			DSADC channel 2 input E
	P33.2	O0		General-purpose output
	TOUT24	O1		GTM output
	ASCLK3	O2		ASCLIN3 output
	SLSO210	O3		QSPI2 output
	PSITX0	O4		PSI5 output
	VADCEMUX01	O5		VADC output
	VADCG2BFL2	O6		VADC output
	–	O7		Reserved

Table 2-74 TC29x Bare Die Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
162	P00.15	MP+ / PU1 / VEXT	4419500	100000	GPIO
163	P00.1 (VADC7.5 / DS5NA)	D	4419500	250000	Analog input
164	P00.2 (VADC7.4 / DS5PA)	D	4528000	310000	Analog input
165	P00.3 (VADC7.3)	D	4419500	370000	Analog input
166	VSS	Vx	4528000	425000	Must be bonded to VSS
167	P00.4 (VADC7.2)	D	4419500	480000	Analog input
168	P00.5 (VADC7.1)	D	4528000	540000	Analog input
169	P00.6 (VADC7.0)	D	4419500	600000	Analog input
170	VEXT	Vx	4528000	655000	Must be bonded to VEXT
171	P00.7 (VADC6.5 / DS4NA)	D	4419500	710000	Analog input
172	P00.8 (VADC6.4 / DS4PA)	D	4528000	770000	Analog input
173	P00.9 (VADC6.3)	D	4419500	830000	Analog input
174	P00.10 (VADC6.2)	D	4528000	890000	Analog input
175	P00.11 (VADC6.1)	D	4419500	950000	Analog input
176	VSS	Vx	4528000	1005000	Must be bonded to VSS
177	P00.12 (VADC6.0)	D	4419500	1060000	Analog input
178	VDD	Vx	4528000	1115000	Must be bonded to VDD
179	VSS	Vx	4528000	1215000	Must be bonded to VSS
180	VEXT	Vx	4419500	1265000	Must be bonded to VEXT
181	VSS	Vx	4528000	1315000	Must be bonded to VSS
182	VDD	Vx	4528000	1415000	Must be bonded to VDD
183	VAREF4	Vx	4528000	1535000	Positive Analog Reference Voltage 4
184	VAGND4	Vx	4419500	1585000	Negative Analog Reference Voltage 4
185	VDDM	Vx	4528000	1635000	Must be bonded to VEXT
186	AN47 (VADC5.7 / DS3ND)	S	4419500	1685000	Analog input
187	AN46 (VADC5.6 / DS3PD)	S	4528000	1735000	Analog input
188	AN45 (VADC5.5 / DS3NC)	S	4419500	1785000	Analog input

Table 2-74 TC29x Bare Die Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
255	VAREF1	Vx	3328000	4295000	Positive Analog Reference Voltage 1
256	VSS	Vx	3178000	4186500	Must be bonded to VSS
257	VSSM	Vx	3228000	4295000	Must be bonded to VSS
258	AN14 (VADC1.6)	D	3078000	4186500	Analog input
259	VDDM	Vx	3128000	4295000	Must be bonded to VEXT
260	AN12 (VADC1.4)	D	2978000	4186500	Analog input
261	AN13 (VADC1.5)	D	3028000	4295000	Analog input
262	AN10 (VADC1.2)	D	2878000	4186500	Analog input
263	AN11 (VADC1.3)	D	2928000	4295000	Analog input (with pull down diagnostics)
264	AN8 (VADC1.0)	D	2778000	4186500	Analog input
265	AN9 (VADC1.1)	D	2828000	4295000	Analog input
266	AN6 (VADC0.6)	D	2678000	4186500	Analog input
267	AN7 (VADC0.7)	D	2728000	4295000	Analog input (with pull down diagnostics)
268	AN4 (VADC0.4)	D	2578000	4186500	Analog input
269	AN5 (VADC0.5)	D	2628000	4295000	Analog input
270	AN2 (VADC0.2 / DS0PA)	D	2478000	4186500	Analog input
271	AN3 (VADC0.3 / DS0NA)	D	2528000	4295000	Analog input
272	AN1 (VADC0.1 / DS1NA)	D	2378000	4186500	Analog input
273	VSSM	Vx	2428000	4295000	Must be bonded to VSS
274	AN0 (VADC0.0 / DS1PA)	D	2278000	4186500	Analog input
275	VDDM	Vx	2328000	4295000	Must be bonded to VEXT
276	EVR_OFF	Vx	2158000	4295000	Must be bonded to VSS
277	P33.0	LP / PU1 / VEXT	2103000	4186500	GPIO
278	VSS	Vx	2048000	4295000	Must be bonded to VSS
279	P33.1	LP / PU1 / VEXT	1993000	4186500	GPIO
280	P34.1	LP / PU1 / VEXT	1933000	4295000	GPIO
281	P33.2	LP / PU1 / VEXT	1873000	4186500	GPIO
282	VSS	Vx	1778000	4295000	Must be bonded to VSS
283	VDD	Vx	1678000	4295000	Must be bonded to VDD
284	P33.3	LP / PU1 / VEXT	1583000	4186500	GPIO
285	VEXT	Vx	1509000	4295000	Must be bonded to VEXT
286	VEXT	Vx	1440000	4186500	Must be bonded to VEXT
287	P34.2	LP / PU1 / VEXT	1385000	4295000	GPIO

Column “**Name**”:

Symbolic name of the pad.

The functions mapped on GPIO pads “Px.y” are described in the User’s Manual chapter ”General Purpose I/O Ports and Peripheral I/O LInes (Ports)”

Column “**Type**”:

LP = Pad class LP (5V/3.3V, Class LP parameters for digital input / output and class D parameters for analog input function)
MP = Pad class MP (5V/3.3V)
MP+ = Pad class MP+ (5V/3.3V)
MPR = Pad class MPR (5V/3.3V)
A2 = Pad class A2 (3.3V)
LVDSM = Pad class LVDSM (5V/3.3V)
LVDSH = Pad class LVDSH (3.3V)
S = Pad class S (Class S parameters for digital input and class D parameters for analog input function)
D = Pad class D (VADC / DSADC)
PU = with pull-up device connected during reset ($\overline{\text{PORST}}$ = 0)
PU1 = with pull-up device connected during reset ($\overline{\text{PORST}}$ = 0)[1) 2) 3)]
PD = with pull-down device connected during reset ($\overline{\text{PORST}}$ = 0)
PD1 = with pull-down device connected during reset ($\overline{\text{PORST}}$ = 0)[1) 2) 3)]
PX = Behavior depends on usage: PD in EVR13 SMPS Mode and PU1 in GPIO Mode
OD = open drain during reset ($\overline{\text{PORST}}$ = 0)
HighZ = tri-state during reset ($\overline{\text{PORST}}$ = 0)
PORST = PORST input pad
XTAL1 = XTAL1 input pad
XTAL2 = XTAL2 input pad
VGATE1P = VGATE1P
VGATE3P = VGATE3P
Vx = Supply
NC = These pins are reserved for future extensions and shall not be connected externally
NC1 = These pins are not connected on package level and will not be used for future extensions
NCVDDPSB = This pin has a different functionality in an Production Device and an Emulation Device. For details pls. see Pin/Ball description of this pin.
NCVDDSB = This pin has a different functionality in an Production Device and an Emulation Device. For details pls. see Pin/Ball description of this pin.

Column “**X**” / “**Y**”:

Pad opening center coordinates

2.4.1 Pad Openings

Two different pad openings are used:

1) The default state of GPIOs (Px.y) during and after PORST active is controllled via HWCFG[6] (P14.4). HWCFG[6] has a weak internal pull-up active at start-up if the pin is left unconnected.See also User´s Manual, “Introduction Chapter”, “General Purpose I/O Ports and Peripheral I/O Lines”, Figure: “Default state of port pins during and after reset”.
2) If HWCFG[6] is left unconnected or is externally pulled high, weak internal pull-ups are active at GPIOs (Px.y) pins during and after reset. Exceptions are P33.8 (HighZ), P40.x (default configuration during and after reset: analog inputs, port input funtion disabled), ESR0, P21.6 / P21.7 (port pins overlayed with JTAG functionality).
3) If HWCFG[6] is connected to ground, port pins are predominantly in HighZ during and after reset. Exceptions are P33.8 (HighZ), P40.x (default configuration during and after reset: analog inputs, port input funtion disabled), ESR0, P21.6 / P21.7 (port pins overlayed with JTAG functionality).

Table 3-5 Operating Conditions (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Digital supply voltage for EBU	V_{EBU} SR	2.97	3.3	3.63	V	3.3V pad parameters are valid; only required if externally supplied
Digital external supply voltage for EVR and during Standby mode	V_{EVRSB} SR	2.97	-	5.5	V	
Digital supply voltage for EBU Flex port	V_{FLEXE} SR	2.97	3.3	4.5	V	3.3V pad parameters are valid
		4.5	5.0	5.5	V	5V pad parameters are valid

1) V_{DD} = 1.33V +- 7.5% (with increased nominal V_{DD}) voltage by +2.5%.
2) No external inductive load permissible if EVR is used. All V_{DD} pins shall be connected together externally on the PCB.
3) Voltage overshoot to 1.69V is permissible, provided the duration is less than 2h cumulated. Reduced ADC accuracy and leakage is increased.
4) Voltage overshoot to 6.5V is permissible, provided the duration is less than 2h cumulated. Reduced ADC accuracy and leakage is increased.
5) All V_{EXT} pins shall be connected together externally on the PCB.
6) All V_{DDP3} pins shall be connected together externally on the PCB.
7) Voltage overshoot to 4.29V is permissible, provided the duration is less than 2h cumulated. Reduced ADC accuracy and leakage is increased.
8) This parameter is valid under the assumption the PORST signal is constantly at low level during the power-up/power-down of V_{DDP3}.

Table 3-27 VADC (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Resistance of the pull-down test device [10]	R_{PDD} CC	-	-	0.3	kOhm	
CSD voltage accuracy [11] [12]	$dVCSD$ CC	-	-	10	%	

1) If the reference voltage is reduced by the factor k (k < 1), TUE,DNL,INL,Gain, and Offset errors increase also by the factor 1/k. V_{AREF} must be decoupled with an external capacitor.
2) For QCONV = X pC and a conversion time of 1 µs a rms value of X µA results for I_{AREFx}.
3) For the details of the mapping for a VADC group to pin V_{AREFx} please see the User's Manual.
4) The broken wire detection delay against V_{AGND} is measured in numbers of consecutive precharge cycles at a conversion rate higher than 1 conversion per 500 ms.
5) The broken wire detection delay against V_{AREF} is measured in numbers of consecutive precharge cycles at a conversion rate higher than 1 conversion per 10 ms. This function is influenced by leakage current, in particular at high temperature.
6) Resulting worst case combined error is arithmetic combination of TUE and EN_{RMS}.
7) This parameter is valid for soldered devices and requires careful analog board design.
8) Value is defined for one sigma Gauss distribution.
9) In order to avoid an additional error due to incomplete sampling, the sampling time shall be set greater than 5 * R_{CSD} * C_{AINS}.
10) The pull-down resistor R_{PDD} is connected between the input pad and the analog multiplexer. The input pad itself adds another 200-Ohm series resistance, when measuring through the pin.
11) CSD: Converter Self Diagnostics, for details please consult the User's Manual.
12) Note, that in case CSD voltage is chosen to nom. 1/3 or 2/3 of V_{AREF} voltage, the reference voltage is loaded with a current of max. V_{AREF} / 45 kOhm.

The following VADC parameter are valid for V_{DDM} = 2.97 V to 4.5 V.

This table also covers the parameters for Class D pads.

Table 3-28 VADC_33V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Analog reference voltage [1]	V_{AREF} SR	V_{AGND} + 1.0	-	V_{DDM} + 0.05	V	
Analog reference ground	V_{AGND} SR	V_{SSM} - 0.05	-	V_{SSM} + 0.05	V	
Analog input voltage range	V_{AIN} SR	V_{AGND}	-	V_{AREF}	V	
Converter reference clock	f_{ADCI} SR	2	-	20	MHz	
Charge consumption per conversion [2] [3]	Q_{CONV} CC	-	35	50	pC	V_{AIN} = 3.3 V, charge consumed from reference pin, precharging disabled
		-	8	17	pC	V_{AIN} = 3.3 V, charge consumed from reference pin, precharging enabled
Conversion time for 12-bit result	t_{C12} CC	-	(16 + STC) x t_{ADCI} + 2 x t_{VADC}	-		Includes sample time and post calibration

Table 3-34 Power Supply

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
∑ Sum of I_{DD} 1.3 V core and peripheral supply currents	I_{DD} CC	-	-	750	mA	max power pattern with $f_{SRI/CPUx}$ = 270 MHz with V_{DD} = 1.3V + 10%; valid for Feature Package T, TP, and TC products
		-	-	800	mA	max power pattern with fSRI/CPUx = 300 MHz with VDD = 1.33V + 7.5%. valid for Feature Package T, TP, and TC products
		-	-	950	mA	max power pattern. valid for Feature Package TA and TB products
		-	-	930	mA	max power pattern. valid for Feature Package TX and TY products
		-	-	567	mA	real power pattern. valid for Feature Package T, TP, and TC products
		-	-	637	mA	real power pattern. valid for Feature Package TA, TB, TX and TY products

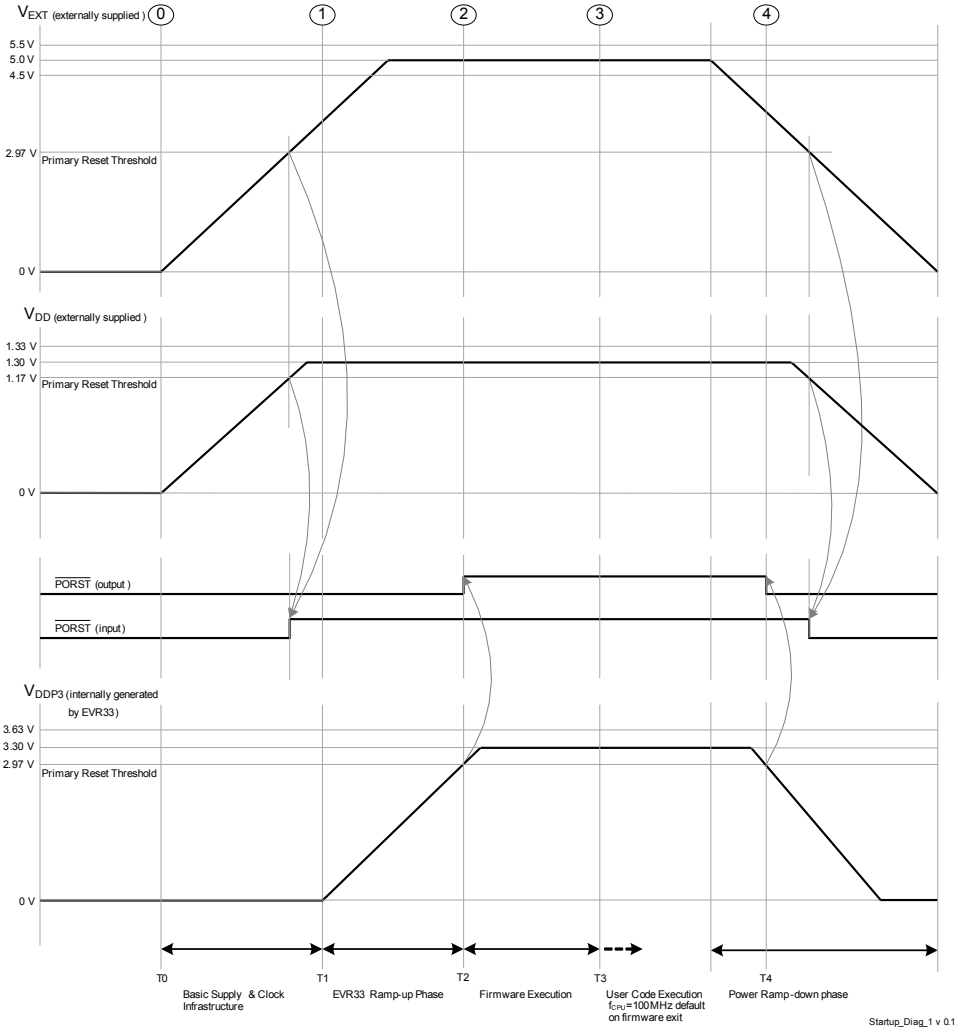

Figure 3-4 External Supply Mode - 5 V and 1.3 V externally supplied

3.19 AC Specifications

All AC parameters are specified for the complette operating range defined in **Chapter 3.4** unless otherwise noted in colum Note / test Condition.

Unless otherwise noted in the figures the timings are defined with the following guidelines:

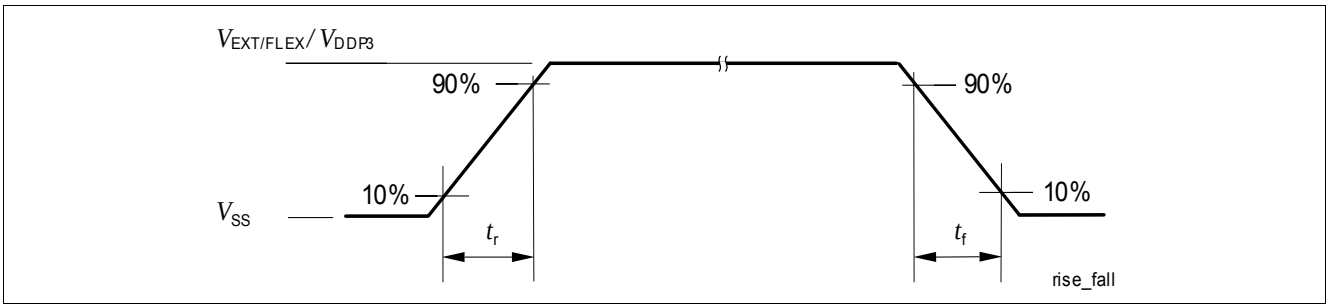

Figure 3-9 Definition of rise / fall times

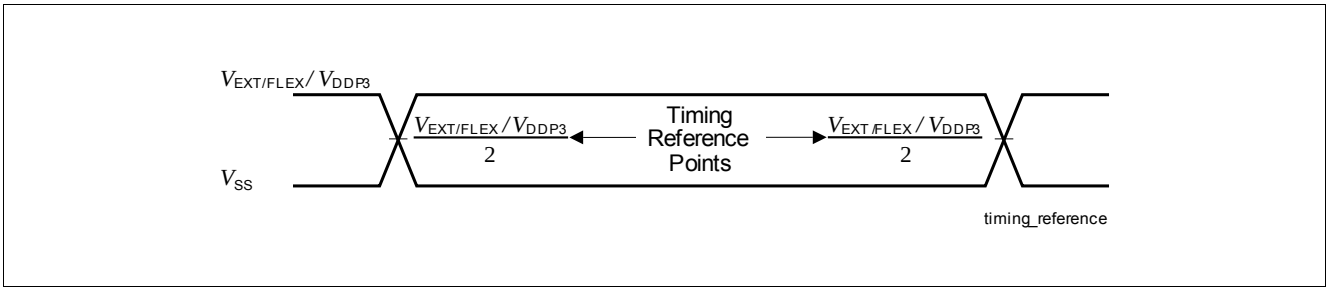

Figure 3-10 Time Reference Point Definition

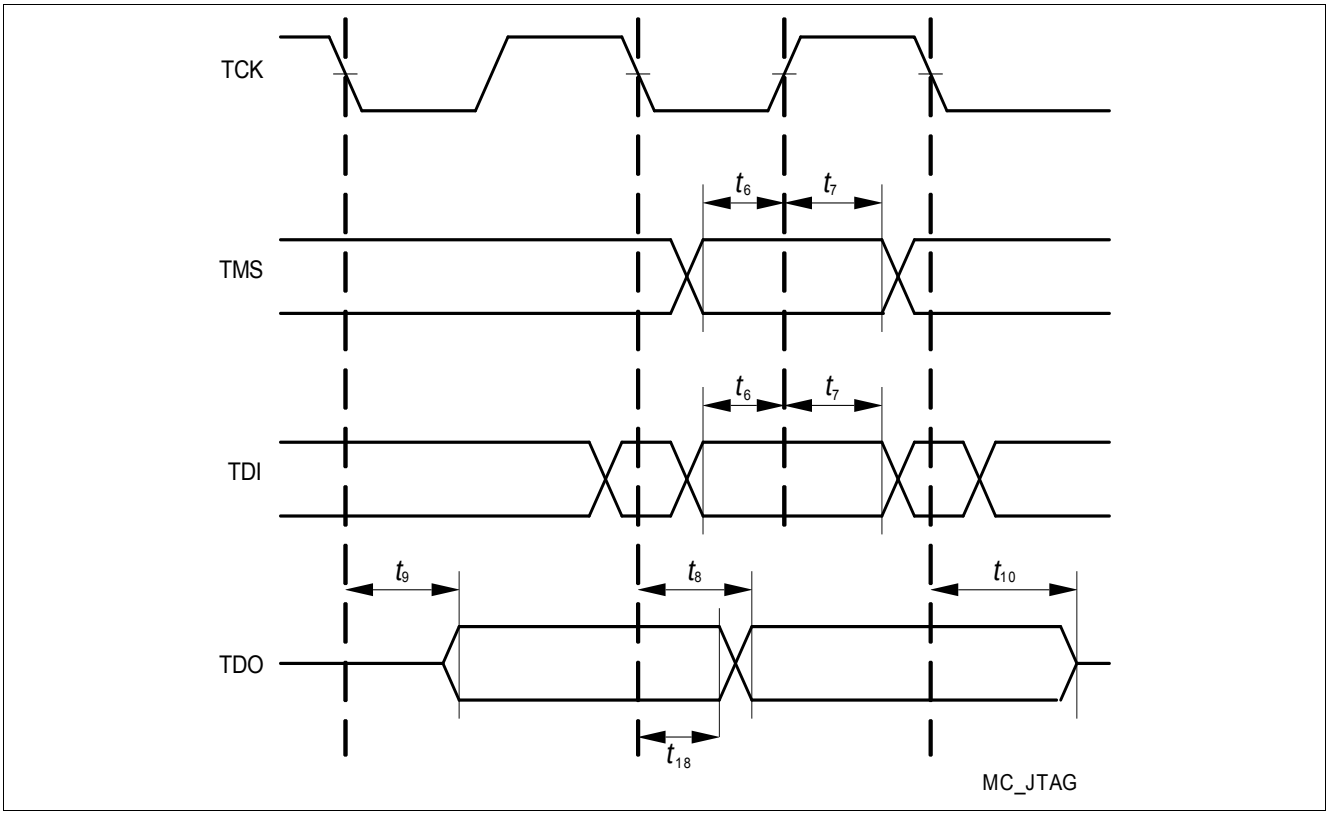

Figure 3-12 JTAG Timing