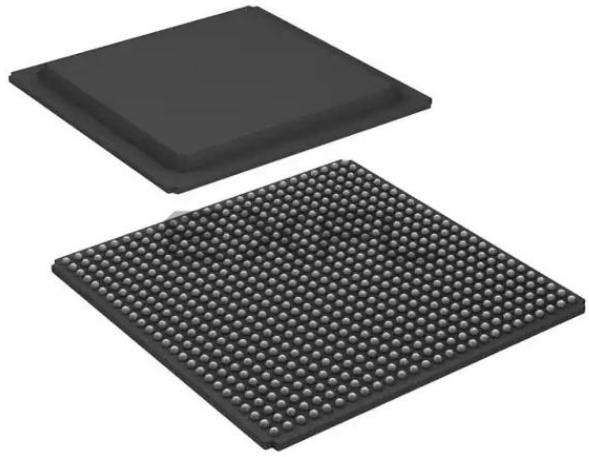
# AMD Xilinx - XCKU3P-L1FFVB676I Datasheet



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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 20340 |
| Number of Logic Elements/Cells | 355950 |
| Total RAM Bits | 31641600 |
| Number of I/O | 280 |
| Number of Gates | - |
| Voltage - Supply | 0.698V ~ 0.876V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 676-BBGA, FCBGA |
| Supplier Device Package | 676-FCBGA (27x27) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xcku3p-l1ffvb676i |

# Quiescent Supply Current

*Table 6:* **Typical Quiescent Supply Current(1)(2)(3)**

| Symbol | Description | Device | Speed Grade and $V_{CCINT}$ Operating Voltages | | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | 0.90V | 0.85V | | 0.72V | | |
| | | | -3 | -2 | -1 | -2 | -1 | |
| $I_{CCINTQ}$ | Quiescent $V_{CCINT}$ supply current. | XCKU3P | 1242 | 1181 | 1181 | 1037 | 1037 | mA |
| | | XCKU5P | 1242 | 1181 | 1181 | 1037 | 1037 | mA |
| | | XCKU9P | 1592 | 1523 | 1523 | 1356 | 1356 | mA |
| | | XCKU11P | 1780 | 1693 | 1693 | 1486 | 1486 | mA |
| | | XCKU13P | 1950 | 1864 | 1864 | 1658 | 1658 | mA |
| | | XCKU15P | 2677 | 2559 | 2559 | 2275 | 2275 | mA |
| $I_{CCINT\_IOQ}$ | Quiescent $V_{CCINT\_IO}$ supply current. | XCKU3P | 61 | 59 | 59 | 59 | 59 | mA |
| | | XCKU5P | 61 | 59 | 59 | 59 | 59 | mA |
| | | XCKU9P | 61 | 59 | 59 | 59 | 59 | mA |
| | | XCKU11P | 120 | 115 | 115 | 115 | 115 | mA |
| | | XCKU13P | 61 | 59 | 59 | 59 | 59 | mA |
| | | XCKU15P | 164 | 158 | 158 | 158 | 158 | mA |
| $I_{CCOQ}$ | Quiescent $V_{CCO}$ supply current. | All devices | 1 | 1 | 1 | 1 | 1 | mA |
| $I_{CCAUXQ}$ | Quiescent $V_{CCAUX}$ supply current. | XCKU3P | 153 | 153 | 153 | 153 | 153 | mA |
| | | XCKU5P | 153 | 153 | 153 | 153 | 153 | mA |
| | | XCKU9P | 227 | 227 | 227 | 227 | 227 | mA |
| | | XCKU11P | 255 | 255 | 255 | 255 | 255 | mA |
| | | XCKU13P | 266 | 266 | 266 | 266 | 266 | mA |
| | | XCKU15P | 396 | 396 | 396 | 396 | 396 | mA |
| $I_{CCAUX\_IOQ}$ | Quiescent $V_{CCAUX\_IO}$ supply current. | XCKU3P | 32 | 32 | 32 | 32 | 32 | mA |
| | | XCKU5P | 32 | 32 | 32 | 32 | 32 | mA |
| | | XCKU9P | 33 | 33 | 33 | 33 | 33 | mA |
| | | XCKU11P | 56 | 56 | 56 | 56 | 56 | mA |
| | | XCKU13P | 33 | 33 | 33 | 33 | 33 | mA |
| | | XCKU15P | 74 | 74 | 74 | 74 | 74 | mA |
| $I_{CCBRAMQ}$ | Quiescent $V_{CCBRAM}$ supply current. | XCKU3P | 18 | 17 | 17 | 17 | 17 | mA |
| | | XCKU5P | 18 | 17 | 17 | 17 | 17 | mA |
| | | XCKU9P | 25 | 24 | 24 | 24 | 24 | mA |
| | | XCKU11P | 23 | 22 | 22 | 22 | 22 | mA |
| | | XCKU13P | 29 | 28 | 28 | 28 | 28 | mA |
| | | XCKU15P | 37 | 35 | 35 | 35 | 35 | mA |

**Notes:**

1. Typical values are specified at nominal voltage, 85°C junction temperatures ($T_j$) with single-ended SelectIO™ resources.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at www.xilinx.com/power) to estimate static power consumption for conditions other than those specified.

# DC Input and Output Levels

Values for $V_{IL}$ and $V_{IH}$ are recommended input voltages. Values for $I_{OL}$ and $I_{OH}$ are guaranteed over the recommended operating conditions at the $V_{OL}$ and $V_{OH}$ test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum $V_{CCO}$ with the respective $V_{OL}$ and $V_{OH}$ voltage levels shown. Other standards are sample tested.

*Table 9:* **SelectIO DC Input and Output Levels For HD I/O Banks(1)(2)(3)**

| I/O Standard | $V_{IL}$ | | $V_{IH}$ | | $V_{OL}$ | $V_{OH}$ | $I_{OL}$ | $I_{OH}$ |
|---|---|---|---|---|---|---|---|---|
| | V, Min | V, Max | V, Min | V, Max | V, Max | V, Min | mA | mA |
| HSTL_I | –0.300 | $V_{REF}$ – 0.100 | $V_{REF}$ + 0.100 | $V_{CCO}$ + 0.300 | 0.400 | $V_{CCO}$ – 0.400 | 8.0 | –8.0 |
| HSTL_I_18 | –0.300 | $V_{REF}$ – 0.100 | $V_{REF}$ + 0.100 | $V_{CCO}$ + 0.300 | 0.400 | $V_{CCO}$ – 0.400 | 8.0 | –8.0 |
| HSUL_12 | –0.300 | $V_{REF}$ – 0.130 | $V_{REF}$ + 0.130 | $V_{CCO}$ + 0.300 | 20% $V_{CCO}$ | 80% $V_{CCO}$ | 0.1 | –0.1 |
| LVCMOS12 | –0.300 | 35% $V_{CCO}$ | 65% $V_{CCO}$ | $V_{CCO}$ + 0.300 | 0.400 | $V_{CCO}$ – 0.400 | Note 4 | Note 4 |
| LVCMOS15 | –0.300 | 35% $V_{CCO}$ | 65% $V_{CCO}$ | $V_{CCO}$ + 0.300 | 0.450 | $V_{CCO}$ – 0.450 | Note 5 | Note 5 |
| LVCMOS18 | –0.300 | 35% $V_{CCO}$ | 65% $V_{CCO}$ | $V_{CCO}$ + 0.300 | 0.450 | $V_{CCO}$ – 0.450 | Note 5 | Note 5 |
| LVCMOS25 | –0.300 | 0.700 | 1.700 | $V_{CCO}$ + 0.300 | 0.400 | $V_{CCO}$ – 0.400 | Note 5 | Note 5 |
| LVCMOS33 | –0.300 | 0.800 | 2.000 | 3.400 | 0.400 | $V_{CCO}$ – 0.400 | Note 5 | Note 5 |
| LVTTL | –0.300 | 0.800 | 2.000 | 3.400 | 0.400 | 2.400 | Note 5 | Note 5 |
| SSTL12 | –0.300 | $V_{REF}$ – 0.100 | $V_{REF}$ + 0.100 | $V_{CCO}$ + 0.300 | $V_{CCO}$/2 – 0.150 | $V_{CCO}$/2 + 0.150 | 14.25 | –14.25 |
| SSTL135 | –0.300 | $V_{REF}$ – 0.090 | $V_{REF}$ + 0.090 | $V_{CCO}$ + 0.300 | $V_{CCO}$/2 – 0.150 | $V_{CCO}$/2 + 0.150 | 8.9 | –8.9 |
| SSTL135_II | –0.300 | $V_{REF}$ – 0.090 | $V_{REF}$ + 0.090 | $V_{CCO}$ + 0.300 | $V_{CCO}$/2 – 0.150 | $V_{CCO}$/2 + 0.150 | 13.0 | –13.0 |
| SSTL15 | –0.300 | $V_{REF}$ – 0.100 | $V_{REF}$ + 0.100 | $V_{CCO}$ + 0.300 | $V_{CCO}$/2 – 0.175 | $V_{CCO}$/2 + 0.175 | 8.9 | –8.9 |
| SSTL15_II | –0.300 | $V_{REF}$ – 0.100 | $V_{REF}$ + 0.100 | $V_{CCO}$ + 0.300 | $V_{CCO}$/2 – 0.175 | $V_{CCO}$/2 + 0.175 | 13.0 | –13.0 |
| SSTL18_I | –0.300 | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 | $V_{CCO}$ + 0.300 | $V_{CCO}$/2 – 0.470 | $V_{CCO}$/2 + 0.470 | 8.0 | –8.0 |
| SSTL18_II | –0.300 | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 | $V_{CCO}$ + 0.300 | $V_{CCO}$/2 – 0.600 | $V_{CCO}$/2 + 0.600 | 13.4 | –13.4 |
| MIPI_DPHY_DCI_LP(6) | –0.300 | 0.550 | 0.880 | $V_{CCO}$ + 0.300 | 0.050 | 1.100 | 0.01 | –0.01 |

**Notes:**

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).
3. POD10 and POD12 DC input and output levels are shown in Table 11, Table 15, Table 16, and Table 17.
4. Supported drive strengths of 4, 8, or 12 mA in HD I/O banks.
5. Supported drive strengths of 4, 8, 12, or 16 mA in HD I/O banks.
6. Low-power option for MIPI_DPHY_DCI.

*Table 10:* **SelectIO DC Input and Output Levels for HP I/O Banks(1)(2)(3)**

| I/O Standard | $V_{IL}$ | | $V_{IH}$ | | $V_{OL}$ | $V_{OH}$ | $I_{OL}$ | $I_{OH}$ |
|---|---|---|---|---|---|---|---|---|
| | V, Min | V, Max | V, Min | V, Max | V, Max | V, Min | mA | mA |
| HSTL_I | –0.300 | $V_{REF}$ – 0.100 | $V_{REF}$ + 0.100 | $V_{CCO}$ + 0.300 | 0.400 | $V_{CCO}$ – 0.400 | 5.8 | –5.8 |
| HSTL_I_12 | –0.300 | $V_{REF}$ – 0.080 | $V_{REF}$ + 0.080 | $V_{CCO}$ + 0.300 | 25% $V_{CCO}$ | 75% $V_{CCO}$ | 4.1 | –4.1 |
| HSTL_I_18 | –0.300 | $V_{REF}$ – 0.100 | $V_{REF}$ + 0.100 | $V_{CCO}$ + 0.300 | 0.400 | $V_{CCO}$ – 0.400 | 6.2 | –6.2 |
| HSUL_12 | –0.300 | $V_{REF}$ – 0.130 | $V_{REF}$ + 0.130 | $V_{CCO}$ + 0.300 | 20% $V_{CCO}$ | 80% $V_{CCO}$ | 0.1 | –0.1 |
| LVCMOS12 | –0.300 | 35% $V_{CCO}$ | 65% $V_{CCO}$ | $V_{CCO}$ + 0.300 | 0.400 | $V_{CCO}$ – 0.400 | Note 4 | Note 4 |
| LVCMOS15 | –0.300 | 35% $V_{CCO}$ | 65% $V_{CCO}$ | $V_{CCO}$ + 0.300 | 0.450 | $V_{CCO}$ – 0.450 | Note 5 | Note 5 |
| LVCMOS18 | –0.300 | 35% $V_{CCO}$ | 65% $V_{CCO}$ | $V_{CCO}$ + 0.300 | 0.450 | $V_{CCO}$ – 0.450 | Note 5 | Note 5 |
| LVDCI_15 | –0.300 | 35% $V_{CCO}$ | 65% $V_{CCO}$ | $V_{CCO}$ + 0.300 | 0.450 | $V_{CCO}$ – 0.450 | 7.0 | –7.0 |
| LVDCI_18 | –0.300 | 35% $V_{CCO}$ | 65% $V_{CCO}$ | $V_{CCO}$ + 0.300 | 0.450 | $V_{CCO}$ – 0.450 | 7.0 | –7.0 |
| SSTL12 | –0.300 | $V_{REF}$ – 0.100 | $V_{REF}$ + 0.100 | $V_{CCO}$ + 0.300 | $V_{CCO}$/2 – 0.150 | $V_{CCO}$/2 + 0.150 | 8.0 | –8.0 |
| SSTL135 | –0.300 | $V_{REF}$ – 0.090 | $V_{REF}$ + 0.090 | $V_{CCO}$ + 0.300 | $V_{CCO}$/2 – 0.150 | $V_{CCO}$/2 + 0.150 | 9.0 | –9.0 |
| SSTL15 | –0.300 | $V_{REF}$ – 0.100 | $V_{REF}$ + 0.100 | $V_{CCO}$ + 0.300 | $V_{CCO}$/2 – 0.175 | $V_{CCO}$/2 + 0.175 | 10.0 | –10.0 |
| SSTL18_I | –0.300 | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 | $V_{CCO}$ + 0.300 | $V_{CCO}$/2 – 0.470 | $V_{CCO}$/2 + 0.470 | 7.0 | –7.0 |
| MIPI_DPHY_DCI_LP(6) | –0.300 | 0.550 | 0.880 | $V_{CCO}$ + 0.300 | 0.050 | 1.100 | 0.01 | –0.01 |

**Notes:**

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).
3. POD10 and POD12 DC input and output levels are shown in Table 11, Table 15, Table 16, and Table 17.
4. Supported drive strengths of 2, 4, 6, or 8 mA in HP I/O banks.
5. Supported drive strengths of 2, 4, 6, 8, or 12 mA in HP I/O banks.
6. Low-power option for MIPI_DPHY_DCI.

*Table 11:* **DC Input Levels for Single-ended POD10 and POD12 I/O Standards(1)(2)**

| I/O Standard | $V_{IL}$ | | $V_{IH}$ | |
|---|---|---|---|---|
| | V, Min | V, Max | V, Min | V, Max |
| POD10 | –0.300 | $V_{REF}$ – 0.068 | $V_{REF}$ + 0.068 | $V_{CCO}$ + 0.300 |
| POD12 | –0.300 | $V_{REF}$ – 0.068 | $V_{REF}$ + 0.068 | $V_{CCO}$ + 0.300 |

**Notes:**

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

*Table 12:* **Differential SelectIO DC Input and Output Levels**

| I/O Standard | $V_{ICM}$ (V)(1) | | | $V_{ID}$(V)(2) | | | $V_{ILHS}$(3) | $V_{IHHS}$(3) | $V_{OCM}$(V)(4) | | | $V_{OD}$(V)(5) | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max | Min | Max | Min | Typ | Max | Min | Typ | Max |
| SUB_LVDS(8) | 0.500 | 0.900 | 1.300 | 0.070 | – | – | – | – | 0.700 | 0.900 | 1.100 | 0.100 | 0.150 | 0.200 |
| LVPECL | 0.300 | 1.200 | 1.425 | 0.100 | 0.350 | 0.600 | – | – | – | – | – | – | – | – |
| SLVS_400_18 | 0.070 | 0.200 | 0.330 | 0.140 | – | 0.450 | – | – | – | – | – | – | – | – |
| SLVS_400_25 | 0.070 | 0.200 | 0.330 | 0.140 | – | 0.450 | – | – | – | – | – | – | – | – |
| MIPI_DPHY_DCI_HS(9) | 0.070 | – | 0.330 | 0.070 | – | – | –0.040 | 0.460 | 0.150 | 0.200 | 0.250 | 0.140 | 0.200 | 0.270 |

**Notes:**

1. $V_{ICM}$ is the input common mode voltage.
2. $V_{ID}$ is the input differential voltage (Q – $\overline{Q}$).
3. $V_{IHHS}$ and $V_{ILHS}$ are the single-ended input high and low voltages, respectively.
4. $V_{OCM}$ is the output common mode voltage.
5. $V_{OD}$ is the output differential voltage (Q – $\overline{Q}$).
6. LVDS_25 is specified in Table 18.
7. LVDS is specified in Table 19.
8. Only the SUB_LVDS receiver is supported in HD I/O banks.
9. High-speed option for MIPI_DPHY_DCI. The $V_{ID}$ maximum is aligned with the standard's specification. A higher $V_{ID}$ is acceptable as long as the $V_{IN}$ specification is also met.

*Table 13:* **Complementary Differential SelectIO DC Input and Output Levels for HD I/O Banks**

| I/O Standard | $V_{ICM}$ (V)(1) | | | $V_{ID}$ (V)(2) | | $V_{OL}$ (V)(3) | $V_{OH}$ (V)(4) | $I_{OL}$ | $I_{OH}$ |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Max | Min | mA | mA |
| DIFF_HSTL_I | 0.300 | 0.750 | 1.125 | 0.100 | – | 0.400 | $V_{CCO}$ – 0.400 | 8.0 | –8.0 |
| DIFF_HSTL_I_18 | 0.300 | 0.900 | 1.425 | 0.100 | – | 0.400 | $V_{CCO}$ – 0.400 | 8.0 | –8.0 |
| DIFF_HSUL_12 | 0.300 | 0.600 | 0.850 | 0.100 | – | 20% $V_{CCO}$ | 80% $V_{CCO}$ | 0.1 | –0.1 |
| DIFF_SSTL12 | 0.300 | 0.600 | 0.850 | 0.100 | – | ($V_{CCO}$/2) – 0.150 | ($V_{CCO}$/2) + 0.150 | 14.25 | –14.25 |
| DIFF_SSTL135 | 0.300 | 0.675 | 1.000 | 0.100 | – | ($V_{CCO}$/2) – 0.150 | ($V_{CCO}$/2) + 0.150 | 8.9 | –8.9 |
| DIFF_SSTL135_II | 0.300 | 0.675 | 1.000 | 0.100 | – | ($V_{CCO}$/2) – 0.150 | ($V_{CCO}$/2) + 0.150 | 13.0 | –13.0 |
| DIFF_SSTL15 | 0.300 | 0.750 | 1.125 | 0.100 | – | ($V_{CCO}$/2) – 0.175 | ($V_{CCO}$/2) + 0.175 | 8.9 | –8.9 |
| DIFF_SSTL15_II | 0.300 | 0.750 | 1.125 | 0.100 | – | ($V_{CCO}$/2) – 0.175 | ($V_{CCO}$/2) + 0.175 | 13.0 | –13.0 |
| DIFF_SSTL18_I | 0.300 | 0.900 | 1.425 | 0.100 | – | ($V_{CCO}$/2) – 0.470 | ($V_{CCO}$/2) + 0.470 | 8.0 | –8.0 |
| DIFF_SSTL18_II | 0.300 | 0.900 | 1.425 | 0.100 | – | ($V_{CCO}$/2) – 0.600 | ($V_{CCO}$/2) + 0.600 | 13.4 | –13.4 |

**Notes:**

1. $V_{ICM}$ is the input common mode voltage.
2. $V_{ID}$ is the input differential voltage.
3. $V_{OL}$ is the single-ended low-output voltage.
4. $V_{OH}$ is the single-ended high-output voltage.

# FPGA Logic Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Kintex UltraScale+ FPGAs. These values are subject to the same guidelines as the AC Switching Characteristics, page 16. In each table, the I/O bank type is either high performance (HP) or high density (HD).

*Table 23:* **LVDS Component Mode Performance**

| Description | I/O Bank Type | Speed Grade and $V_{CCINT}$ Operating Voltages | | | | | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 0.90V | | 0.85V | | | | 0.72V | | | | |
| | | -3 | | -2 | | -1 | | -2 | | -1 | | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| LVDS TX DDR (OSERDES 4:1, 8:1) | HP | 0 | 1250 | 0 | 1250 | 0 | 1250 | 0 | 1250 | 0 | 1250 | Mb/s |
| LVDS TX SDR (OSERDES 2:1, 4:1) | HP | 0 | 625 | 0 | 625 | 0 | 625 | 0 | 625 | 0 | 625 | Mb/s |
| LVDS RX DDR (ISERDES 1:4, 1:8)(1) | HP | 0 | 1250 | 0 | 1250 | 0 | 1250 | 0 | 1250 | 0 | 1250 | Mb/s |
| LVDS RX DDR | HD | 0 | 250 | 0 | 250 | 0 | 250 | 0 | 250 | 0 | 250 | Mb/s |
| LVDS RX SDR (ISERDES 1:2, 1:4)(1) | HP | 0 | 625 | 0 | 625 | 0 | 625 | 0 | 625 | 0 | 625 | Mb/s |
| LVDS RX SDR | HD | 0 | 125 | 0 | 125 | 0 | 125 | 0 | 125 | 0 | 125 | Mb/s |

**Notes:**

1. LVDS receivers are typically bounded with certain applications to achieve maximum performance. Package skews are not included and should be removed through PCB routing.

*Table 24:* **LVDS Native Mode Performance(1)(2)**

| Description | DATA_WIDTH | I/O Bank Type | Speed Grade and $V_{CCINT}$ Operating Voltages | | | | | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0.90V | | 0.85V | | | | 0.72V | | | | |
| | | | -3 | | -2 | | -1 | | -2 | | -1 | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| LVDS TX DDR (TX_BITSLICE) | 4 | HP | 375 | 1600 | 375 | 1600 | 375 | 1260 | 375 | 1400 | 375 | 1260 | Mb/s |
| | 8 | | 375 | 1600 | 375 | 1600 | 375 | 1260 | 375 | 1600 | 375 | 1260 | Mb/s |
| LVDS TX SDR (TX_BITSLICE) | 4 | HP | 187.5 | 800 | 187.5 | 800 | 187.5 | 630 | 187.5 | 700 | 187.5 | 630 | Mb/s |
| | 8 | | 187.5 | 800 | 187.5 | 800 | 187.5 | 630 | 187.5 | 800 | 187.5 | 630 | Mb/s |
| LVDS RX DDR (RX_BITSLICE)(3) | 4 | HP | 375 | 1600 | 375 | 1600 | 375 | 1260 | 375 | 1400 | 375 | 1260 | Mb/s |
| | 8 | | 375 | 1600 | 375 | 1600 | 375 | 1260 | 375 | 1600 | 375 | 1260 | Mb/s |
| LVDS RX SDR (RX_BITSLICE)(3) | 4 | HP | 187.5 | 800 | 187.5 | 800 | 187.5 | 630 | 187.5 | 700 | 187.5 | 630 | Mb/s |
| | 8 | | 187.5 | 800 | 187.5 | 800 | 187.5 | 630 | 187.5 | 800 | 187.5 | 630 | Mb/s |

**Notes:**

1. Native mode is supported through the High-Speed SelectIO Interface Wizard available with the Vivado Design Suite. The performance values assume a source-synchronous interface.
2. PLL settings can restrict the minimum allowable data rate. For example, when using the PLL with CLKOUTPHY_MODE = VCO_HALF the minimum frequency is PLL_FVCOMIN/2.
3. LVDS receivers are typically bounded with certain applications to achieve maximum performance. Package skews are not included and should be removed through PCB routing.

# IOB High Performance (HP) Switching Characteristics

*Table 29:* **IOB High Performance (HP) Switching Characteristics**

| I/O Standards | $T_{INBUF\_DELAY\_PAD\_I}$ | | | | | $T_{OUTBUF\_DELAY\_O\_PAD}$ | | | | | $T_{OUTBUF\_DELAY\_TD\_PAD}$ | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0.90V | 0.85V | | 0.72V | | 0.90V | 0.85V | | 0.72V | | 0.90V | 0.85V | | 0.72V | | |
| | -3 | -2 | -1 | -2 | -1 | -3 | -2 | -1 | -2 | -1 | -3 | -2 | -1 | -2 | -1 | |
| DIFF_HSTL_I_12_F | 0.394 | 0.394 | 0.402 | 0.394 | 0.402 | 0.423 | 0.423 | 0.443 | 0.423 | 0.443 | 0.553 | 0.553 | 0.582 | 0.553 | 0.582 | ns |
| DIFF_HSTL_I_12_M | 0.394 | 0.394 | 0.402 | 0.394 | 0.402 | 0.552 | 0.552 | 0.583 | 0.552 | 0.583 | 0.641 | 0.641 | 0.679 | 0.641 | 0.679 | ns |
| DIFF_HSTL_I_12_S | 0.394 | 0.394 | 0.402 | 0.394 | 0.402 | 0.752 | 0.752 | 0.800 | 0.752 | 0.800 | 0.813 | 0.813 | 0.868 | 0.813 | 0.868 | ns |
| DIFF_HSTL_I_18_F | 0.319 | 0.319 | 0.339 | 0.319 | 0.339 | 0.456 | 0.456 | 0.474 | 0.456 | 0.474 | 0.576 | 0.576 | 0.606 | 0.576 | 0.606 | ns |
| DIFF_HSTL_I_18_M | 0.319 | 0.319 | 0.339 | 0.319 | 0.339 | 0.570 | 0.570 | 0.603 | 0.570 | 0.603 | 0.653 | 0.653 | 0.692 | 0.653 | 0.692 | ns |
| DIFF_HSTL_I_18_S | 0.319 | 0.319 | 0.339 | 0.319 | 0.339 | 0.782 | 0.782 | 0.834 | 0.782 | 0.834 | 0.816 | 0.816 | 0.871 | 0.816 | 0.871 | ns |
| DIFF_HSTL_I_DCI_12_F | 0.394 | 0.394 | 0.402 | 0.394 | 0.402 | 0.406 | 0.406 | 0.429 | 0.406 | 0.429 | 0.534 | 0.534 | 0.564 | 0.534 | 0.564 | ns |
| DIFF_HSTL_I_DCI_12_M | 0.394 | 0.394 | 0.402 | 0.394 | 0.402 | 0.557 | 0.557 | 0.587 | 0.557 | 0.587 | 0.653 | 0.653 | 0.694 | 0.653 | 0.694 | ns |
| DIFF_HSTL_I_DCI_12_S | 0.394 | 0.394 | 0.402 | 0.394 | 0.402 | 0.755 | 0.755 | 0.806 | 0.755 | 0.806 | 0.842 | 0.842 | 0.907 | 0.842 | 0.907 | ns |
| DIFF_HSTL_I_DCI_18_F | 0.323 | 0.323 | 0.339 | 0.323 | 0.339 | 0.445 | 0.445 | 0.461 | 0.445 | 0.461 | 0.566 | 0.566 | 0.595 | 0.566 | 0.595 | ns |
| DIFF_HSTL_I_DCI_18_M | 0.323 | 0.323 | 0.339 | 0.323 | 0.339 | 0.555 | 0.555 | 0.586 | 0.555 | 0.586 | 0.643 | 0.643 | 0.684 | 0.643 | 0.684 | ns |
| DIFF_HSTL_I_DCI_18_S | 0.323 | 0.323 | 0.339 | 0.323 | 0.339 | 0.762 | 0.762 | 0.818 | 0.762 | 0.818 | 0.836 | 0.836 | 0.900 | 0.836 | 0.900 | ns |
| DIFF_HSTL_I_DCI_F | 0.397 | 0.397 | 0.417 | 0.397 | 0.417 | 0.431 | 0.431 | 0.445 | 0.431 | 0.445 | 0.555 | 0.555 | 0.575 | 0.555 | 0.575 | ns |
| DIFF_HSTL_I_DCI_M | 0.397 | 0.397 | 0.417 | 0.397 | 0.417 | 0.553 | 0.553 | 0.583 | 0.553 | 0.583 | 0.644 | 0.644 | 0.684 | 0.644 | 0.684 | ns |
| DIFF_HSTL_I_DCI_S | 0.397 | 0.397 | 0.417 | 0.397 | 0.417 | 0.767 | 0.767 | 0.823 | 0.767 | 0.823 | 0.848 | 0.848 | 0.912 | 0.848 | 0.912 | ns |
| DIFF_HSTL_I_F | 0.404 | 0.404 | 0.417 | 0.404 | 0.417 | 0.423 | 0.423 | 0.443 | 0.423 | 0.443 | 0.549 | 0.549 | 0.581 | 0.549 | 0.581 | ns |
| DIFF_HSTL_I_M | 0.404 | 0.404 | 0.417 | 0.404 | 0.417 | 0.555 | 0.555 | 0.586 | 0.555 | 0.586 | 0.640 | 0.640 | 0.677 | 0.640 | 0.677 | ns |
| DIFF_HSTL_I_S | 0.404 | 0.404 | 0.417 | 0.404 | 0.417 | 0.767 | 0.767 | 0.818 | 0.767 | 0.818 | 0.811 | 0.811 | 0.866 | 0.811 | 0.866 | ns |
| DIFF_HSUL_12_DCI_F | 0.381 | 0.381 | 0.400 | 0.381 | 0.400 | 0.425 | 0.425 | 0.443 | 0.425 | 0.443 | 0.558 | 0.558 | 0.586 | 0.558 | 0.586 | ns |
| DIFF_HSUL_12_DCI_M | 0.381 | 0.381 | 0.400 | 0.381 | 0.400 | 0.557 | 0.557 | 0.587 | 0.557 | 0.587 | 0.653 | 0.653 | 0.694 | 0.653 | 0.694 | ns |
| DIFF_HSUL_12_DCI_S | 0.381 | 0.381 | 0.400 | 0.381 | 0.400 | 0.737 | 0.737 | 0.787 | 0.737 | 0.787 | 0.822 | 0.822 | 0.885 | 0.822 | 0.885 | ns |
| DIFF_HSUL_12_F | 0.394 | 0.394 | 0.402 | 0.394 | 0.402 | 0.412 | 0.412 | 0.430 | 0.412 | 0.430 | 0.538 | 0.538 | 0.566 | 0.538 | 0.566 | ns |
| DIFF_HSUL_12_M | 0.394 | 0.394 | 0.402 | 0.394 | 0.402 | 0.552 | 0.552 | 0.583 | 0.552 | 0.583 | 0.641 | 0.641 | 0.679 | 0.641 | 0.679 | ns |
| DIFF_HSUL_12_S | 0.394 | 0.394 | 0.402 | 0.394 | 0.402 | 0.752 | 0.752 | 0.800 | 0.752 | 0.800 | 0.813 | 0.813 | 0.868 | 0.813 | 0.868 | ns |
| DIFF_POD10_DCI_F | 0.411 | 0.411 | 0.430 | 0.411 | 0.430 | 0.425 | 0.425 | 0.444 | 0.425 | 0.444 | 0.555 | 0.555 | 0.584 | 0.555 | 0.584 | ns |
| DIFF_POD10_DCI_M | 0.411 | 0.411 | 0.430 | 0.411 | 0.430 | 0.542 | 0.542 | 0.571 | 0.542 | 0.571 | 0.640 | 0.640 | 0.681 | 0.640 | 0.681 | ns |
| DIFF_POD10_DCI_S | 0.411 | 0.411 | 0.430 | 0.411 | 0.430 | 0.754 | 0.754 | 0.815 | 0.754 | 0.815 | 0.850 | 0.850 | 0.917 | 0.850 | 0.917 | ns |
| DIFF_POD10_F | 0.411 | 0.411 | 0.433 | 0.411 | 0.433 | 0.438 | 0.438 | 0.459 | 0.438 | 0.459 | 0.569 | 0.569 | 0.601 | 0.569 | 0.601 | ns |
| DIFF_POD10_M | 0.411 | 0.411 | 0.433 | 0.411 | 0.433 | 0.538 | 0.538 | 0.568 | 0.538 | 0.568 | 0.630 | 0.630 | 0.667 | 0.630 | 0.667 | ns |
| DIFF_POD10_S | 0.411 | 0.411 | 0.433 | 0.411 | 0.433 | 0.766 | 0.766 | 0.821 | 0.766 | 0.821 | 0.836 | 0.836 | 0.894 | 0.836 | 0.894 | ns |
| DIFF_POD12_DCI_F | 0.407 | 0.407 | 0.432 | 0.407 | 0.432 | 0.425 | 0.425 | 0.443 | 0.425 | 0.443 | 0.558 | 0.558 | 0.586 | 0.558 | 0.586 | ns |
| DIFF_POD12_DCI_M | 0.407 | 0.407 | 0.432 | 0.407 | 0.432 | 0.543 | 0.543 | 0.572 | 0.543 | 0.572 | 0.638 | 0.638 | 0.678 | 0.638 | 0.678 | ns |
| DIFF_POD12_DCI_S | 0.407 | 0.407 | 0.432 | 0.407 | 0.432 | 0.772 | 0.772 | 0.822 | 0.772 | 0.822 | 0.862 | 0.862 | 0.929 | 0.862 | 0.929 | ns |
| DIFF_POD12_F | 0.409 | 0.409 | 0.430 | 0.409 | 0.430 | 0.455 | 0.455 | 0.476 | 0.455 | 0.476 | 0.595 | 0.595 | 0.626 | 0.595 | 0.626 | ns |
| DIFF_POD12_M | 0.409 | 0.409 | 0.430 | 0.409 | 0.430 | 0.551 | 0.551 | 0.582 | 0.551 | 0.582 | 0.641 | 0.641 | 0.679 | 0.641 | 0.679 | ns |
| DIFF_POD12_S | 0.409 | 0.409 | 0.430 | 0.409 | 0.430 | 0.767 | 0.767 | 0.817 | 0.767 | 0.817 | 0.832 | 0.832 | 0.889 | 0.832 | 0.889 | ns |
| DIFF_SSTL12_DCI_F | 0.381 | 0.381 | 0.400 | 0.381 | 0.400 | 0.425 | 0.425 | 0.443 | 0.425 | 0.443 | 0.558 | 0.558 | 0.586 | 0.558 | 0.586 | ns |
| DIFF_SSTL12_DCI_M | 0.381 | 0.381 | 0.400 | 0.381 | 0.400 | 0.557 | 0.557 | 0.587 | 0.557 | 0.587 | 0.654 | 0.654 | 0.694 | 0.654 | 0.694 | ns |
| DIFF_SSTL12_DCI_S | 0.381 | 0.381 | 0.400 | 0.381 | 0.400 | 0.754 | 0.754 | 0.803 | 0.754 | 0.803 | 0.842 | 0.842 | 0.908 | 0.842 | 0.908 | ns |

*Table 29:* **IOB High Performance (HP) Switching Characteristics *(Cont'd)***

| I/O Standards | $T_{INBUF\_DELAY\_PAD\_I}$ | | | | | $T_{OUTBUF\_DELAY\_O\_PAD}$ | | | | | $T_{OUTBUF\_DELAY\_TD\_PAD}$ | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0.90V | 0.85V | | 0.72V | | 0.90V | 0.85V | | 0.72V | | 0.90V | 0.85V | | 0.72V | | |
| | -3 | -2 | -1 | -2 | -1 | -3 | -2 | -1 | -2 | -1 | -3 | -2 | -1 | -2 | -1 | |
| DIFF_SSTL12_F | 0.394 | 0.394 | 0.402 | 0.394 | 0.402 | 0.412 | 0.412 | 0.430 | 0.412 | 0.430 | 0.538 | 0.538 | 0.566 | 0.538 | 0.566 | ns |
| DIFF_SSTL12_M | 0.394 | 0.394 | 0.402 | 0.394 | 0.402 | 0.553 | 0.553 | 0.584 | 0.553 | 0.584 | 0.641 | 0.641 | 0.676 | 0.641 | 0.676 | ns |
| DIFF_SSTL12_S | 0.394 | 0.394 | 0.402 | 0.394 | 0.402 | 0.758 | 0.758 | 0.808 | 0.758 | 0.808 | 0.823 | 0.823 | 0.879 | 0.823 | 0.879 | ns |
| DIFF_SSTL135_DCI_F | 0.371 | 0.371 | 0.402 | 0.371 | 0.402 | 0.411 | 0.411 | 0.428 | 0.411 | 0.428 | 0.537 | 0.537 | 0.565 | 0.537 | 0.565 | ns |
| DIFF_SSTL135_DCI_M | 0.371 | 0.371 | 0.402 | 0.371 | 0.402 | 0.551 | 0.551 | 0.582 | 0.551 | 0.582 | 0.645 | 0.645 | 0.685 | 0.645 | 0.685 | ns |
| DIFF_SSTL135_DCI_S | 0.371 | 0.371 | 0.402 | 0.371 | 0.402 | 0.746 | 0.746 | 0.799 | 0.746 | 0.799 | 0.829 | 0.829 | 0.893 | 0.829 | 0.893 | ns |
| DIFF_SSTL135_F | 0.375 | 0.375 | 0.402 | 0.375 | 0.402 | 0.408 | 0.408 | 0.428 | 0.408 | 0.428 | 0.528 | 0.528 | 0.561 | 0.528 | 0.561 | ns |
| DIFF_SSTL135_M | 0.375 | 0.375 | 0.402 | 0.375 | 0.402 | 0.555 | 0.555 | 0.585 | 0.555 | 0.585 | 0.641 | 0.641 | 0.679 | 0.641 | 0.679 | ns |
| DIFF_SSTL135_S | 0.375 | 0.375 | 0.402 | 0.375 | 0.402 | 0.772 | 0.772 | 0.823 | 0.772 | 0.823 | 0.827 | 0.827 | 0.878 | 0.827 | 0.878 | ns |
| DIFF_SSTL15_DCI_F | 0.397 | 0.397 | 0.417 | 0.397 | 0.417 | 0.412 | 0.412 | 0.429 | 0.412 | 0.429 | 0.531 | 0.531 | 0.563 | 0.531 | 0.563 | ns |
| DIFF_SSTL15_DCI_M | 0.397 | 0.397 | 0.417 | 0.397 | 0.417 | 0.553 | 0.553 | 0.583 | 0.553 | 0.583 | 0.645 | 0.645 | 0.685 | 0.645 | 0.685 | ns |
| DIFF_SSTL15_DCI_S | 0.397 | 0.397 | 0.417 | 0.397 | 0.417 | 0.768 | 0.768 | 0.822 | 0.768 | 0.822 | 0.847 | 0.847 | 0.912 | 0.847 | 0.912 | ns |
| DIFF_SSTL15_F | 0.404 | 0.404 | 0.417 | 0.404 | 0.417 | 0.424 | 0.424 | 0.445 | 0.424 | 0.445 | 0.551 | 0.551 | 0.577 | 0.551 | 0.577 | ns |
| DIFF_SSTL15_M | 0.404 | 0.404 | 0.417 | 0.404 | 0.417 | 0.554 | 0.554 | 0.585 | 0.554 | 0.585 | 0.639 | 0.639 | 0.677 | 0.639 | 0.677 | ns |
| DIFF_SSTL15_S | 0.404 | 0.404 | 0.417 | 0.404 | 0.417 | 0.767 | 0.767 | 0.817 | 0.767 | 0.817 | 0.813 | 0.813 | 0.867 | 0.813 | 0.867 | ns |
| DIFF_SSTL18_I_DCI_F | 0.320 | 0.320 | 0.336 | 0.320 | 0.336 | 0.445 | 0.445 | 0.461 | 0.445 | 0.461 | 0.566 | 0.566 | 0.595 | 0.566 | 0.595 | ns |
| DIFF_SSTL18_I_DCI_M | 0.320 | 0.320 | 0.336 | 0.320 | 0.336 | 0.554 | 0.554 | 0.585 | 0.554 | 0.585 | 0.644 | 0.644 | 0.683 | 0.644 | 0.683 | ns |
| DIFF_SSTL18_I_DCI_S | 0.320 | 0.320 | 0.336 | 0.320 | 0.336 | 0.762 | 0.762 | 0.818 | 0.762 | 0.818 | 0.837 | 0.837 | 0.899 | 0.837 | 0.899 | ns |
| DIFF_SSTL18_I_F | 0.316 | 0.316 | 0.336 | 0.316 | 0.336 | 0.454 | 0.454 | 0.476 | 0.454 | 0.476 | 0.578 | 0.578 | 0.608 | 0.578 | 0.608 | ns |
| DIFF_SSTL18_I_M | 0.316 | 0.316 | 0.336 | 0.316 | 0.336 | 0.571 | 0.571 | 0.603 | 0.571 | 0.603 | 0.652 | 0.652 | 0.692 | 0.652 | 0.692 | ns |
| DIFF_SSTL18_I_S | 0.316 | 0.316 | 0.336 | 0.316 | 0.336 | 0.782 | 0.782 | 0.835 | 0.782 | 0.835 | 0.816 | 0.816 | 0.870 | 0.816 | 0.870 | ns |
| HSLVDCI_15_F | 0.393 | 0.393 | 0.415 | 0.393 | 0.415 | 0.425 | 0.425 | 0.443 | 0.425 | 0.443 | 0.548 | 0.548 | 0.579 | 0.548 | 0.579 | ns |
| HSLVDCI_15_M | 0.393 | 0.393 | 0.415 | 0.393 | 0.415 | 0.552 | 0.552 | 0.581 | 0.552 | 0.581 | 0.644 | 0.644 | 0.684 | 0.644 | 0.684 | ns |
| HSLVDCI_15_S | 0.393 | 0.393 | 0.415 | 0.393 | 0.415 | 0.748 | 0.748 | 0.802 | 0.748 | 0.802 | 0.827 | 0.827 | 0.890 | 0.827 | 0.890 | ns |
| HSLVDCI_18_F | 0.424 | 0.424 | 0.447 | 0.424 | 0.447 | 0.445 | 0.445 | 0.461 | 0.445 | 0.461 | 0.566 | 0.566 | 0.595 | 0.566 | 0.595 | ns |
| HSLVDCI_18_M | 0.424 | 0.424 | 0.447 | 0.424 | 0.447 | 0.567 | 0.567 | 0.598 | 0.567 | 0.598 | 0.658 | 0.658 | 0.699 | 0.658 | 0.699 | ns |
| HSLVDCI_18_S | 0.424 | 0.424 | 0.447 | 0.424 | 0.447 | 0.761 | 0.761 | 0.817 | 0.761 | 0.817 | 0.836 | 0.836 | 0.900 | 0.836 | 0.900 | ns |
| HSTL_I_12_F | 0.378 | 0.378 | 0.399 | 0.378 | 0.399 | 0.423 | 0.423 | 0.443 | 0.423 | 0.443 | 0.553 | 0.553 | 0.582 | 0.553 | 0.582 | ns |
| HSTL_I_12_M | 0.378 | 0.378 | 0.399 | 0.378 | 0.399 | 0.551 | 0.551 | 0.582 | 0.551 | 0.582 | 0.642 | 0.642 | 0.679 | 0.642 | 0.679 | ns |
| HSTL_I_12_S | 0.378 | 0.378 | 0.399 | 0.378 | 0.399 | 0.750 | 0.750 | 0.799 | 0.750 | 0.799 | 0.813 | 0.813 | 0.868 | 0.813 | 0.868 | ns |
| HSTL_I_18_F | 0.322 | 0.322 | 0.339 | 0.322 | 0.339 | 0.456 | 0.456 | 0.474 | 0.456 | 0.474 | 0.576 | 0.576 | 0.606 | 0.576 | 0.606 | ns |
| HSTL_I_18_M | 0.322 | 0.322 | 0.339 | 0.322 | 0.339 | 0.569 | 0.569 | 0.602 | 0.569 | 0.602 | 0.653 | 0.653 | 0.692 | 0.653 | 0.692 | ns |
| HSTL_I_18_S | 0.322 | 0.322 | 0.339 | 0.322 | 0.339 | 0.781 | 0.781 | 0.833 | 0.781 | 0.833 | 0.816 | 0.816 | 0.871 | 0.816 | 0.871 | ns |
| HSTL_I_DCI_12_F | 0.378 | 0.378 | 0.399 | 0.378 | 0.399 | 0.406 | 0.406 | 0.429 | 0.406 | 0.429 | 0.534 | 0.534 | 0.564 | 0.534 | 0.564 | ns |
| HSTL_I_DCI_12_M | 0.378 | 0.378 | 0.399 | 0.378 | 0.399 | 0.556 | 0.556 | 0.586 | 0.556 | 0.586 | 0.654 | 0.654 | 0.694 | 0.654 | 0.694 | ns |
| HSTL_I_DCI_12_S | 0.378 | 0.378 | 0.399 | 0.378 | 0.399 | 0.754 | 0.754 | 0.803 | 0.754 | 0.803 | 0.842 | 0.842 | 0.907 | 0.842 | 0.907 | ns |
| HSTL_I_DCI_18_F | 0.321 | 0.321 | 0.339 | 0.321 | 0.339 | 0.445 | 0.445 | 0.461 | 0.445 | 0.461 | 0.566 | 0.566 | 0.595 | 0.566 | 0.595 | ns |
| HSTL_I_DCI_18_M | 0.321 | 0.321 | 0.339 | 0.321 | 0.339 | 0.554 | 0.554 | 0.585 | 0.554 | 0.585 | 0.643 | 0.643 | 0.684 | 0.643 | 0.684 | ns |
| HSTL_I_DCI_18_S | 0.321 | 0.321 | 0.339 | 0.321 | 0.339 | 0.761 | 0.761 | 0.817 | 0.761 | 0.817 | 0.836 | 0.836 | 0.900 | 0.836 | 0.900 | ns |
| HSTL_I_DCI_F | 0.393 | 0.393 | 0.415 | 0.393 | 0.415 | 0.431 | 0.431 | 0.445 | 0.431 | 0.445 | 0.555 | 0.555 | 0.575 | 0.555 | 0.575 | ns |
| HSTL_I_DCI_M | 0.393 | 0.393 | 0.415 | 0.393 | 0.415 | 0.552 | 0.552 | 0.581 | 0.552 | 0.581 | 0.644 | 0.644 | 0.684 | 0.644 | 0.684 | ns |

# Input Delay Measurement Methodology

Table 31 shows the test setup parameters used for measuring input delay.

*Table 31:* **Input Delay Measurement Methodology**

| Description | I/O Standard Attribute | $V_L$ (1)(2) | $V_H$ (1)(2) | $V_{MEAS}$ (1)(4)(6) | $V_{REF}$ (1)(3)(5) |
|---|---|---|---|---|---|
| LVCMOS, 1.2V | LVCMOS12 | 0.1 | 1.1 | 0.6 | – |
| LVCMOS, LVDCI, HSLVDCI, 1.5V | LVCMOS15, LVDCI_15, HSLVDCI_15 | 0.1 | 1.4 | 0.75 | – |
| LVCMOS, LVDCI, HSLVDCI, 1.8V | LVCMOS18, LVDCI_18, HSLVDCI_18 | 0.1 | 1.7 | 0.9 | – |
| LVCMOS, 2.5V | LVCMOS25 | 0.1 | 2.4 | 1.25 | – |
| LVCMOS, 3.3V | LVCMOS33 | 0.1 | 3.2 | 1.65 | – |
| LVTTL, 3.3V | LVTTL | 0.1 | 3.2 | 1.65 | – |
| HSTL (high-speed transceiver logic), class I, 1.2V | HSTL_I_12 | $V_{REF}$ – 0.25 | $V_{REF}$ + 0.25 | $V_{REF}$ | 0.6 |
| HSTL, class I, 1.5V | HSTL_I | $V_{REF}$ – 0.325 | $V_{REF}$ + 0.325 | $V_{REF}$ | 0.75 |
| HSTL, class I, 1.8V | HSTL_I_18 | $V_{REF}$ – 0.4 | $V_{REF}$ + 0.4 | $V_{REF}$ | 0.9 |
| HSUL (high-speed unterminated logic), 1.2V | HSUL_12 | $V_{REF}$ – 0.25 | $V_{REF}$ + 0.25 | $V_{REF}$ | 0.6 |
| SSTL12 (stub series terminated logic), 1.2V | SSTL12 | $V_{REF}$ – 0.25 | $V_{REF}$ + 0.25 | $V_{REF}$ | 0.6 |
| SSTL135 and SSTL135 class II, 1.35V | SSTL135, SSTL135_II | $V_{REF}$ – 0.2875 | $V_{REF}$ + 0.2875 | $V_{REF}$ | 0.675 |
| SSTL15 and SSTL15 class II, 1.5V | SSTL15, SSTL15_II | $V_{REF}$ – 0.325 | $V_{REF}$ + 0.325 | $V_{REF}$ | 0.75 |
| SSTL18, class I and II, 1.8V | SSTL18_I, SSTL18_II | $V_{REF}$ – 0.4 | $V_{REF}$ + 0.4 | $V_{REF}$ | 0.9 |
| POD10, 1.0V | POD10 | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | $V_{REF}$ | 0.7 |
| POD12, 1.2V | POD12 | $V_{REF}$ – 0.24 | $V_{REF}$ + 0.24 | $V_{REF}$ | 0.84 |
| DIFF_HSTL, class I, 1.2V | DIFF_HSTL_I_12 | 0.6 – 0.25 | 0.6 + 0.25 | 0 (6) | – |
| DIFF_HSTL, class I, 1.5V | DIFF_HSTL_I | 0.75 – 0.325 | 0.75 + 0.325 | 0 (6) | – |
| DIFF_HSTL, class I, 1.8V | DIFF_HSTL_I_18 | 0.9 – 0.4 | 0.9 + 0.4 | 0 (6) | – |
| DIFF_HSUL, 1.2V | DIFF_HSUL_12 | 0.6 – 0.25 | 0.6 + 0.25 | 0 (6) | – |
| DIFF_SSTL, 1.2V | DIFF_SSTL12 | 0.6 – 0.25 | 0.6 + 0.25 | 0 (6) | – |
| DIFF_SSTL135 and DIFF_SSTL135 class II, 1.35V | DIFF_SSTL135, DIFF_SSTL135_II | 0.675 – 0.2875 | 0.675 + 0.2875 | 0 (6) | – |
| DIFF_SSTL15 and DIFF_SSTL15 class II, 1.5V | DIFF_SSTL15, DIFF_SSTL15_II | 0.75 – 0.325 | 0.75 + 0.325 | 0 (6) | – |
| DIFF_SSTL18_I, DIFF_SSTL18_II, 1.8V | DIFF_SSTL18_I, DIFF_SSTL18_II | 0.9 – 0.4 | 0.9 + 0.4 | 0 (6) | – |
| DIFF_POD10, 1.0V | DIFF_POD10 | 0.5 – 0.2 | 0.5 + 0.2 | 0 (6) | – |
| DIFF_POD12, 1.2V | DIFF_POD12 | 0.6 – 0.25 | 0.6 + 0.25 | 0 (6) | – |
| LVDS (low-voltage differential signaling), 1.8V | LVDS | 0.9 – 0.125 | 0.9 + 0.125 | 0 (6) | – |
| LVDS_25, 2.5V | LVDS_25 | 1.25 – 0.125 | 1.25 + 0.125 | 0 (6) | – |
| SUB_LVDS, 1.8V | SUB_LVDS | 0.9 – 0.125 | 0.9 + 0.125 | 0 (6) | – |

# DSP48 Slice Switching Characteristics

*Table 36:* **DSP48 Slice Switching Characteristics**

| Symbol | Description | Speed Grade and $V_{CCINT}$ Operating Voltages | | | | | Units |
|---|---|---|---|---|---|---|---|
| | | 0.90V | 0.85V | | 0.72V | | |
| | | -3 | -2 | -1 | -2 | -1 | |
| **Maximum Frequency** | | | | | | | |
| $F_{MAX}$ | With all registers used. | 891 | 775 | 645 | 644 | 600 | MHz |
| $F_{MAX\_PATDET}$ | With pattern detector. | 794 | 687 | 571 | 562 | 524 | MHz |
| $F_{MAX\_MULT\_NOMREG}$ | Two register multiply without MREG. | 635 | 544 | 456 | 440 | 413 | MHz |
| $F_{MAX\_MULT\_NOMREG\_PATDET}$ | Two register multiply without MREG with pattern detect. | 577 | 492 | 410 | 395 | 371 | MHz |
| $F_{MAX\_PREADD\_NOADREG}$ | Without ADREG. | 655 | 565 | 468 | 453 | 423 | MHz |
| $F_{MAX\_NOPIPELINEREG}$ | Without pipeline registers (MREG, ADREG). | 483 | 410 | 338 | 323 | 304 | MHz |
| $F_{MAX\_NOPIPELINEREG\_PATDET}$ | Without pipeline registers (MREG, ADREG) with pattern detect. | 448 | 379 | 314 | 299 | 280 | MHz |

# Clock Buffers and Networks

*Table 37:* **Clock Buffers Switching Characteristics**

| Symbol | Description | Speed Grade and $V_{CCINT}$ Operating Voltages | | | | | Units |
|---|---|---|---|---|---|---|---|
| | | 0.90V | 0.85V | | 0.72V | | |
| | | -3 | -2 | -1 | -2 | -1 | |
| **Global Clock Switching Characteristics (Including BUFGCTRL)** | | | | | | | |
| $F_{MAX}$ | Maximum frequency of a global clock tree (BUFG). | 891 | 775 | 667 | 725 | 667 | MHz |
| **Global Clock Buffer with Input Divide Capability (BUFGCE_DIV)** | | | | | | | |
| $F_{MAX}$ | Maximum frequency of a global clock buffer with input divide capability (BUFGCE_DIV). | 891 | 775 | 667 | 725 | 667 | MHz |
| **Global Clock Buffer with Clock Enable (BUFGCE)** | | | | | | | |
| $F_{MAX}$ | Maximum frequency of a global clock buffer with clock enable (BUFGCE). | 891 | 775 | 667 | 725 | 667 | MHz |
| **Leaf Clock Buffer with Clock Enable (BUFCE_LEAF)** | | | | | | | |
| $F_{MAX}$ | Maximum frequency of a leaf clock buffer with clock enable (BUFCE_LEAF). | 891 | 775 | 667 | 725 | 667 | MHz |
| **GTH or GTY Clock Buffer with Clock Enable and Clock Input Divide Capability (BUFG_GT)** | | | | | | | |
| $F_{MAX}$ | Maximum frequency of a serial transceiver clock buffer with clock enable and clock input divide capability. | 512 | 512 | 512 | 512 | 512 | MHz |

# MMCM Switching Characteristics

*Table 38:* **MMCM Specification**

| Symbol | Description | Speed Grade and $V_{CCINT}$ Operating Voltages | | | | | Units |
|---|---|---|---|---|---|---|---|
| | | 0.90V | 0.85V | | 0.72V | | |
| | | -3 | -2 | -1 | -2 | -1 | |
| MMCM_$F_{INMAX}$ | Maximum input clock frequency. | 1066 | 933 | 800 | 933 | 800 | MHz |
| MMCM_$F_{INMIN}$ | Minimum input clock frequency. | 10 | 10 | 10 | 10 | 10 | MHz |
| MMCM_$F_{INJITTER}$ | Maximum input clock period jitter. | < 20% of clock input period or 1 ns Max | | | | | |
| MMCM_$F_{INDUTY}$ | Input duty cycle range: 10–49 MHz. | 25–75 | | | | | % |
| | Input duty cycle range: 50–199 MHz. | 30–70 | | | | | % |
| | Input duty cycle range: 200–399 MHz. | 35–65 | | | | | % |
| | Input duty cycle range: 400–499 MHz. | 40–60 | | | | | % |
| | Input duty cycle range: >500 MHz. | 45–55 | | | | | % |
| MMCM_$F_{MIN_PSCLK}$ | Minimum dynamic phase shift clock frequency. | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | MHz |
| MMCM_$F_{MAX_PSCLK}$ | Maximum dynamic phase shift clock frequency. | 550 | 500 | 450 | 500 | 450 | MHz |
| MMCM_$F_{VCOMIN}$ | Minimum MMCM VCO frequency. | 800 | 800 | 800 | 800 | 800 | MHz |
| MMCM_$F_{VCOMAX}$ | Maximum MMCM VCO frequency. | 1600 | 1600 | 1600 | 1600 | 1600 | MHz |
| MMCM_$F_{BANDWIDTH}$ | Low MMCM bandwidth at typical.(1) | 1.00 | 1.00 | 1.00 | 1.00 | 1.00 | MHz |
| | High MMCM bandwidth at typical.(1) | 4.00 | 4.00 | 4.00 | 4.00 | 4.00 | MHz |
| MMCM_$T_{STATPHAOFFSET}$ | Static phase offset of the MMCM outputs.(2) | 0.12 | 0.12 | 0.12 | 0.12 | 0.12 | ns |
| MMCM_$T_{OUTJITTER}$ | MMCM output jitter. | Note 3 | | | | | |
| MMCM_$T_{OUTDUTY}$ | MMCM output clock duty cycle precision.(4) | 0.165 | 0.20 | 0.20 | 0.20 | 0.20 | ns |
| MMCM_$T_{LOCKMAX}$ | MMCM maximum lock time for MMCM_$F_{PFDMIN}$. | 100 | 100 | 100 | 100 | 100 | µs |
| MMCM_$F_{OUTMAX}$ | MMCM maximum output frequency. | 891 | 775 | 667 | 725 | 667 | MHz |
| MMCM_$F_{OUTMIN}$ | MMCM minimum output frequency.(4)(5) | 6.25 | 6.25 | 6.25 | 6.25 | 6.25 | MHz |
| MMCM_$T_{EXTFDVAR}$ | External clock feedback variation. | < 20% of clock input period or 1 ns Max | | | | | |
| MMCM_$RST_{MINPULSE}$ | Minimum reset pulse width. | 5.00 | 5.00 | 5.00 | 5.00 | 5.00 | ns |
| MMCM_$F_{PFDMAX}$ | Maximum frequency at the phase frequency detector. | 550 | 500 | 450 | 500 | 450 | MHz |
| MMCM_$F_{PFDMIN}$ | Minimum frequency at the phase frequency detector. | 10 | 10 | 10 | 10 | 10 | MHz |
| MMCM_$T_{FBDELAY}$ | Maximum delay in the feedback path. | 5 ns Max or one clock cycle | | | | | |
| MMCM_$F_{DPRCLK_MAX}$ | Maximum DRP clock frequency. | 250 | 250 | 250 | 250 | 250 | MHz |

**Notes:**

1. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any MMCM outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard.
4. Includes global clock buffer.
5. Calculated as $F_{VCO}$/128 assuming output duty cycle is 50%.

*Table 55:* **GTH Transceiver User Clock Switching Characteristics[1] *(Cont'd)***

| Symbol | Description | Data Width Conditions (Bit) | | Speed Grade, Temperature Ranges, and $V_{CCINT}$ Operating Voltages | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | | 0.90V | 0.85V | | 0.72V | | |
| | | Internal Logic | Interconnect Logic | -3[2] | -2[2][3] | -1[4][5] | -2[3] | -1[3][5] | |
| $F_{TXOUTPROGDIV}$ | TXOUTCLK maximum frequency sourced from TXPROGDIVCLK. | | | 511.719 | 511.719 | 511.719 | 511.719 | 511.719 | MHz |
| $F_{RXOUTPROGDIV}$ | RXOUTCLK maximum frequency sourced from RXPROGDIVCLK. | | | 511.719 | 511.719 | 511.719 | 511.719 | 511.719 | MHz |
| $F_{TXIN}$ | TXUSRCLK[6] maximum frequency | 16 | 16, 32 | 511.719 | 511.719 | 390.625 | 390.625 | 322.266 | MHz |
| | | 32 | 32, 64 | 511.719 | 511.719 | 390.625 | 390.625 | 322.266 | MHz |
| | | 20 | 20, 40 | 409.375 | 409.375 | 312.500 | 312.500 | 257.813 | MHz |
| | | 40 | 40, 80 | 409.375 | 409.375 | 312.500 | 312.500 | 257.813 | MHz |
| $F_{RXIN}$ | RXUSRCLK[6] maximum frequency | 16 | 16, 32 | 511.719 | 511.719 | 390.625 | 390.625 | 322.266 | MHz |
| | | 32 | 32, 64 | 511.719 | 511.719 | 390.625 | 390.625 | 322.266 | MHz |
| | | 20 | 20, 40 | 409.375 | 409.375 | 312.500 | 312.500 | 257.813 | MHz |
| | | 40 | 40, 80 | 409.375 | 409.375 | 312.500 | 312.500 | 257.813 | MHz |
| $F_{TXIN2}$ | TXUSRCLK2[6] maximum frequency | 16 | 16 | 511.719 | 511.719 | 390.625 | 390.625 | 322.266 | MHz |
| | | 16 | 32 | 255.859 | 255.859 | 195.313 | 195.313 | 161.133 | MHz |
| | | 32 | 32 | 511.719 | 511.719 | 390.625 | 390.625 | 322.266 | MHz |
| | | 32 | 64 | 255.859 | 255.859 | 195.313 | 195.313 | 161.133 | MHz |
| | | 20 | 20 | 409.375 | 409.375 | 312.500 | 312.500 | 257.813 | MHz |
| | | 20 | 40 | 204.688 | 204.688 | 156.250 | 156.250 | 128.906 | MHz |
| | | 40 | 40 | 409.375 | 409.375 | 312.500 | 312.500 | 257.813 | MHz |
| | | 40 | 80 | 204.688 | 204.688 | 156.250 | 156.250 | 128.906 | MHz |
| $F_{RXIN2}$ | RXUSRCLK2[6] maximum frequency | 16 | 16 | 511.719 | 511.719 | 390.625 | 390.625 | 322.266 | MHz |
| | | 16 | 32 | 255.859 | 255.859 | 195.313 | 195.313 | 161.133 | MHz |
| | | 32 | 32 | 511.719 | 511.719 | 390.625 | 390.625 | 322.266 | MHz |
| | | 32 | 64 | 255.859 | 255.859 | 195.313 | 195.313 | 161.133 | MHz |
| | | 20 | 20 | 409.375 | 409.375 | 312.500 | 312.500 | 257.813 | MHz |
| | | 20 | 40 | 204.688 | 204.688 | 156.250 | 156.250 | 128.906 | MHz |
| | | 40 | 40 | 409.375 | 409.375 | 312.500 | 312.500 | 257.813 | MHz |
| | | 40 | 80 | 204.688 | 204.688 | 156.250 | 156.250 | 128.906 | MHz |

**Notes:**

1. Clocking must be implemented as described in the *UltraScale Architecture GTH Transceiver User Guide* (UG576).
2. For speed grades -3E, -2E, and -2I, a 16-bit and 20-bit internal data path can only be used for line rates less than 8.1875 Gb/s.
3. For speed grade -2LE, a 16-bit and 20-bit internal data path can only be used for line rates less than 8.1875 Gb/s when $V_{CCINT}$ = 0.85V or 6.25 Gb/s when $V_{CCINT}$ = 0.72V.
4. For speed grades -1E and -1I, a 16-bit and 20-bit internal data path can only be used for line rates less than 6.25 Gb/s.
5. For speed grade -1LI, a 16-bit and 20-bit internal data path can only be used for line rates less than 6.25 Gb/s when $V_{CCINT}$ = 0.85V or 5.15625 Gb/s when $V_{CCINT}$ = 0.72V.
6. When the gearbox is used, these maximums refer to the XCLK. For more information, see the *Valid Data Width Combinations for TX Asynchronous Gearbox* table in the *UltraScale Architecture GTH Transceiver User Guide* (UG576).

*Table 56:* **GTH Transceiver Transmitter Switching Characteristics**

| Symbol | Description | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $F_{GTHTX}$ | Serial data rate range | | 0.500 | – | $F_{GTHMAX}$ | Gb/s |
| $T_{RTX}$ | TX rise time | 20%–80% | – | 21 | – | ps |
| $T_{FTX}$ | TX fall time | 80%–20% | – | 21 | – | ps |
| $T_{LLSKEW}$ | TX lane-to-lane skew(1) | | – | – | 500.00 | ps |
| $T_{J16.375}$ | Total jitter(2)(4) | 16.375 Gb/s | – | – | 0.28 | UI |
| $D_{J16.375}$ | Deterministic jitter(2)(4) | | – | – | 0.17 | UI |
| $T_{J15.0}$ | Total jitter(2)(4) | 15.0 Gb/s | – | – | 0.28 | UI |
| $D_{J15.0}$ | Deterministic jitter(2)(4) | | – | – | 0.17 | UI |
| $T_{J14.1}$ | Total jitter(2)(4) | 14.1 Gb/s | – | – | 0.28 | UI |
| $D_{J14.1}$ | Deterministic jitter(2)(4) | | – | – | 0.17 | UI |
| $T_{J14.1}$ | Total jitter(2)(4) | 14.025 Gb/s | – | – | 0.28 | UI |
| $D_{J14.1}$ | Deterministic jitter(2)(4) | | – | – | 0.17 | UI |
| $T_{J13.1}$ | Total jitter(2)(4) | 13.1 Gb/s | – | – | 0.28 | UI |
| $D_{J13.1}$ | Deterministic jitter(2)(4) | | – | – | 0.17 | UI |
| $T_{J12.5\_QPLL}$ | Total jitter(2)(4) | 12.5 Gb/s | – | – | 0.28 | UI |
| $D_{J12.5\_QPLL}$ | Deterministic jitter(2)(4) | | – | – | 0.17 | UI |
| $T_{J12.5\_CPLL}$ | Total jitter(3)(4) | 12.5 Gb/s | – | – | 0.33 | UI |
| $D_{J12.5\_CPLL}$ | Deterministic jitter(3)(4) | | – | – | 0.17 | UI |
| $T_{J11.3\_QPLL}$ | Total jitter(2)(4) | 11.3 Gb/s | – | – | 0.28 | UI |
| $D_{J11.3\_QPLL}$ | Deterministic jitter(2)(4) | | – | – | 0.17 | UI |
| $T_{J10.3125\_QPLL}$ | Total jitter(2)(4) | 10.3125 Gb/s | – | – | 0.28 | UI |
| $D_{J10.3125\_QPLL}$ | Deterministic jitter(2)(4) | | – | – | 0.17 | UI |
| $T_{J10.3125\_CPLL}$ | Total jitter(3)(4) | 10.3125 Gb/s | – | – | 0.33 | UI |
| $D_{J10.3125\_CPLL}$ | Deterministic jitter(3)(4) | | – | – | 0.17 | UI |
| $T_{J9.953\_QPLL}$ | Total jitter(2)(4) | 9.953 Gb/s | – | – | 0.28 | UI |
| $D_{J9.953\_QPLL}$ | Deterministic jitter(2)(4) | | – | – | 0.17 | UI |
| $T_{J9.953\_CPLL}$ | Total jitter(3)(4) | 9.953 Gb/s | – | – | 0.33 | UI |
| $D_{J9.953\_CPLL}$ | Deterministic jitter(3)(4) | | – | – | 0.17 | UI |
| $T_{J8.0}$ | Total jitter(3)(4) | 8.0 Gb/s | – | – | 0.32 | UI |
| $D_{J8.0}$ | Deterministic jitter(3)(4) | | – | – | 0.17 | UI |
| $T_{J6.6}$ | Total jitter(3)(4) | 6.6 Gb/s | – | – | 0.30 | UI |
| $D_{J6.6}$ | Deterministic jitter(3)(4) | | – | – | 0.15 | UI |
| $T_{J5.0}$ | Total jitter(3)(4) | 5.0 Gb/s | – | – | 0.30 | UI |
| $D_{J5.0}$ | Deterministic jitter(3)(4) | | – | – | 0.15 | UI |
| $T_{J4.25}$ | Total jitter(3)(4) | 4.25 Gb/s | – | – | 0.30 | UI |
| $D_{J4.25}$ | Deterministic jitter(3)(4) | | – | – | 0.15 | UI |
| $T_{J4.0}$ | Total jitter(3)(4) | 4.0 Gb/s | – | – | 0.32 | UI |
| $D_{J4.0}$ | Deterministic jitter(3)(4) | | – | – | 0.16 | UI |
| $T_{J3.20}$ | Total jitter(3)(4) | 3.20 Gb/s(5) | – | – | 0.20 | UI |
| $D_{J3.20}$ | Deterministic jitter(3)(4) | | – | – | 0.10 | UI |

*Table 57:* **GTH Transceiver Receiver Switching Characteristics *(Cont'd)***

| Symbol | Description | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $J_{T\_SJ2.5}$ | Sinusoidal jitter (CPLL)(3) | 2.5 Gb/s(5) | 0.30 | – | – | UI |
| $J_{T\_SJ1.25}$ | Sinusoidal jitter (CPLL)(3) | 1.25 Gb/s(6) | 0.30 | – | – | UI |
| $J_{T\_SJ500}$ | Sinusoidal jitter (CPLL)(3) | 500 Mb/s(7) | 0.30 | – | – | UI |
| **SJ Jitter Tolerance with Stressed Eye(2)** | | | | | | |
| $J_{T\_TJSE3.2}$ | Total jitter with stressed eye(8) | 3.2 Gb/s | 0.70 | – | – | UI |
| $J_{T\_TJSE6.6}$ | | 6.6 Gb/s | 0.70 | – | – | UI |
| $J_{T\_SJSE3.2}$ | Sinusoidal jitter with stressed eye(8) | 3.2 Gb/s | 0.10 | – | – | UI |
| $J_{T\_SJSE6.6}$ | | 6.6 Gb/s | 0.10 | – | – | UI |

**Notes:**
1. Using RXOUT_DIV = 1, 2, and 4.
2. All jitter values are based on a bit error ratio of $10^{-12}$.
3. The frequency of the injected sinusoidal jitter is 80 MHz.
4. CPLL frequency at 3.2 GHz and RXOUT_DIV = 2.
5. CPLL frequency at 2.5 GHz and RXOUT_DIV = 2.
6. CPLL frequency at 2.5 GHz and RXOUT_DIV = 4.
7. CPLL frequency at 2.0 GHz and RXOUT_DIV = 8.
8. Composite jitter with RX equalizer enabled. DFE disabled.

## GTH Transceiver Electrical Compliance

The *UltraScale Architecture GTH Transceiver User Guide* (UG576) contains recommended use modes that ensure compliance for the protocols listed in Table 58. The transceiver wizard provides the recommended settings for those use cases and for protocol specific characteristics.

# GTY Transceiver Specifications

The *UltraScale Architecture and Product Overview* (DS890) lists the Kintex UltraScale+ FPGAs that include the GTY transceivers.

## GTY Transceiver DC Input and Output Levels

Table 59 and Table 60 summarize the DC specifications of the GTY transceivers in Kintex UltraScale+ FPGAs. Consult the *UltraScale Architecture GTY Transceiver User Guide* (UG578) for further information.

*Table 59:* **GTY Transceiver DC Specifications**

| Symbol | DC Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $DV_{PPIN}$ | Differential peak-to-peak input voltage (external AC coupled) | >10.3125 Gb/s | 150 | – | 1250 | mV |
| | | 6.6 Gb/s to 10.3125 Gb/s | 150 | – | 1250 | mV |
| | | ≤ 6.6 Gb/s | 150 | – | 2000 | mV |
| $V_{IN}$ | Single-ended input voltage. Voltage measured at the pin referenced to GND. | DC coupled $V_{MGTAVTT}$ = 1.2V | –400 | – | $V_{MGTAVTT}$ | mV |
| $V_{CMIN}$ | Common mode input voltage | DC coupled $V_{MGTAVTT}$ = 1.2V | – | 2/3 $V_{MGTAVTT}$ | – | mV |
| $D_{VPPOUT}$ | Differential peak-to-peak output voltage(1) | Transmitter output swing is set to 11111 | 800 | – | – | mV |
| $V_{CMOUTDC}$ | Common mode output voltage: DC coupled (equation based) | When remote RX is terminated to GND | $V_{MGTAVTT}/2 - D_{VPPOUT}/4$ | | | mV |
| | | When remote RX termination is floating | $V_{MGTAVTT} - D_{VPPOUT}/2$ | | | mV |
| | | When remote RX is terminated to $V_{RX\_TERM}$(2) | $V_{MGTAVTT} - \frac{D_{VPPOUT}}{4} - \left(\frac{V_{MGTAVTT} - V_{RX\_TERM}}{2}\right)$ | | | mV |
| $V_{CMOUTAC}$ | Common mode output voltage: AC coupled | Equation based | $V_{MGTAVTT} - D_{VPPOUT}/2$ | | | mV |
| $R_{IN}$ | Differential input resistance | | – | 100 | – | Ω |
| $R_{OUT}$ | Differential output resistance | | – | 100 | – | Ω |
| $T_{OSKEW}$ | Transmitter output pair (TXP and TXN) intra-pair skew | | – | – | 10 | ps |
| $C_{EXT}$ | Recommended external AC coupling capacitor(3) | | – | 100 | – | nF |

**Notes:**

1. The output swing and pre-emphasis levels are programmable using the GTY transceiver attributes discussed in the *UltraScale Architecture GTY Transceiver User Guide* (UG578) and can result in values lower than reported in this table.
2. $V_{RX\_TERM}$ is the remote RX termination voltage.
3. Other values can be used as appropriate to conform to specific protocols and standards.

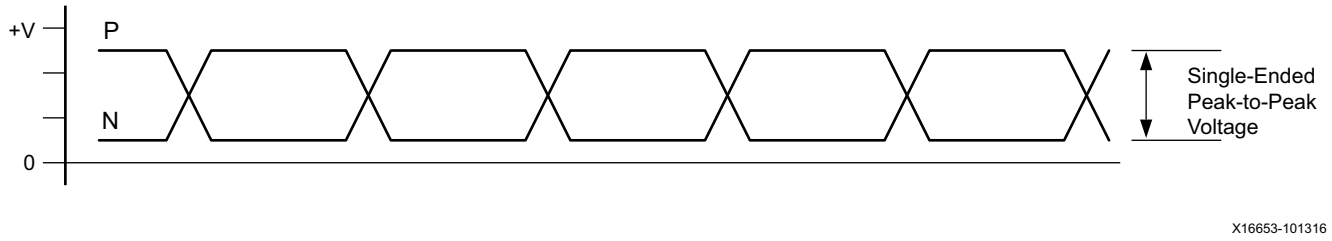


*Figure 5:* **Single-Ended Peak-to-Peak Voltage**

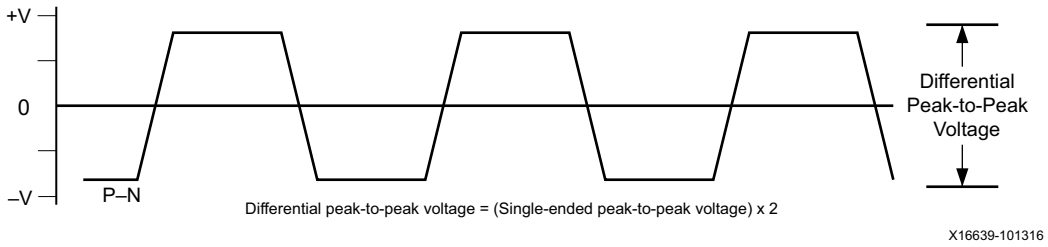


*Figure 6:* **Differential Peak-to-Peak Voltage**

Table 60 and Table 61 summarize the DC specifications of the clock input of the GTY transceivers in Kintex UltraScale+ FPGAs. Consult the *UltraScale Architecture GTY Transceiver User Guide* (UG578) for further information.

*Table 60:* **GTY Transceiver Clock DC Input Level Specification**

| Symbol | DC Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $V_{IDIFF}$ | Differential peak-to-peak input voltage | 250 | – | 2000 | mV |
| $R_{IN}$ | Differential input resistance | – | 100 | – | Ω |
| $C_{EXT}$ | Required external AC coupling capacitor | – | 10 | – | nF |

*Table 61:* **GTY Transceiver Clock Output Level Specification**

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{OL}$ | Output Low voltage for P and N | $R_T$ = 100Ω across P and N signals | 100 | – | 330 | mV |
| $V_{OH}$ | Output High voltage for P and N | $R_T$ = 100Ω across P and N signals | 500 | – | 700 | mV |
| $V_{DDOUT}$ | Differential output voltage<br>(P–N), P = High<br>(N–P), N = High | $R_T$ = 100Ω across P and N signals | 300 | – | 430 | mV |
| $V_{CMOUT}$ | Common mode voltage | $R_T$ = 100Ω across P and N signals | 300 | – | 500 | mV |

# Integrated Interface Block for Interlaken

More information and documentation on solutions using the integrated interface block for Interlaken can be found at UltraScale Interlaken. The *UltraScale Architecture and Product Overview* (DS890) lists how many blocks are in each Kintex UltraScale+ FPGA. This section describes the following Interlaken configurations.

- 12 x 12.5 Gb/s protocol and lane logic mode (Table 71).
- 6 x 25.78125 Gb/s and 6 x 28.21 Gb/s protocol and lane logic mode (Table 72).
- 12 x 25.78125 Gb/s lane logic only mode (Table 73).

Kintex UltraScale+ FPGAs in the SFVB784, FFVA676, and FFVA1156 packages are only supported using the 12 x 12.5 Gb/s Interlaken configuration. See Table 62 for the $F_{GTYMAX}$ description.

*Table 71:* **Maximum Performance for Interlaken 12 x 12.5 Gb/s Protocol and Lane Logic Mode Designs**

| Symbol | Description | Speed Grade and $V_{CCINT}$ Operating Voltages | | | | | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 0.90V | | 0.85V | | | | 0.72V | | | | |
| | | -3 | | -2 | | -1 | | -2 | | -1 | | |
| $F_{RX\_SERDES\_CLK}$ | Receive serializer/ deserializer clock | 195.32 | | 195.32 | | 195.32 | | 195.32 | | 195.32 | | MHz |
| $F_{TX\_SERDES\_CLK}$ | Transmit serializer/ deserializer clock | 195.32 | | 195.32 | | 195.32 | | 195.32 | | 195.32 | | MHz |
| $F_{DRP\_CLK}$ | Dynamic reconfiguration port clock | 250.00 | | 250.00 | | 250.00 | | 250.00 | | 250.00 | | MHz |
| | | Min(1) | Max | Min(1) | Max | Min(1) | Max | Min(1) | Max | Min(1) | Max | |
| $F_{CORE\_CLK}$ | Interlaken core clock | 300.00 | 322.27 | 300.00 | 322.27 | 300.00 | 322.27 | 300.00 | 322.27 | 300.00 | 322.27 | MHz |
| $F_{LBUS\_CLK}$ | Interlaken local bus clock | 300.00 | 322.27 | 300.00 | 322.27 | 300.00 | 322.27 | 300.00 | 322.27 | 300.00 | 322.27 | MHz |

**Notes:**

1. These are the minimum clock frequencies at the maximum lane performance.

# Integrated Interface Block for 100G Ethernet MAC and PCS

More information and documentation on solutions using the integrated 100 Gb/s Ethernet block can be found at UltraScale Integrated 100G Ethernet MAC/PCS. The *UltraScale Architecture and Product Overview* (DS890) lists how many blocks are in each Kintex UltraScale+ FPGA.

*Table 74:* **Maximum Performance for 100G Ethernet Designs**

| Symbol | Description | Speed Grade and $V_{CCINT}$ Operating Voltages | | | | | Units |
|---|---|---|---|---|---|---|---|
| | | 0.90V | 0.85V | | 0.72V | | |
| | | -3 | -2(1) | -1 | -2 | -1(2) | |
| $F_{TX\_CLK}$ | Transmit clock | 390.625 | 390.625 | 322.223 | 322.223 | 322.223 | MHz |
| $F_{RX\_CLK}$ | Receive clock | 390.625 | 390.625 | 322.223 | 322.223 | 322.223 | MHz |
| $F_{RX\_SERDES\_CLK}$ | Receive serializer/deserializer clock | 390.625 | 390.625 | 322.223 | 322.223 | 322.223 | MHz |
| $F_{DRP\_CLK}$ | Dynamic reconfiguration port clock | 250.00 | 250.00 | 250.00 | 250.00 | 250.00 | MHz |

**Notes:**
1. The maximum clock frequency of 390.625 MHz only applies to the CAUI-10 interface. The maximum clock frequency for the CAUI-4 interface is 322.223 MHz.
2. The CAUI-4 interface is not supported by -1L speed grade devices where $V_{CCINT}$=0.72V.

# Integrated Interface Block for PCI Express Designs

More information and documentation on solutions for PCI Express designs can be found at PCI Express. The *UltraScale Architecture and Product Overview* (DS890) lists how many blocks are in each Kintex UltraScale+ FPGA.

*Table 75:* **Maximum Performance for PCI Express Designs(1)(2)**

| Symbol | Description | Speed Grade and $V_{CCINT}$ Operating Voltages | | | | | Units |
|---|---|---|---|---|---|---|---|
| | | 0.90V | 0.85V | | 0.72V | | |
| | | -3 | -2 | -1 | -2 | -1 | |
| $F_{PIPECLK}$ | Pipe clock maximum frequency. | 250.00 | 250.00 | 250.00 | 250.00 | 250.00 | MHz |
| $F_{CORECLK}$ | Core clock maximum frequency. | 500.00 | 500.00 | 500.00 | 250.00 | 250.00 | MHz |
| $F_{DRPCLK}$ | DRP clock maximum frequency. | 250.00 | 250.00 | 250.00 | 250.00 | 250.00 | MHz |
| $F_{MCAPCLK}$ | MCAP clock maximum frequency. | 125.00 | 125.00 | 125.00 | 125.00 | 125.00 | MHz |

**Notes:**
1. PCI Express Gen4 operation is supported for x1, x2, x4, and x8 widths.
2. PCI Express Gen4 operation is supported in -3E, -2E, and -2I speed grades.

*Table 76:* **System Monitor Specifications *(Cont'd)***

| Parameter | Symbol | Comments/Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Supply sensor error[4] | | Supply voltages 0.72V to 1.2V, $T_j$ = –40°C to 100°C (with external REF) | – | – | ±0.5 | % |
| | | Supply voltages 0.72V to 1.2V, $T_j$ = –55°C to 125°C (with external REF) | – | – | ±1.0 | % |
| | | All other supply voltages, $T_j$ = –40°C to 100°C (with external REF) | – | – | ±1.0 | % |
| | | All other supply voltages, $T_j$ = –55°C to 125°C (with external REF) | – | – | ±2.0 | % |
| | | Supply voltages 0.72V to 1.2V, $T_j$ = –40°C to 100°C (with internal REF) | – | – | ±1.0 | % |
| | | Supply voltages 0.72V to 1.2V, $T_j$ = –55°C to 125°C (with internal REF) | – | – | ±2.0 | % |
| | | All other supply voltages, $T_j$ = –40°C to 100°C (with internal REF) | – | – | ±1.5 | % |
| | | All other supply voltages, $T_j$ = –55°C to 125°C (with internal REF) | – | – | ±2.5 | % |
| **Conversion Rate[5]** | | | | | | |
| Conversion time—continuous | $t_{CONV}$ | Number of ADCCLK cycles | 26 | – | 32 | Cycles |
| Conversion time—event | $t_{CONV}$ | Number of ADCCLK cycles | – | – | 21 | Cycles |
| DRP clock frequency | DCLK | DRP clock frequency | 8 | – | 250 | MHz |
| ADC clock frequency | ADCCLK | Derived from DCLK | 1 | – | 5.2 | MHz |
| DCLK duty cycle | | | 40 | – | 60 | % |
| **SYSMON Reference[6]** | | | | | | |
| External reference | $V_{REFP}$ | Externally supplied reference voltage | 1.20 | 1.25 | 1.30 | V |
| On-chip reference | | Ground $V_{REFP}$ pin to AGND, $T_j$ = –40°C to 100°C | 1.2375 | 1.25 | 1.2625 | V |
| | | Ground $V_{REFP}$ pin to AGND, $T_j$ = –55°C to 125°C | 1.225 | 1.25 | 1.275 | V |

**Notes:**

1. ADC offset errors are removed by enabling the ADC automatic offset calibration feature. The values are specified for when this feature is enabled.
2. See the *Analog Input* section in the *UltraScale Architecture System Monitor User Guide* (UG580).
3. When reading temperature values directly from the PMBus interface, the SYSMON has a +4°C offset due to the transfer function used by the PMBus application. For example, the external REF temperature sensor error's range of ±3°C becomes +1°C to +7°C when the temperature is read through the PMBus interface.
4. Supply sensor offset and gain errors are removed by enabling the automatic offset and gain calibration feature. The values are specified for when this feature is enabled.
5. See the *Adjusting the Acquisition Settling Time* section in the *UltraScale Architecture System Monitor User Guide* (UG580).
6. Any variation in the reference voltage from the nominal $V_{REFP}$ = 1.25V and $V_{REFN}$ = 0V will result in a deviation from the ideal transfer function. This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric type applications allowing reference to vary by ±4% is permitted.

# SYSMON I2C/PMBus Interfaces

*Table 77:* **SYSMON I2C Fast Mode Interface Switching Characteristics(1)**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $T_{SMFCKL}$ | SCL Low time | 1.3 | – | µs |
| $T_{SMFCKH}$ | SCL High time | 0.6 | – | µs |
| $T_{SMFCKO}$ | SDAO clock-to-out delay | – | 900 | ns |
| $T_{SMFDCK}$ | SDAI setup time | 100 | – | ns |
| $F_{SMFCLK}$ | SCL clock frequency | – | 400 | kHz |

**Notes:**
1. The test conditions are configured to the LVCMOS 1.8V I/O standard.

*Table 78:* **SYSMON I2C Standard Mode Interface Switching Characteristics(1)**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $T_{SMSCKL}$ | SCL Low time | 4.7 | – | µs |
| $T_{SMSCKH}$ | SCL High time | 4.0 | – | µs |
| $T_{SMSCKO}$ | SDAO clock-to-out delay | – | 3450 | ns |
| $T_{SMSDCK}$ | SDAI setup time | 250 | – | ns |
| $F_{SMSCLK}$ | SCL clock frequency | – | 100 | kHz |

**Notes:**
1. The test conditions are configured to the LVCMOS 1.8V I/O standard.

# Notice of Disclaimer



## Automotive Applications Disclaimer