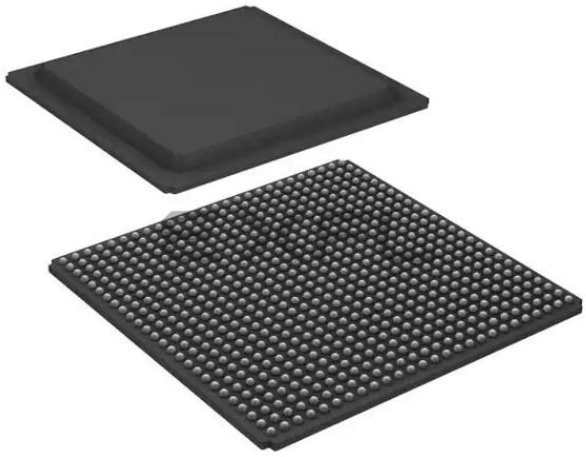

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	20340
Number of Logic Elements/Cells	355950
Total RAM Bits	31641600
Number of I/O	280
Number of Gates	-
Voltage - Supply	0.698V ~ 0.876V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	676-BBGA, FCBGA
Supplier Device Package	676-FCBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcku3p-l2ffvb676e

Table 1: **Absolute Maximum Ratings(1) *(Cont'd)***

Symbol	Description	Min	Max	Units
Temperature				
T_{STG}	Storage temperature (ambient).	–65	150	°C
T_{SOL}	Maximum soldering temperature.(12)	–	260	°C
T_j	Maximum junction temperature.(12)	–	125	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. V_{CCINT_IO} must be connected to V_{CCBRAM}.
3. V_{CCAUX_IO} must be connected to V_{CCAUX}.
4. The lower absolute voltage specification always applies.
5. If V_{CCO} is 3.3V, the maximum voltage is 3.4V.
6. For I/O operation, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).
7. When operating outside of the recommended operating conditions, refer to Table 4 and Table 5 for maximum overshoot and undershoot specifications.
8. AC coupled operation is not supported for RX termination = floating.
9. For GTY transceivers, DC coupled operation is not supported for RX termination = GND.
10. DC coupled operation is not supported for RX termination = programmable.
11. For more information on supported GTH or GTY transceiver terminations see the *UltraScale Architecture GTH Transceiver User Guide* (UG576) or *UltraScale Architecture GTY Transceiver User Guide* (UG578).
12. For soldering guidelines and thermal considerations, see the *UltraScale and UltraScale+ FPGAs Packaging and Pinout Specifications* (UG575).

Recommended Operating Conditions

Table 2: **Recommended Operating Conditions(1)(2)**

Symbol	Description	Min	Typ	Max	Units
FPGA Logic					
V_{CCINT}	Internal supply voltage.	0.825	0.850	0.876	V
	For -1LI and -2LE devices (V_{CCINT} = 0.72V): internal supply voltage.	0.698	0.720	0.742	V
	For -3E devices: internal supply voltage.	0.873	0.900	0.927	V
V_{CCINT_IO}(3)	Internal supply voltage for the I/O banks.	0.825	0.850	0.876	V
	For -1LI and -2LE devices (V_{CCINT} = 0.72V): internal supply voltage for the I/O banks.	0.825	0.850	0.876	V
	For -3E devices: internal supply voltage for the I/O banks.	0.873	0.900	0.927	V
V_{CCBRAM}	Block RAM supply voltage.	0.825	0.850	0.876	V
	For -3E devices: block RAM supply voltage.	0.873	0.900	0.927	V
V_{CCAUX}	Auxiliary supply voltage.	1.746	1.800	1.854	V
V_{CCO}(4)(5)	Supply voltage for HD I/O banks.	1.140	–	3.400	V
	Supply voltage for HP I/O banks.	0.950	–	1.900	V
V_{CCAUX_IO}(6)	Auxiliary I/O supply voltage.	1.746	1.800	1.854	V
V_{IN}(7)	I/O input voltage.	–0.200	–	V_{CCO} + 0.200	V
I_{IN}(8)	Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode.	–	–	10	mA
V_{BATT}(9)	Battery voltage	1.000	–	1.890	V

Power-On/Off Power Supply Sequencing

The recommended power-on sequence is V_{CCINT}, V_{CCINT_IO}/V_{CCBRAM}, V_{CCAUX}/V_{CCAUX_IO}, and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCINT} and V_{CCINT_IO}/V_{CCBRAM} have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously. V_{CCINT_IO} must be connected to V_{CCBRAM}. If V_{CCAUX}/V_{CCAUX_IO} and V_{CCO} have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously. V_{CCAUX} and V_{CCAUX_IO} must be connected together. V_{CCADC} and V_{REF} can be powered at any time and have no power-up sequencing requirements.

The recommended power-on sequence to achieve minimum current draw for the GTH or GTY transceivers is V_{CCINT}, $V_{MGTAVCC}$, $V_{MGTAVTT}$ OR $V_{MGTAVCC}$, V_{CCINT}, $V_{MGTAVTT}$. There is no recommended sequencing for $V_{MGTVCCAUX}$. Both $V_{MGTAVCC}$ and V_{CCINT} can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw.

If these recommended sequences are not met, current drawn from $V_{MGTAVTT}$ can be higher than specifications during power-up and power-down.

Table 10: **SelectIO DC Input and Output Levels for HP I/O Banks(1)(2)(3)**

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
HSTL_I	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	5.8	–5.8
HSTL_I_12	–0.300	V_{REF} – 0.080	V_{REF} + 0.080	V_{CCO} + 0.300	25% V_{CCO}	75% V_{CCO}	4.1	–4.1
HSTL_I_18	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	6.2	–6.2
HSUL_12	–0.300	V_{REF} – 0.130	V_{REF} + 0.130	V_{CCO} + 0.300	20% V_{CCO}	80% V_{CCO}	0.1	–0.1
LVCMOS12	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	Note 4	Note 4
LVCMOS15	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	Note 5	Note 5
LVCMOS18	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	Note 5	Note 5
LVDCI_15	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	7.0	–7.0
LVDCI_18	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	7.0	–7.0
SSTL12	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{CCO}/2 – 0.150	V_{CCO}/2 + 0.150	8.0	–8.0
SSTL135	–0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO} + 0.300	V_{CCO}/2 – 0.150	V_{CCO}/2 + 0.150	9.0	–9.0
SSTL15	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{CCO}/2 – 0.175	V_{CCO}/2 + 0.175	10.0	–10.0
SSTL18_I	–0.300	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.300	V_{CCO}/2 – 0.470	V_{CCO}/2 + 0.470	7.0	–7.0
MIPI_DPHY_DCI_LP(6)	–0.300	0.550	0.880	V_{CCO} + 0.300	0.050	1.100	0.01	–0.01

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).
3. POD10 and POD12 DC input and output levels are shown in Table 11, Table 15, Table 16, and Table 17.
4. Supported drive strengths of 2, 4, 6, or 8 mA in HP I/O banks.
5. Supported drive strengths of 2, 4, 6, 8, or 12 mA in HP I/O banks.
6. Low-power option for MIPI_DPHY_DCI.

Table 11: **DC Input Levels for Single-ended POD10 and POD12 I/O Standards(1)(2)**

I/O Standard	V_{IL}		V_{IH}	
	V, Min	V, Max	V, Min	V, Max
POD10	–0.300	V_{REF} – 0.068	V_{REF} + 0.068	V_{CCO} + 0.300
POD12	–0.300	V_{REF} – 0.068	V_{REF} + 0.068	V_{CCO} + 0.300

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

Table 14: **Complementary Differential SelectIO DC Input and Output Levels for HP I/O Banks(1)**

I/O Standard	V_{ICM} (V)(2)			V_{ID} (V)(3)		V_{OL} (V)(4)	V_{OH} (V)(5)	I_{OL}	I_{OH}
	Min	Typ	Max	Min	Max	Max	Min	mA	mA
DIFF_HSTL_I	0.680	$V_{CCO}/2$	($V_{CCO}/2$) + 0.150	0.100	–	0.400	V_{CCO} – 0.400	5.8	–5.8
DIFF_HSTL_I_12	0.400 x V_{CCO}	$V_{CCO}/2$	0.600 x V_{CCO}	0.100	–	0.250 x V_{CCO}	0.750 x V_{CCO}	4.1	–4.1
DIFF_HSTL_I_18	($V_{CCO}/2$) – 0.175	$V_{CCO}/2$	($V_{CCO}/2$) + 0.175	0.100	–	0.400	V_{CCO} – 0.400	6.2	–6.2
DIFF_HSUL_12	($V_{CCO}/2$) – 0.120	$V_{CCO}/2$	($V_{CCO}/2$) + 0.120	0.100	–	20% V_{CCO}	80% V_{CCO}	0.1	–0.1
DIFF_SSTL12	($V_{CCO}/2$) – 0.150	$V_{CCO}/2$	($V_{CCO}/2$) + 0.150	0.100	–	($V_{CCO}/2$) – 0.150	($V_{CCO}/2$) + 0.150	8.0	–8.0
DIFF_SSTL135	($V_{CCO}/2$) – 0.150	$V_{CCO}/2$	($V_{CCO}/2$) + 0.150	0.100	–	($V_{CCO}/2$) – 0.150	($V_{CCO}/2$) + 0.150	9.0	–9.0
DIFF_SSTL15	($V_{CCO}/2$) – 0.175	$V_{CCO}/2$	($V_{CCO}/2$) + 0.175	0.100	–	($V_{CCO}/2$) – 0.175	($V_{CCO}/2$) + 0.175	10.0	–10.0
DIFF_SSTL18_I	($V_{CCO}/2$) – 0.175	$V_{CCO}/2$	($V_{CCO}/2$) + 0.175	0.100	–	($V_{CCO}/2$) – 0.470	($V_{CCO}/2$) + 0.470	7.0	–7.0

Notes:

1. DIFF_POD10 and DIFF_POD12 HP I/O bank specifications are shown in Table 15, Table 16, and Table 17.
2. V_{ICM} is the input common mode voltage.
3. V_{ID} is the input differential voltage.
4. V_{OL} is the single-ended low-output voltage.
5. V_{OH} is the single-ended high-output voltage.

Table 15: **DC Input Levels for Differential POD10 and POD12 I/O Standards(1)(2)**

I/O Standard	V_{ICM} (V)			V_{ID} (V)	
	Min	Typ	Max	Min	Max
DIFF_POD10	0.63	0.70	0.77	0.14	–
DIFF_POD12	0.76	0.84	0.92	0.16	–

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

Table 16: **DC Output Levels for Single-ended and Differential POD10 and POD12 Standards(1)(2)**

Symbol	Description	V_{OUT}	Min	Typ	Max	Units
R_{OL}	Pull-down resistance.	V_{OM_DC} (as described in Table 17)	36	40	44	Ω
R_{OH}	Pull-up resistance.	V_{OM_DC} (as described in Table 17)	36	40	44	Ω

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

Table 17: **Table 16 Definitions for DC Output Levels for POD Standards**

Symbol	Description	All Speed Grades	Units
V_{OM_DC}	DC output Mid measurement level (for IV curve linearity).	0.8 x V_{CCO}	V

Production Silicon and Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases.

Table 22 lists the production released Kintex UltraScale+ FPGAs, speed grade, and the minimum corresponding supported speed specification version and Vivado software revisions. The Vivado software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 22: **Kintex UltraScale+ FPGA Device Production Software and Speed Specification Release**

Device	Speed Grade and V_{CCINT} Operating Voltages						
	0.90V	0.85V				0.72V	
	-3	-2	-1	-2L	-1L	-2L	-1L
XCKU3P		Vivado tools 2017.1 v1.10					
XCKU5P		Vivado tools 2017.1 v1.10					
XCKU9P							
XCKU11P							
XCKU13P							
XCKU15P							

Notes:

1. Blank entries indicate a device and/or speed grade in Advance or Preliminary status.

FPGA Logic Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Kintex UltraScale+ FPGAs. These values are subject to the same guidelines as the AC Switching Characteristics, page 16. In each table, the I/O bank type is either high performance (HP) or high density (HD).

Table 23: **LVDS Component Mode Performance**

Description	I/O Bank Type	Speed Grade and V_{CCINT} Operating Voltages										Units
		0.90V		0.85V				0.72V				
		-3		-2		-1		-2		-1		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
LVDS TX DDR (OSERDES 4:1, 8:1)	HP	0	1250	0	1250	0	1250	0	1250	0	1250	Mb/s
LVDS TX SDR (OSERDES 2:1, 4:1)	HP	0	625	0	625	0	625	0	625	0	625	Mb/s
LVDS RX DDR (ISERDES 1:4, 1:8)(1)	HP	0	1250	0	1250	0	1250	0	1250	0	1250	Mb/s
LVDS RX DDR	HD	0	250	0	250	0	250	0	250	0	250	Mb/s
LVDS RX SDR (ISERDES 1:2, 1:4)(1)	HP	0	625	0	625	0	625	0	625	0	625	Mb/s
LVDS RX SDR	HD	0	125	0	125	0	125	0	125	0	125	Mb/s

Notes:

1. LVDS receivers are typically bounded with certain applications to achieve maximum performance. Package skews are not included and should be removed through PCB routing.

Table 24: **LVDS Native Mode Performance(1)(2)**

Description	DATA_WIDTH	I/O Bank Type	Speed Grade and V_{CCINT} Operating Voltages										Units
			0.90V		0.85V				0.72V				
			-3		-2		-1		-2		-1		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
LVDS TX DDR (TX_BITSLICE)	4	HP	375	1600	375	1600	375	1260	375	1400	375	1260	Mb/s
	8		375	1600	375	1600	375	1260	375	1600	375	1260	Mb/s
LVDS TX SDR (TX_BITSLICE)	4	HP	187.5	800	187.5	800	187.5	630	187.5	700	187.5	630	Mb/s
	8		187.5	800	187.5	800	187.5	630	187.5	800	187.5	630	Mb/s
LVDS RX DDR (RX_BITSLICE)(3)	4	HP	375	1600	375	1600	375	1260	375	1400	375	1260	Mb/s
	8		375	1600	375	1600	375	1260	375	1600	375	1260	Mb/s
LVDS RX SDR (RX_BITSLICE)(3)	4	HP	187.5	800	187.5	800	187.5	630	187.5	700	187.5	630	Mb/s
	8		187.5	800	187.5	800	187.5	630	187.5	800	187.5	630	Mb/s

Notes:

1. Native mode is supported through the High-Speed SelectIO Interface Wizard available with the Vivado Design Suite. The performance values assume a source-synchronous interface.
2. PLL settings can restrict the minimum allowable data rate. For example, when using the PLL with CLKOUTPHY_MODE = VCO_HALF the minimum frequency is PLL_FVCOMIN/2.
3. LVDS receivers are typically bounded with certain applications to achieve maximum performance. Package skews are not included and should be removed through PCB routing.

Table 25: **MIPI D-PHY Performance**

Description	I/O Bank Type	Speed Grade and V_{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
MIPI D-PHY transmitter or receiver.	HP	1500	1500	1260	1260	1260	Mb/s

Table 26: **LVDS Native-Mode 1000BASE-X Support(1)**

Description	I/O Bank Type	Speed Grade and V_{CCINT} Operating Voltages				
		0.90V	0.85V		0.72V	
		-3	-2	-1	-2	-1
1000BASE-X	HP	Yes				

Notes:

1. 1000BASE-X support is based on the *IEEE Standard for CSMA/CD Access Method and Physical Layer Specifications* (IEEE Std 802.3-2008).

Table 27 provides the maximum data rates for applicable memory standards using the Kintex UltraScale+ FPGA memory PHY. Refer to Memory Interfaces for the complete list of memory interface standards supported and detailed specifications. The final performance of the memory interface is determined through a complete design implemented in the Vivado Design Suite, following guidelines in the *UltraScale Architecture PCB Design Guide* (UG583), electrical analysis, and characterization of the system.

Table 27: **Maximum Physical Interface (PHY) Rate for Memory Interfaces**

Memory Standard	Package	DRAM Type	Speed Grade and V_{CCINT} Operating Voltages					Units
			0.90V	0.85V		0.72V		
			-3	-2	-1	-2	-1	
DDR4	All FFV packages	Single rank component	2666	2666	2400	2400	2133	Mb/s
		1 rank DIMM(1)(2)(3)	2400	2400	2133	2133	1866	Mb/s
		2 rank DIMM(1)(4)	2133	2133	1866	1866	1600	Mb/s
		4 rank DIMM(1)(5)	1600	1600	1333	1333	N/A	Mb/s
	SFVB784	Single rank component	2400	2400	2133	2133	1866	Mb/s
		1 rank DIMM(1)(2)	2133	2133	1866	1866	1600	Mb/s
		2 rank DIMM(1)(4)	1866	1866	1600	1600	1600	Mb/s
DDR3	All FFV packages	Single rank component	2133	2133	2133	2133	1866	Mb/s
		1 rank DIMM(1)(2)	1866	1866	1866	1866	1600	Mb/s
		2 rank DIMM(1)(4)	1600	1600	1600	1600	1333	Mb/s
		4 rank DIMM(1)(5)	1066	1066	1066	1066	800	Mb/s
	SFVB784	Single rank component	1866	1866	1866	1866	1600	Mb/s
		1 rank DIMM(1)(2)	1600	1600	1600	1600	1600	Mb/s
		2 rank DIMM(1)(4)	1600	1600	1600	1600	1333	Mb/s
		4 rank DIMM(1)(5)	1066	1066	1066	1066	800	Mb/s