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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 20340 |
| Number of Logic Elements/Cells | 355950 |
| Total RAM Bits | 31641600 |
| Number of I/O | 256 |
| Number of Gates | - |
| Voltage - Supply | 0.698V ~ 0.876V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 100°C (TJ) |
| Package / Case | 784-BFBGA, FCBGA |
| Supplier Device Package | 784-FCBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xcku3p-l2sfvb784e |

# DC Input and Output Levels

Values for $V_{IL}$ and $V_{IH}$ are recommended input voltages. Values for $I_{OL}$ and $I_{OH}$ are guaranteed over the recommended operating conditions at the $V_{OL}$ and $V_{OH}$ test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum $V_{CCO}$ with the respective $V_{OL}$ and $V_{OH}$ voltage levels shown. Other standards are sample tested.

*Table 9:* **SelectIO DC Input and Output Levels For HD I/O Banks(1)(2)(3)**

| I/O Standard | $V_{IL}$ | | $V_{IH}$ | | $V_{OL}$ | $V_{OH}$ | $I_{OL}$ | $I_{OH}$ |
|---|---|---|---|---|---|---|---|---|
| | V, Min | V, Max | V, Min | V, Max | V, Max | V, Min | mA | mA |
| HSTL_I | –0.300 | $V_{REF}$ – 0.100 | $V_{REF}$ + 0.100 | $V_{CCO}$ + 0.300 | 0.400 | $V_{CCO}$ – 0.400 | 8.0 | –8.0 |
| HSTL_I_18 | –0.300 | $V_{REF}$ – 0.100 | $V_{REF}$ + 0.100 | $V_{CCO}$ + 0.300 | 0.400 | $V_{CCO}$ – 0.400 | 8.0 | –8.0 |
| HSUL_12 | –0.300 | $V_{REF}$ – 0.130 | $V_{REF}$ + 0.130 | $V_{CCO}$ + 0.300 | 20% $V_{CCO}$ | 80% $V_{CCO}$ | 0.1 | –0.1 |
| LVCMOS12 | –0.300 | 35% $V_{CCO}$ | 65% $V_{CCO}$ | $V_{CCO}$ + 0.300 | 0.400 | $V_{CCO}$ – 0.400 | Note 4 | Note 4 |
| LVCMOS15 | –0.300 | 35% $V_{CCO}$ | 65% $V_{CCO}$ | $V_{CCO}$ + 0.300 | 0.450 | $V_{CCO}$ – 0.450 | Note 5 | Note 5 |
| LVCMOS18 | –0.300 | 35% $V_{CCO}$ | 65% $V_{CCO}$ | $V_{CCO}$ + 0.300 | 0.450 | $V_{CCO}$ – 0.450 | Note 5 | Note 5 |
| LVCMOS25 | –0.300 | 0.700 | 1.700 | $V_{CCO}$ + 0.300 | 0.400 | $V_{CCO}$ – 0.400 | Note 5 | Note 5 |
| LVCMOS33 | –0.300 | 0.800 | 2.000 | 3.400 | 0.400 | $V_{CCO}$ – 0.400 | Note 5 | Note 5 |
| LVTTL | –0.300 | 0.800 | 2.000 | 3.400 | 0.400 | 2.400 | Note 5 | Note 5 |
| SSTL12 | –0.300 | $V_{REF}$ – 0.100 | $V_{REF}$ + 0.100 | $V_{CCO}$ + 0.300 | $V_{CCO}$/2 – 0.150 | $V_{CCO}$/2 + 0.150 | 14.25 | –14.25 |
| SSTL135 | –0.300 | $V_{REF}$ – 0.090 | $V_{REF}$ + 0.090 | $V_{CCO}$ + 0.300 | $V_{CCO}$/2 – 0.150 | $V_{CCO}$/2 + 0.150 | 8.9 | –8.9 |
| SSTL135_II | –0.300 | $V_{REF}$ – 0.090 | $V_{REF}$ + 0.090 | $V_{CCO}$ + 0.300 | $V_{CCO}$/2 – 0.150 | $V_{CCO}$/2 + 0.150 | 13.0 | –13.0 |
| SSTL15 | –0.300 | $V_{REF}$ – 0.100 | $V_{REF}$ + 0.100 | $V_{CCO}$ + 0.300 | $V_{CCO}$/2 – 0.175 | $V_{CCO}$/2 + 0.175 | 8.9 | –8.9 |
| SSTL15_II | –0.300 | $V_{REF}$ – 0.100 | $V_{REF}$ + 0.100 | $V_{CCO}$ + 0.300 | $V_{CCO}$/2 – 0.175 | $V_{CCO}$/2 + 0.175 | 13.0 | –13.0 |
| SSTL18_I | –0.300 | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 | $V_{CCO}$ + 0.300 | $V_{CCO}$/2 – 0.470 | $V_{CCO}$/2 + 0.470 | 8.0 | –8.0 |
| SSTL18_II | –0.300 | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 | $V_{CCO}$ + 0.300 | $V_{CCO}$/2 – 0.600 | $V_{CCO}$/2 + 0.600 | 13.4 | –13.4 |
| MIPI_DPHY_DCI_LP(6) | –0.300 | 0.550 | 0.880 | $V_{CCO}$ + 0.300 | 0.050 | 1.100 | 0.01 | –0.01 |

**Notes:**

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).
3. POD10 and POD12 DC input and output levels are shown in Table 11, Table 15, Table 16, and Table 17.
4. Supported drive strengths of 4, 8, or 12 mA in HD I/O banks.
5. Supported drive strengths of 4, 8, 12, or 16 mA in HD I/O banks.
6. Low-power option for MIPI_DPHY_DCI.

*Table 10:* **SelectIO DC Input and Output Levels for HP I/O Banks(1)(2)(3)**

| I/O Standard | $V_{IL}$ | | $V_{IH}$ | | $V_{OL}$ | $V_{OH}$ | $I_{OL}$ | $I_{OH}$ |
|---|---|---|---|---|---|---|---|---|
| | V, Min | V, Max | V, Min | V, Max | V, Max | V, Min | mA | mA |
| HSTL_I | –0.300 | $V_{REF}$ – 0.100 | $V_{REF}$ + 0.100 | $V_{CCO}$ + 0.300 | 0.400 | $V_{CCO}$ – 0.400 | 5.8 | –5.8 |
| HSTL_I_12 | –0.300 | $V_{REF}$ – 0.080 | $V_{REF}$ + 0.080 | $V_{CCO}$ + 0.300 | 25% $V_{CCO}$ | 75% $V_{CCO}$ | 4.1 | –4.1 |
| HSTL_I_18 | –0.300 | $V_{REF}$ – 0.100 | $V_{REF}$ + 0.100 | $V_{CCO}$ + 0.300 | 0.400 | $V_{CCO}$ – 0.400 | 6.2 | –6.2 |
| HSUL_12 | –0.300 | $V_{REF}$ – 0.130 | $V_{REF}$ + 0.130 | $V_{CCO}$ + 0.300 | 20% $V_{CCO}$ | 80% $V_{CCO}$ | 0.1 | –0.1 |
| LVCMOS12 | –0.300 | 35% $V_{CCO}$ | 65% $V_{CCO}$ | $V_{CCO}$ + 0.300 | 0.400 | $V_{CCO}$ – 0.400 | Note 4 | Note 4 |
| LVCMOS15 | –0.300 | 35% $V_{CCO}$ | 65% $V_{CCO}$ | $V_{CCO}$ + 0.300 | 0.450 | $V_{CCO}$ – 0.450 | Note 5 | Note 5 |
| LVCMOS18 | –0.300 | 35% $V_{CCO}$ | 65% $V_{CCO}$ | $V_{CCO}$ + 0.300 | 0.450 | $V_{CCO}$ – 0.450 | Note 5 | Note 5 |
| LVDCI_15 | –0.300 | 35% $V_{CCO}$ | 65% $V_{CCO}$ | $V_{CCO}$ + 0.300 | 0.450 | $V_{CCO}$ – 0.450 | 7.0 | –7.0 |
| LVDCI_18 | –0.300 | 35% $V_{CCO}$ | 65% $V_{CCO}$ | $V_{CCO}$ + 0.300 | 0.450 | $V_{CCO}$ – 0.450 | 7.0 | –7.0 |
| SSTL12 | –0.300 | $V_{REF}$ – 0.100 | $V_{REF}$ + 0.100 | $V_{CCO}$ + 0.300 | $V_{CCO}$/2 – 0.150 | $V_{CCO}$/2 + 0.150 | 8.0 | –8.0 |
| SSTL135 | –0.300 | $V_{REF}$ – 0.090 | $V_{REF}$ + 0.090 | $V_{CCO}$ + 0.300 | $V_{CCO}$/2 – 0.150 | $V_{CCO}$/2 + 0.150 | 9.0 | –9.0 |
| SSTL15 | –0.300 | $V_{REF}$ – 0.100 | $V_{REF}$ + 0.100 | $V_{CCO}$ + 0.300 | $V_{CCO}$/2 – 0.175 | $V_{CCO}$/2 + 0.175 | 10.0 | –10.0 |
| SSTL18_I | –0.300 | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 | $V_{CCO}$ + 0.300 | $V_{CCO}$/2 – 0.470 | $V_{CCO}$/2 + 0.470 | 7.0 | –7.0 |
| MIPI_DPHY_DCI_LP(6) | –0.300 | 0.550 | 0.880 | $V_{CCO}$ + 0.300 | 0.050 | 1.100 | 0.01 | –0.01 |

**Notes:**

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).
3. POD10 and POD12 DC input and output levels are shown in Table 11, Table 15, Table 16, and Table 17.
4. Supported drive strengths of 2, 4, 6, or 8 mA in HP I/O banks.
5. Supported drive strengths of 2, 4, 6, 8, or 12 mA in HP I/O banks.
6. Low-power option for MIPI_DPHY_DCI.

*Table 11:* **DC Input Levels for Single-ended POD10 and POD12 I/O Standards(1)(2)**

| I/O Standard | $V_{IL}$ | | $V_{IH}$ | |
|---|---|---|---|---|
| | V, Min | V, Max | V, Min | V, Max |
| POD10 | –0.300 | $V_{REF}$ – 0.068 | $V_{REF}$ + 0.068 | $V_{CCO}$ + 0.300 |
| POD12 | –0.300 | $V_{REF}$ – 0.068 | $V_{REF}$ + 0.068 | $V_{CCO}$ + 0.300 |

**Notes:**

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

*Table 12:* **Differential SelectIO DC Input and Output Levels**

| I/O Standard | $V_{ICM}$ (V)(1) | | | $V_{ID}$(V)(2) | | | $V_{ILHS}$(3) | $V_{IHHS}$(3) | $V_{OCM}$(V)(4) | | | $V_{OD}$(V)(5) | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max | Min | Max | Min | Typ | Max | Min | Typ | Max |
| SUB_LVDS(8) | 0.500 | 0.900 | 1.300 | 0.070 | – | – | – | – | 0.700 | 0.900 | 1.100 | 0.100 | 0.150 | 0.200 |
| LVPECL | 0.300 | 1.200 | 1.425 | 0.100 | 0.350 | 0.600 | – | – | – | – | – | – | – | – |
| SLVS_400_18 | 0.070 | 0.200 | 0.330 | 0.140 | – | 0.450 | – | – | – | – | – | – | – | – |
| SLVS_400_25 | 0.070 | 0.200 | 0.330 | 0.140 | – | 0.450 | – | – | – | – | – | – | – | – |
| MIPI_DPHY_DCI_HS(9) | 0.070 | – | 0.330 | 0.070 | – | – | –0.040 | 0.460 | 0.150 | 0.200 | 0.250 | 0.140 | 0.200 | 0.270 |

**Notes:**

1. $V_{ICM}$ is the input common mode voltage.
2. $V_{ID}$ is the input differential voltage (Q – $\overline{Q}$).
3. $V_{IHHS}$ and $V_{ILHS}$ are the single-ended input high and low voltages, respectively.
4. $V_{OCM}$ is the output common mode voltage.
5. $V_{OD}$ is the output differential voltage (Q – $\overline{Q}$).
6. LVDS_25 is specified in Table 18.
7. LVDS is specified in Table 19.
8. Only the SUB_LVDS receiver is supported in HD I/O banks.
9. High-speed option for MIPI_DPHY_DCI. The $V_{ID}$ maximum is aligned with the standard's specification. A higher $V_{ID}$ is acceptable as long as the $V_{IN}$ specification is also met.

*Table 13:* **Complementary Differential SelectIO DC Input and Output Levels for HD I/O Banks**

| I/O Standard | $V_{ICM}$ (V)(1) | | | $V_{ID}$ (V)(2) | | $V_{OL}$ (V)(3) | $V_{OH}$ (V)(4) | $I_{OL}$ | $I_{OH}$ |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Max | Min | mA | mA |
| DIFF_HSTL_I | 0.300 | 0.750 | 1.125 | 0.100 | – | 0.400 | $V_{CCO}$ – 0.400 | 8.0 | –8.0 |
| DIFF_HSTL_I_18 | 0.300 | 0.900 | 1.425 | 0.100 | – | 0.400 | $V_{CCO}$ – 0.400 | 8.0 | –8.0 |
| DIFF_HSUL_12 | 0.300 | 0.600 | 0.850 | 0.100 | – | 20% $V_{CCO}$ | 80% $V_{CCO}$ | 0.1 | –0.1 |
| DIFF_SSTL12 | 0.300 | 0.600 | 0.850 | 0.100 | – | ($V_{CCO}$/2) – 0.150 | ($V_{CCO}$/2) + 0.150 | 14.25 | –14.25 |
| DIFF_SSTL135 | 0.300 | 0.675 | 1.000 | 0.100 | – | ($V_{CCO}$/2) – 0.150 | ($V_{CCO}$/2) + 0.150 | 8.9 | –8.9 |
| DIFF_SSTL135_II | 0.300 | 0.675 | 1.000 | 0.100 | – | ($V_{CCO}$/2) – 0.150 | ($V_{CCO}$/2) + 0.150 | 13.0 | –13.0 |
| DIFF_SSTL15 | 0.300 | 0.750 | 1.125 | 0.100 | – | ($V_{CCO}$/2) – 0.175 | ($V_{CCO}$/2) + 0.175 | 8.9 | –8.9 |
| DIFF_SSTL15_II | 0.300 | 0.750 | 1.125 | 0.100 | – | ($V_{CCO}$/2) – 0.175 | ($V_{CCO}$/2) + 0.175 | 13.0 | –13.0 |
| DIFF_SSTL18_I | 0.300 | 0.900 | 1.425 | 0.100 | – | ($V_{CCO}$/2) – 0.470 | ($V_{CCO}$/2) + 0.470 | 8.0 | –8.0 |
| DIFF_SSTL18_II | 0.300 | 0.900 | 1.425 | 0.100 | – | ($V_{CCO}$/2) – 0.600 | ($V_{CCO}$/2) + 0.600 | 13.4 | –13.4 |

**Notes:**

1. $V_{ICM}$ is the input common mode voltage.
2. $V_{ID}$ is the input differential voltage.
3. $V_{OL}$ is the single-ended low-output voltage.
4. $V_{OH}$ is the single-ended high-output voltage.

# LVDS DC Specifications (LVDS_25)

The LVDS_25 standard is available in the HD I/O banks. See the *UltraScale Architecture SelectIO Resources User Guide* (UG571) for more information.

*Table 18:* **LVDS_25 DC Specifications**

| Symbol | DC Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CCO}$(1) | Supply voltage. | | 2.375 | 2.500 | 2.625 | V |
| $V_{IDIFF}$ | Differential input voltage:<br>($\underline{Q}$ – $\overline{Q}$), $\underline{Q}$ = High<br>($\overline{Q}$ – $\underline{Q}$), $\overline{Q}$ = High | | 100 | 350 | 600(2) | mV |
| $V_{ICM}$ | Input common-mode voltage. | | 0.300 | 1.200 | 1.425 | V |

**Notes:**

1. LVDS_25 in HD I/O banks supports inputs only. LVDS_25 inputs without internal termination have no $V_{CCO}$ requirements. Any $V_{CCO}$ can be chosen as long as the input voltage levels do not violate the *Recommended Operating Condition* (Table 2) specification for the $V_{IN}$ I/O pin voltage.
2. Maximum $V_{IDIFF}$ value is specified for the maximum $V_{ICM}$ specification. With a lower $V_{ICM}$, a higher $V_{DIFF}$ is tolerated only when the recommended operating conditions and overshoot/undershoot $V_{IN}$ specifications are maintained.

# LVDS DC Specifications (LVDS)

The LVDS standard is available in the HP I/O banks. See the *UltraScale Architecture SelectIO Resources User Guide* (UG571) for more information.

*Table 19:* **LVDS DC Specifications**

| Symbol | DC Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CCO}$(1) | Supply voltage. | | 1.710 | 1.800 | 1.890 | V |
| $V_{ODIFF}$(2) | Differential output voltage:<br>($\underline{Q}$ – $\overline{Q}$), $\underline{Q}$ = High<br>($\overline{Q}$ – $\underline{Q}$), $\overline{Q}$ = High | $R_T$ = 100Ω across Q and $\overline{Q}$ signals | 247 | 350 | 454 | mV |
| $V_{OCM}$(2) | Output common-mode voltage. | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 1.000 | 1.250 | 1.425 | V |
| $V_{IDIFF}$(3) | Differential input voltage:<br>($\underline{Q}$ – $\overline{Q}$), $\underline{Q}$ = High<br>($\overline{Q}$ – $\underline{Q}$), $\overline{Q}$ = High | | 100 | 350 | 600(3) | mV |
| $V_{ICM\_DC}$(4) | Input common-mode voltage (DC coupling). | | 0.300 | 1.200 | 1.425 | V |
| $V_{ICM\_AC}$(5) | Input common-mode voltage (AC coupling). | | 0.600 | – | 1.100 | V |

**Notes:**

1. In HP I/O banks, when LVDS is used with input-only functionality, it can be placed in a bank where the $V_{CCO}$ levels are different from the specified level only if internal differential termination is not used. In this scenario, $V_{CCO}$ must be chosen to ensure the input pin voltage levels do not violate the *Recommended Operating Condition* (Table 2) specification for the $V_{IN}$ I/O pin voltage.
2. $V_{OCM}$ and $V_{ODIFF}$ values are for LVDS_PRE_EMPHASIS = FALSE.
3. Maximum $V_{IDIFF}$ value is specified for the maximum $V_{ICM}$ specification. With a lower $V_{ICM}$, a higher $V_{DIFF}$ is tolerated only when the recommended operating conditions and overshoot/undershoot $V_{IN}$ specifications are maintained.
4. Input common mode voltage for DC coupled configurations. EQUALIZATION = EQ_NONE (Default).
5. External input common mode voltage specification for AC coupled configurations. EQUALIZATION = EQ_LEVEL0, EQ_LEVEL1, EQ_LEVEL2, EQ_LEVEL3, EQ_LEVEL4.

# AC Switching Characteristics

All values represented in this data sheet are based on the speed specifications in the Vivado® Design Suite as outlined in Table 20.

*Table 20:* **Speed Specification Version By Device**

| 2017.1 | Device |
|---|---|
| 1.08 | XCKU11P |
| 1.10 | XCKU3P, XCKU5P, XCKU9P, XCKU13P, and XCKU15P |

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

**Advance Product Specification**

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

**Preliminary Product Specification**

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

**Product Specification**

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to production before faster speed grades.

## Testing of AC Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. All AC switching characteristics are representative of worst-case supply voltage and junction temperature conditions.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Kintex UltraScale+ FPGAs.

*Table 27:* **Maximum Physical Interface (PHY) Rate for Memory Interfaces *(Cont'd)***

| Memory Standard | Package | DRAM Type | Speed Grade and $V_{CCINT}$ Operating Voltages | | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | 0.90V | 0.85V | | 0.72V | | |
| | | | -3 | -2 | -1 | -2 | -1 | |
| DDR3L | All FFV packages | Single rank component | 1866 | 1866 | 1866 | 1866 | 1600 | Mb/s |
| | | 1 rank DIMM(1)(2) | 1600 | 1600 | 1600 | 1600 | 1333 | Mb/s |
| | | 2 rank DIMM(1)(3) | 1333 | 1333 | 1333 | 1333 | 1066 | Mb/s |
| | | 4 rank DIMM(1)(5) | 800 | 800 | 800 | 800 | 606 | Mb/s |
| | SFVB784 | Single rank component | 1600 | 1600 | 1600 | 1600 | 1600 | Mb/s |
| | | 1 rank DIMM(1)(2) | 1600 | 1600 | 1600 | 1600 | 1333 | Mb/s |
| | | 2 rank DIMM(1)(4) | 1333 | 1333 | 1333 | 1333 | 1066 | Mb/s |
| | | 4 rank DIMM(1)(5) | 800 | 800 | 800 | 800 | 606 | Mb/s |
| QDR II+ | All | Single rank component(6) | 633 | 633 | 600 | 600 | 550 | MHz |
| RLDRAM 3 | All FFV packages | Single rank component | 1200 | 1200 | 1066 | 1066 | 933 | MHz |
| | SFVB784 | Single rank component | 1066 | 1066 | 933 | 933 | 800 | MHz |
| QDR IV XP | All | Single rank component | 1066 | 1066 | 1066 | 933 | 933 | MHz |
| LPDDR3 | All | Single rank component | 1600 | 1600 | 1600 | 1600 | 1600 | Mb/s |

**Notes:**

1. Dual in-line memory module (DIMM) includes RDIMM, SODIMM, UDIMM, and LRDIMM.
2. Includes: 1 rank 1 slot, DDP 2 rank, LRDIMM 2 or 4 rank 1 slot.
3. For the DDR4 DDP components at -3 and -2 speed grades and $V_{CCINT}$ = 0.85V, the maximum data rate is 2133 Mb/s for six or more DDP devices. For five or less DDP devices, use the single rank DIMM data rates for the -3 and -2 speed grades at 0.85V.
4. Includes: 2 rank 1 slot, 1 rank 2 slot, LRDIMM 2 rank 2 slot.
5. Includes: 2 rank 2 slot, 4 rank 1 slot.
6. The QDRII+ performance specifications are for burst-length 4 (BL = 4) implementations.

*Table 29:* **IOB High Performance (HP) Switching Characteristics *(Cont'd)***

| I/O Standards | $T_{INBUF\_DELAY\_PAD\_I}$ | | | | | $T_{OUTBUF\_DELAY\_O\_PAD}$ | | | | | $T_{OUTBUF\_DELAY\_TD\_PAD}$ | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0.90V | 0.85V | | 0.72V | | 0.90V | 0.85V | | 0.72V | | 0.90V | 0.85V | | 0.72V | | |
| | -3 | -2 | -1 | -2 | -1 | -3 | -2 | -1 | -2 | -1 | -3 | -2 | -1 | -2 | -1 | |
| HSTL_I_DCI_S | 0.393 | 0.393 | 0.415 | 0.393 | 0.415 | 0.766 | 0.766 | 0.821 | 0.766 | 0.821 | 0.847 | 0.847 | 0.912 | 0.847 | 0.912 | ns |
| HSTL_I_F | 0.378 | 0.378 | 0.399 | 0.378 | 0.399 | 0.423 | 0.423 | 0.443 | 0.423 | 0.443 | 0.549 | 0.549 | 0.581 | 0.549 | 0.581 | ns |
| HSTL_I_M | 0.378 | 0.378 | 0.399 | 0.378 | 0.399 | 0.554 | 0.554 | 0.585 | 0.554 | 0.585 | 0.640 | 0.640 | 0.677 | 0.640 | 0.677 | ns |
| HSTL_I_S | 0.378 | 0.378 | 0.399 | 0.378 | 0.399 | 0.766 | 0.766 | 0.816 | 0.766 | 0.816 | 0.811 | 0.811 | 0.866 | 0.811 | 0.866 | ns |
| HSUL_12_DCI_F | 0.378 | 0.378 | 0.399 | 0.378 | 0.399 | 0.425 | 0.425 | 0.443 | 0.425 | 0.443 | 0.558 | 0.558 | 0.586 | 0.558 | 0.586 | ns |
| HSUL_12_DCI_M | 0.378 | 0.378 | 0.399 | 0.378 | 0.399 | 0.556 | 0.556 | 0.586 | 0.556 | 0.586 | 0.654 | 0.654 | 0.694 | 0.654 | 0.694 | ns |
| HSUL_12_DCI_S | 0.378 | 0.378 | 0.399 | 0.378 | 0.399 | 0.736 | 0.736 | 0.784 | 0.736 | 0.784 | 0.821 | 0.821 | 0.886 | 0.821 | 0.886 | ns |
| HSUL_12_F | 0.378 | 0.378 | 0.399 | 0.378 | 0.399 | 0.412 | 0.412 | 0.430 | 0.412 | 0.430 | 0.538 | 0.538 | 0.566 | 0.538 | 0.566 | ns |
| HSUL_12_M | 0.378 | 0.378 | 0.399 | 0.378 | 0.399 | 0.551 | 0.551 | 0.582 | 0.551 | 0.582 | 0.642 | 0.642 | 0.679 | 0.642 | 0.679 | ns |
| HSUL_12_S | 0.378 | 0.378 | 0.399 | 0.378 | 0.399 | 0.750 | 0.750 | 0.799 | 0.750 | 0.799 | 0.813 | 0.813 | 0.868 | 0.813 | 0.868 | ns |
| LVCMOS12_F_2 | 0.512 | 0.512 | 0.555 | 0.512 | 0.555 | 0.672 | 0.672 | 0.692 | 0.672 | 0.692 | 0.898 | 0.898 | 0.922 | 0.898 | 0.922 | ns |
| LVCMOS12_F_4 | 0.512 | 0.512 | 0.555 | 0.512 | 0.555 | 0.504 | 0.504 | 0.521 | 0.504 | 0.521 | 0.664 | 0.664 | 0.693 | 0.664 | 0.693 | ns |
| LVCMOS12_F_6 | 0.512 | 0.512 | 0.555 | 0.512 | 0.555 | 0.485 | 0.485 | 0.507 | 0.485 | 0.507 | 0.634 | 0.634 | 0.669 | 0.634 | 0.669 | ns |
| LVCMOS12_F_8 | 0.512 | 0.512 | 0.555 | 0.512 | 0.555 | 0.465 | 0.465 | 0.489 | 0.465 | 0.489 | 0.611 | 0.611 | 0.666 | 0.611 | 0.666 | ns |
| LVCMOS12_M_2 | 0.512 | 0.512 | 0.555 | 0.512 | 0.555 | 0.708 | 0.708 | 0.727 | 0.708 | 0.727 | 0.916 | 0.916 | 0.945 | 0.916 | 0.945 | ns |
| LVCMOS12_M_4 | 0.512 | 0.512 | 0.555 | 0.512 | 0.555 | 0.550 | 0.550 | 0.573 | 0.550 | 0.573 | 0.664 | 0.664 | 0.690 | 0.664 | 0.690 | ns |
| LVCMOS12_M_6 | 0.512 | 0.512 | 0.555 | 0.512 | 0.555 | 0.527 | 0.527 | 0.554 | 0.527 | 0.554 | 0.622 | 0.622 | 0.652 | 0.622 | 0.652 | ns |
| LVCMOS12_M_8 | 0.512 | 0.512 | 0.555 | 0.512 | 0.555 | 0.540 | 0.540 | 0.571 | 0.540 | 0.571 | 0.614 | 0.614 | 0.649 | 0.614 | 0.649 | ns |
| LVCMOS12_S_2 | 0.512 | 0.512 | 0.555 | 0.512 | 0.555 | 0.767 | 0.767 | 0.803 | 0.767 | 0.803 | 0.990 | 0.990 | 1.024 | 0.990 | 1.024 | ns |
| LVCMOS12_S_4 | 0.512 | 0.512 | 0.555 | 0.512 | 0.555 | 0.666 | 0.666 | 0.704 | 0.666 | 0.704 | 0.803 | 0.803 | 0.848 | 0.803 | 0.848 | ns |
| LVCMOS12_S_6 | 0.512 | 0.512 | 0.555 | 0.512 | 0.555 | 0.657 | 0.657 | 0.695 | 0.657 | 0.695 | 0.732 | 0.732 | 0.774 | 0.732 | 0.774 | ns |
| LVCMOS12_S_8 | 0.512 | 0.512 | 0.555 | 0.512 | 0.555 | 0.708 | 0.708 | 0.761 | 0.708 | 0.761 | 0.745 | 0.745 | 0.790 | 0.745 | 0.790 | ns |
| LVCMOS15_F_12 | 0.414 | 0.414 | 0.445 | 0.414 | 0.445 | 0.500 | 0.500 | 0.522 | 0.500 | 0.522 | 0.647 | 0.647 | 0.682 | 0.647 | 0.682 | ns |
| LVCMOS15_F_2 | 0.414 | 0.414 | 0.445 | 0.414 | 0.445 | 0.702 | 0.702 | 0.722 | 0.702 | 0.722 | 0.919 | 0.919 | 0.940 | 0.919 | 0.940 | ns |
| LVCMOS15_F_4 | 0.414 | 0.414 | 0.445 | 0.414 | 0.445 | 0.579 | 0.579 | 0.601 | 0.579 | 0.601 | 0.755 | 0.755 | 0.781 | 0.755 | 0.781 | ns |
| LVCMOS15_F_6 | 0.414 | 0.414 | 0.445 | 0.414 | 0.445 | 0.547 | 0.547 | 0.569 | 0.547 | 0.569 | 0.711 | 0.711 | 0.742 | 0.711 | 0.742 | ns |
| LVCMOS15_F_8 | 0.414 | 0.414 | 0.445 | 0.414 | 0.445 | 0.518 | 0.518 | 0.538 | 0.518 | 0.538 | 0.686 | 0.686 | 0.703 | 0.686 | 0.703 | ns |
| LVCMOS15_M_12 | 0.414 | 0.414 | 0.445 | 0.414 | 0.445 | 0.607 | 0.607 | 0.644 | 0.607 | 0.644 | 0.637 | 0.637 | 0.676 | 0.637 | 0.676 | ns |
| LVCMOS15_M_2 | 0.414 | 0.414 | 0.445 | 0.414 | 0.445 | 0.741 | 0.741 | 0.770 | 0.741 | 0.770 | 0.938 | 0.938 | 0.962 | 0.938 | 0.962 | ns |
| LVCMOS15_M_4 | 0.414 | 0.414 | 0.445 | 0.414 | 0.445 | 0.625 | 0.625 | 0.651 | 0.625 | 0.651 | 0.754 | 0.754 | 0.786 | 0.754 | 0.786 | ns |
| LVCMOS15_M_6 | 0.414 | 0.414 | 0.445 | 0.414 | 0.445 | 0.576 | 0.576 | 0.604 | 0.576 | 0.604 | 0.674 | 0.674 | 0.710 | 0.674 | 0.710 | ns |
| LVCMOS15_M_8 | 0.414 | 0.414 | 0.445 | 0.414 | 0.445 | 0.568 | 0.568 | 0.601 | 0.568 | 0.601 | 0.639 | 0.639 | 0.681 | 0.639 | 0.681 | ns |
| LVCMOS15_S_12 | 0.414 | 0.414 | 0.445 | 0.414 | 0.445 | 0.788 | 0.788 | 0.855 | 0.788 | 0.855 | 0.695 | 0.695 | 0.733 | 0.695 | 0.733 | ns |
| LVCMOS15_S_2 | 0.414 | 0.414 | 0.445 | 0.414 | 0.445 | 0.829 | 0.829 | 0.864 | 0.829 | 0.864 | 1.039 | 1.039 | 1.079 | 1.039 | 1.079 | ns |
| LVCMOS15_S_4 | 0.414 | 0.414 | 0.445 | 0.414 | 0.445 | 0.687 | 0.687 | 0.725 | 0.687 | 0.725 | 0.813 | 0.813 | 0.851 | 0.813 | 0.851 | ns |
| LVCMOS15_S_6 | 0.414 | 0.414 | 0.445 | 0.414 | 0.445 | 0.671 | 0.671 | 0.710 | 0.671 | 0.710 | 0.726 | 0.726 | 0.763 | 0.726 | 0.763 | ns |
| LVCMOS15_S_8 | 0.414 | 0.414 | 0.445 | 0.414 | 0.445 | 0.704 | 0.704 | 0.755 | 0.704 | 0.755 | 0.721 | 0.721 | 0.758 | 0.721 | 0.758 | ns |
| LVCMOS18_F_12 | 0.418 | 0.418 | 0.445 | 0.418 | 0.445 | 0.573 | 0.573 | 0.601 | 0.573 | 0.601 | 0.731 | 0.731 | 0.769 | 0.731 | 0.769 | ns |
| LVCMOS18_F_2 | 0.418 | 0.418 | 0.445 | 0.418 | 0.445 | 0.739 | 0.739 | 0.760 | 0.739 | 0.760 | 0.945 | 0.945 | 0.971 | 0.945 | 0.971 | ns |
| LVCMOS18_F_4 | 0.418 | 0.418 | 0.445 | 0.418 | 0.445 | 0.609 | 0.609 | 0.630 | 0.609 | 0.630 | 0.778 | 0.778 | 0.802 | 0.778 | 0.802 | ns |
| LVCMOS18_F_6 | 0.418 | 0.418 | 0.445 | 0.418 | 0.445 | 0.603 | 0.603 | 0.633 | 0.603 | 0.633 | 0.781 | 0.781 | 0.808 | 0.781 | 0.808 | ns |

*Table 29:* **IOB High Performance (HP) Switching Characteristics *(Cont'd)***

| I/O Standards | $T_{INBUF\_DELAY\_PAD\_I}$ | | | | | $T_{OUTBUF\_DELAY\_O\_PAD}$ | | | | | $T_{OUTBUF\_DELAY\_TD\_PAD}$ | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0.90V | 0.85V | | 0.72V | | 0.90V | 0.85V | | 0.72V | | 0.90V | 0.85V | | 0.72V | | |
| | -3 | -2 | -1 | -2 | -1 | -3 | -2 | -1 | -2 | -1 | -3 | -2 | -1 | -2 | -1 | |
| LVCMOS18_F_8 | 0.418 | 0.418 | 0.445 | 0.418 | 0.445 | 0.573 | 0.573 | 0.600 | 0.573 | 0.600 | 0.733 | 0.733 | 0.767 | 0.733 | 0.767 | ns |
| LVCMOS18_M_12 | 0.418 | 0.418 | 0.445 | 0.418 | 0.445 | 0.640 | 0.640 | 0.678 | 0.640 | 0.678 | 0.670 | 0.670 | 0.709 | 0.670 | 0.709 | ns |
| LVCMOS18_M_2 | 0.418 | 0.418 | 0.445 | 0.418 | 0.445 | 0.798 | 0.798 | 0.822 | 0.798 | 0.822 | 0.991 | 0.991 | 1.016 | 0.991 | 1.016 | ns |
| LVCMOS18_M_4 | 0.418 | 0.418 | 0.445 | 0.418 | 0.445 | 0.664 | 0.664 | 0.693 | 0.664 | 0.693 | 0.798 | 0.798 | 0.836 | 0.798 | 0.836 | ns |
| LVCMOS18_M_6 | 0.418 | 0.418 | 0.445 | 0.418 | 0.445 | 0.629 | 0.629 | 0.663 | 0.629 | 0.663 | 0.735 | 0.735 | 0.775 | 0.735 | 0.775 | ns |
| LVCMOS18_M_8 | 0.418 | 0.418 | 0.445 | 0.418 | 0.445 | 0.626 | 0.626 | 0.661 | 0.626 | 0.661 | 0.705 | 0.705 | 0.746 | 0.705 | 0.746 | ns |
| LVCMOS18_S_12 | 0.418 | 0.418 | 0.445 | 0.418 | 0.445 | 0.795 | 0.795 | 0.861 | 0.795 | 0.861 | 0.683 | 0.683 | 0.721 | 0.683 | 0.721 | ns |
| LVCMOS18_S_2 | 0.418 | 0.418 | 0.445 | 0.418 | 0.445 | 0.862 | 0.862 | 0.897 | 0.862 | 0.897 | 1.076 | 1.076 | 1.098 | 1.076 | 1.098 | ns |
| LVCMOS18_S_4 | 0.418 | 0.418 | 0.445 | 0.418 | 0.445 | 0.716 | 0.716 | 0.758 | 0.716 | 0.758 | 0.829 | 0.829 | 0.872 | 0.829 | 0.872 | ns |
| LVCMOS18_S_6 | 0.418 | 0.418 | 0.445 | 0.418 | 0.445 | 0.682 | 0.682 | 0.724 | 0.682 | 0.724 | 0.724 | 0.724 | 0.762 | 0.724 | 0.762 | ns |
| LVCMOS18_S_8 | 0.418 | 0.418 | 0.445 | 0.418 | 0.445 | 0.707 | 0.707 | 0.760 | 0.707 | 0.760 | 0.709 | 0.709 | 0.745 | 0.709 | 0.745 | ns |
| LVDCI_15_F | 0.425 | 0.425 | 0.462 | 0.425 | 0.462 | 0.426 | 0.426 | 0.443 | 0.426 | 0.443 | 0.548 | 0.548 | 0.581 | 0.548 | 0.581 | ns |
| LVDCI_15_M | 0.425 | 0.425 | 0.462 | 0.425 | 0.462 | 0.553 | 0.553 | 0.582 | 0.553 | 0.582 | 0.645 | 0.645 | 0.685 | 0.645 | 0.685 | ns |
| LVDCI_15_S | 0.425 | 0.425 | 0.462 | 0.425 | 0.462 | 0.749 | 0.749 | 0.803 | 0.749 | 0.803 | 0.821 | 0.821 | 0.890 | 0.821 | 0.890 | ns |
| LVDCI_18_F | 0.414 | 0.414 | 0.447 | 0.414 | 0.447 | 0.441 | 0.441 | 0.459 | 0.441 | 0.459 | 0.560 | 0.560 | 0.589 | 0.560 | 0.589 | ns |
| LVDCI_18_M | 0.414 | 0.414 | 0.447 | 0.414 | 0.447 | 0.554 | 0.554 | 0.585 | 0.554 | 0.585 | 0.644 | 0.644 | 0.683 | 0.644 | 0.683 | ns |
| LVDCI_18_S | 0.414 | 0.414 | 0.447 | 0.414 | 0.447 | 0.760 | 0.760 | 0.818 | 0.760 | 0.818 | 0.837 | 0.837 | 0.899 | 0.837 | 0.899 | ns |
| LVDS | 0.539 | 0.539 | 0.620 | 0.539 | 0.620 | 0.626 | 0.626 | 0.662 | 0.626 | 0.662 | 960.447 | 960.447 | 960.447 | 960.447 | 960.447 | ns |
| MIPI_DPHY_DCI_HS | 0.386 | 0.386 | 0.415 | 0.386 | 0.415 | 0.502 | 0.502 | 0.522 | 0.502 | 0.522 | N/A | N/A | N/A | N/A | N/A | ns |
| MIPI_DPHY_DCI_LP | 8.438 | 8.438 | 8.792 | 8.438 | 8.792 | 0.914 | 0.914 | 0.937 | 0.914 | 0.937 | N/A | N/A | N/A | N/A | N/A | ns |
| POD10_DCI_F | 0.408 | 0.408 | 0.430 | 0.408 | 0.430 | 0.425 | 0.425 | 0.444 | 0.425 | 0.444 | 0.555 | 0.555 | 0.584 | 0.555 | 0.584 | ns |
| POD10_DCI_M | 0.408 | 0.408 | 0.430 | 0.408 | 0.430 | 0.542 | 0.542 | 0.571 | 0.542 | 0.571 | 0.640 | 0.640 | 0.681 | 0.640 | 0.681 | ns |
| POD10_DCI_S | 0.408 | 0.408 | 0.430 | 0.408 | 0.430 | 0.754 | 0.754 | 0.815 | 0.754 | 0.815 | 0.850 | 0.850 | 0.917 | 0.850 | 0.917 | ns |
| POD10_F | 0.407 | 0.407 | 0.430 | 0.407 | 0.430 | 0.438 | 0.438 | 0.459 | 0.438 | 0.459 | 0.569 | 0.569 | 0.601 | 0.569 | 0.601 | ns |
| POD10_M | 0.407 | 0.407 | 0.430 | 0.407 | 0.430 | 0.538 | 0.538 | 0.568 | 0.538 | 0.568 | 0.630 | 0.630 | 0.667 | 0.630 | 0.667 | ns |
| POD10_S | 0.407 | 0.407 | 0.430 | 0.407 | 0.430 | 0.766 | 0.766 | 0.821 | 0.766 | 0.821 | 0.836 | 0.836 | 0.894 | 0.836 | 0.894 | ns |
| POD12_DCI_F | 0.409 | 0.409 | 0.431 | 0.409 | 0.431 | 0.425 | 0.425 | 0.443 | 0.425 | 0.443 | 0.558 | 0.558 | 0.586 | 0.558 | 0.586 | ns |
| POD12_DCI_M | 0.409 | 0.409 | 0.431 | 0.409 | 0.431 | 0.543 | 0.543 | 0.572 | 0.543 | 0.572 | 0.638 | 0.638 | 0.678 | 0.638 | 0.678 | ns |
| POD12_DCI_S | 0.409 | 0.409 | 0.431 | 0.409 | 0.431 | 0.772 | 0.772 | 0.822 | 0.772 | 0.822 | 0.862 | 0.862 | 0.929 | 0.862 | 0.929 | ns |
| POD12_F | 0.409 | 0.409 | 0.431 | 0.409 | 0.431 | 0.455 | 0.455 | 0.476 | 0.455 | 0.476 | 0.595 | 0.595 | 0.626 | 0.595 | 0.626 | ns |
| POD12_M | 0.409 | 0.409 | 0.431 | 0.409 | 0.431 | 0.551 | 0.551 | 0.582 | 0.551 | 0.582 | 0.641 | 0.641 | 0.679 | 0.641 | 0.679 | ns |
| POD12_S | 0.409 | 0.409 | 0.431 | 0.409 | 0.431 | 0.767 | 0.767 | 0.817 | 0.767 | 0.817 | 0.832 | 0.832 | 0.889 | 0.832 | 0.889 | ns |
| SLVS_400_18 | 0.539 | 0.539 | 0.620 | 0.539 | 0.620 | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A | ns |
| SSTL12_DCI_F | 0.381 | 0.381 | 0.399 | 0.381 | 0.399 | 0.425 | 0.425 | 0.443 | 0.425 | 0.443 | 0.558 | 0.558 | 0.586 | 0.558 | 0.586 | ns |
| SSTL12_DCI_M | 0.381 | 0.381 | 0.399 | 0.381 | 0.399 | 0.557 | 0.557 | 0.587 | 0.557 | 0.587 | 0.654 | 0.654 | 0.694 | 0.654 | 0.694 | ns |
| SSTL12_DCI_S | 0.381 | 0.381 | 0.399 | 0.381 | 0.399 | 0.754 | 0.754 | 0.803 | 0.754 | 0.803 | 0.842 | 0.842 | 0.908 | 0.842 | 0.908 | ns |
| SSTL12_F | 0.403 | 0.403 | 0.403 | 0.403 | 0.403 | 0.412 | 0.412 | 0.430 | 0.412 | 0.430 | 0.538 | 0.538 | 0.566 | 0.538 | 0.566 | ns |
| SSTL12_M | 0.403 | 0.403 | 0.403 | 0.403 | 0.403 | 0.553 | 0.553 | 0.584 | 0.553 | 0.584 | 0.641 | 0.641 | 0.676 | 0.641 | 0.676 | ns |
| SSTL12_S | 0.403 | 0.403 | 0.403 | 0.403 | 0.403 | 0.758 | 0.758 | 0.808 | 0.758 | 0.808 | 0.823 | 0.823 | 0.879 | 0.823 | 0.879 | ns |
| SSTL135_DCI_F | 0.366 | 0.366 | 0.399 | 0.366 | 0.399 | 0.411 | 0.411 | 0.428 | 0.411 | 0.428 | 0.537 | 0.537 | 0.565 | 0.537 | 0.565 | ns |
| SSTL135_DCI_M | 0.366 | 0.366 | 0.399 | 0.366 | 0.399 | 0.551 | 0.551 | 0.582 | 0.551 | 0.582 | 0.645 | 0.645 | 0.685 | 0.645 | 0.685 | ns |

# Output Delay Measurement Methodology

Output delays are measured with short output traces. Standard termination was used for all testing. The propagation delay of the trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in Figure 1 and Figure 2.

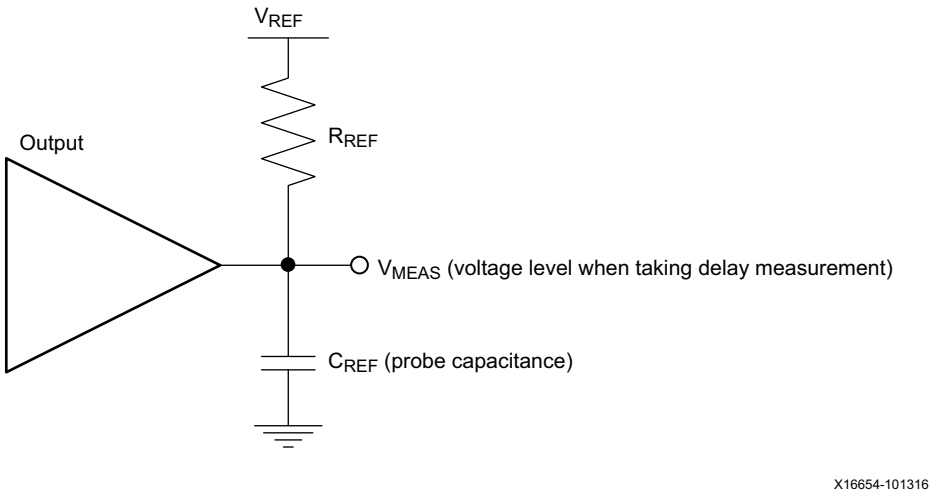


*Figure 1:* **Single-Ended Test Setup**

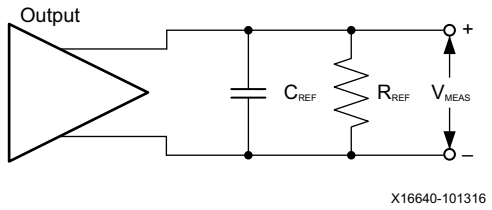


*Figure 2:* **Differential Test Setup**

Parameters $V_{REF}$, $R_{REF}$, $C_{REF}$, and $V_{MEAS}$ fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using this method:

1. Simulate the output driver of choice into the generalized test setup using values from Table 32.
2. Record the time to $V_{MEAS}$.
3. Simulate the output driver of choice into the actual PCB trace and load using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to $V_{MEAS}$.
5. Compare the results of step 2 and step 4. The increase or decrease in delay yields the actual propagation delay of the PCB trace.

# UltraRAM Switching Characteristics

The *UltraScale Architecture and Product Overview* (DS890) lists the Kintex UltraScale+ FPGAs that include this memory.

*Table 34:* **UltraRAM Switching Characteristics**

| Symbol | Description | Speed Grade and $V_{CCINT}$ Operating Voltages | | | | | Units |
|---|---|---|---|---|---|---|---|
| | | 0.90V | 0.85V | | 0.72V | | |
| | | -3 | -2 | -1 | -2 | -1 | |
| **Maximum Frequency** | | | | | | | |
| $F_{MAX}$ | UltraRAM maximum frequency with OREG_B = True. | 650 | 600 | 575 | 500 | 481 | MHz |
| $F_{MAX\_ECC}$ | UltraRAM maximum frequency with OREG_B = False and EN_ECC_RD_B = True. | 450 | 400 | 386 | 325 | 315 | MHz |
| $F_{MAX\_NORPIPELINE}$ | UltraRAM maximum frequency with OREG_B = False and EN_ECC_RD_B = False. | 550 | 500 | 478 | 425 | 408 | MHz |
| $T_{PW}$ (1) | Minimum pulse width. | 650 | 700 | 730 | 800 | 832 | ps |
| $T_{RSTPW}$ | Asynchronous reset minimum pulse width. One cycle required. | 1 clock cycle | | | | | |

**Notes:**

1. The MMCM and PLL DUTY_CYCLE attribute should be set to 50% to meet the pulse-width requirements at the higher frequencies.

# Input/Output Delay Switching Characteristics

*Table 35:* **Input/Output Delay Switching Characteristics**

| Symbol | Description | Speed Grade and $V_{CCINT}$ Operating Voltages | | | | | Units |
|---|---|---|---|---|---|---|---|
| | | 0.90V | 0.85V | | 0.72V | | |
| | | -3 | -2 | -1 | -2 | -1 | |
| $F_{REFCLK}$ | REFCLK frequency for IDELAYCTRL (component mode). | 300 to 800 | | | | | MHz |
| | REFCLK frequency for BITSLICE_CONTROL (native mode). | 300 to 2666.67 | 300 to 2666.67 | 300 to 2400 | 300 to 2400 | 300 to 2133 | MHz |
| $T_{MINPER\_CLK}$ | Minimum period for IODELAY clock. | 3.195 | 3.195 | 3.195 | 3.195 | 3.195 | ns |
| $T_{MINPER\_RST}$ | Minimum reset pulse width. | 52.00 | | | | | ns |
| $T_{IDELAY\_RESOLUTION}$/ $T_{ODELAY\_RESOLUTION}$ | IDELAY/ODELAY chain resolution. | 2.1 to 12 | | | | | ps |

**Notes:**

1. PLL settings could restrict the minimum allowable data rate. For example, when using a PLL with CLKOUTPHY = VCO_HALF, the minimum frequency is PLL_FVCOMIN/2.

# GTH Transceiver Specifications

The *UltraScale Architecture and Product Overview* (DS890) lists the Kintex UltraScale+ FPGAs that include the GTH transceivers.

## GTH Transceiver DC Input and Output Levels

Table 47 summarizes the DC specifications of the GTH transceivers in the Kintex UltraScale+ FPGAs. Consult the *UltraScale Architecture GTH Transceiver User Guide* (UG576) for further information.

*Table 47:* **GTH Transceiver DC Specifications**

| Symbol | DC Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $DV_{PPIN}$ | Differential peak-to-peak input voltage (external AC coupled). | >10.3125 Gb/s | 150 | – | 1250 | mV |
| | | 6.6 Gb/s to 10.3125 Gb/s | 150 | – | 1250 | mV |
| | | ≤ 6.6 Gb/s | 150 | – | 2000 | mV |
| $V_{IN}$ | Single-ended input voltage. Voltage measured at the pin referenced to GND. | DC coupled $V_{MGTAVTT}$ = 1.2V | –400 | – | $V_{MGTAVTT}$ | mV |
| $V_{CMIN}$ | Common mode input voltage. | DC coupled $V_{MGTAVTT}$ = 1.2V | – | 2/3 $V_{MGTAVTT}$ | – | mV |
| $D_{VPPOUT}$ | Differential peak-to-peak output voltage.(1) | Transmitter output swing is set to 11111 | 800 | – | – | mV |
| $V_{CMOUTDC}$ | Common mode output voltage: DC coupled (equation based). | When remote RX is terminated to GND | $V_{MGTAVTT}/2 - D_{VPPOUT}/4$ | | | mV |
| | | When remote RX termination is floating | $V_{MGTAVTT} - D_{VPPOUT}/2$ | | | mV |
| | | When remote RX is terminated to $V_{RX\_TERM}$(2) | $V_{MGTAVTT} - \frac{D_{VPPOUT}}{4} - \left(\frac{V_{MGTAVTT} - V_{RX\_TERM}}{2}\right)$ | | | mV |
| $V_{CMOUTAC}$ | Common mode output voltage: AC coupled (equation based). | | $V_{MGTAVTT} - D_{VPPOUT}/2$ | | | mV |
| $R_{IN}$ | Differential input resistance. | | – | 100 | – | Ω |
| $R_{OUT}$ | Differential output resistance. | | – | 100 | – | Ω |
| $T_{OSKEW}$ | Transmitter output pair (TXP and TXN) intra-pair skew (All packages). | | – | – | 10 | ps |
| $C_{EXT}$ | Recommended external AC coupling capacitor.(3) | | – | 100 | – | nF |

**Notes:**

1. The output swing and pre-emphasis levels are programmable using the attributes discussed in the *UltraScale Architecture GTH Transceiver User Guide* (UG576), and can result in values lower than reported in this table.
2. $V_{RX\_TERM}$ is the remote RX termination voltage.
3. Other values can be used as appropriate to conform to specific protocols and standards.

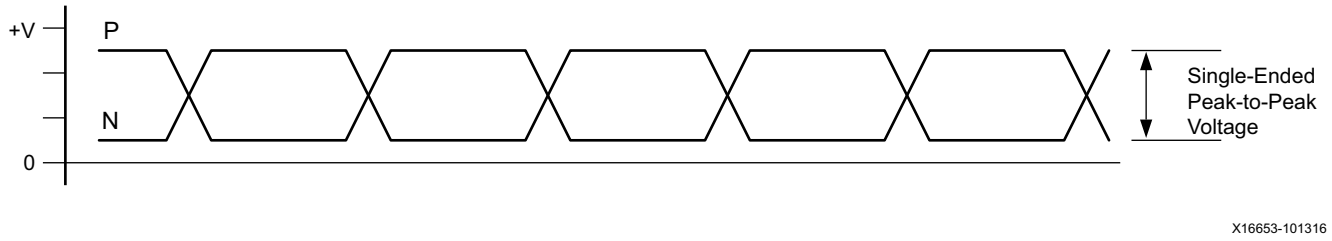


*Figure 3:* **Single-Ended Peak-to-Peak Voltage**

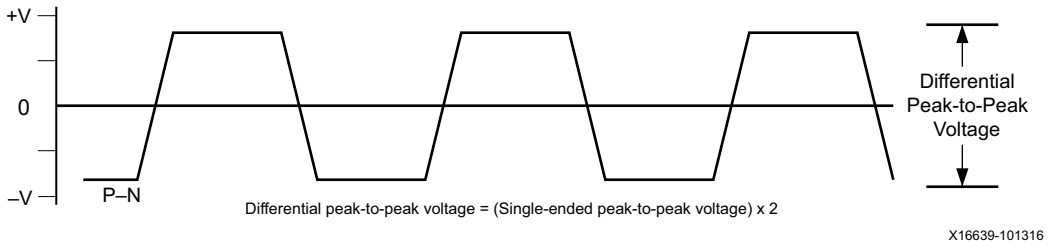


*Figure 4:* **Differential Peak-to-Peak Voltage**

Table 48 and Table 49 summarize the DC specifications of the GTH transceivers input and output clocks in Kintex UltraScale+ FPGAs. Consult the *UltraScale Architecture GTH Transceiver User Guide* (UG576) for further information.

*Table 48:* **GTH Transceiver Clock DC Input Level Specification**

| Symbol | DC Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $V_{IDIFF}$ | Differential peak-to-peak input voltage. | 250 | – | 2000 | mV |
| $R_{IN}$ | Differential input resistance. | – | 100 | – | Ω |
| $C_{EXT}$ | Required external AC coupling capacitor. | – | 10 | – | nF |

*Table 49:* **GTH Transceiver Clock Output Level Specification**

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{OL}$ | Output Low voltage for P and N. | $R_T$ = 100Ω across P and N signals | 100 | – | 330 | mV |
| $V_{OH}$ | Output High voltage for P and N. | $R_T$ = 100Ω across P and N signals | 500 | – | 700 | mV |
| $V_{DDOUT}$ | Differential output voltage.<br>(P–N), P = High<br>(N–P), N = High | $R_T$ = 100Ω across P and N signals | 300 | – | 430 | mV |
| $V_{CMOUT}$ | Common mode voltage. | $R_T$ = 100Ω across P and N signals | 300 | – | 500 | mV |

*Table 58:* **GTH Transceiver Protocol List**

| Protocol | Specification | Serial Rate (Gb/s) | Electrical Compliance |
|---|---|---|---|
| CAUI-10 | IEEE 802.3-2012 | 10.3125 | Compliant |
| nPPI | IEEE 802.3-2012 | 10.3125 | Compliant |
| 10GBASE-KR(1) | IEEE 802.3-2012 | 10.3125 | Compliant |
| 40GBASE-KR | IEEE 802.3-2012 | 10.3125 | Compliant |
| SFP+ | SFF-8431 (SR and LR) | 9.95328–11.10 | Compliant |
| XFP | INF-8077i, revision 4.5 | 10.3125 | Compliant |
| RXAUI | CEI-6G-SR | 6.25 | Compliant |
| XAUI | IEEE 802.3-2012 | 3.125 | Compliant |
| 1000BASE-X | IEEE 802.3-2012 | 1.25 | Compliant |
| 5.0G Ethernet | IEEE 802.3bx (PAR) | 5 | Compliant |
| 2.5G Ethernet | IEEE 802.3bx (PAR) | 2.5 | Compliant |
| HiGig, HiGig+, HiGig2 | IEEE 802.3-2012 | 3.74, 6.6 | Compliant |
| OTU2 | ITU G.8251 | 10.709225 | Compliant |
| OTU4 (OTL4.10) | OIF-CEI-11G-SR | 11.180997 | Compliant |
| OC-3/12/48/192 | GR-253-CORE | 0.1555–9.956 | Compliant |
| TFI-5 | OIF-TFI5-0.1.0 | 2.488 | Compliant |
| Interlaken | OIF-CEI-6G, OIF-CEI-11G-SR | 4.25–12.5 | Compliant |
| PCIe Gen1, 2, 3 | PCI Express base 3.0 | 2.5, 5.0, and 8.0 | Compliant |
| SDI(2) | SMPTE 424M-2006 | 0.27–2.97 | Compliant |
| UHD-SDI(2) | SMPTE ST-2081 6G, SMPTE ST-2082 12G | 6 and 12 | Compliant |
| Hybrid memory cube (HMC) | HMC-15G-SR | 10, 12.5, and 15.0 | Compliant |
| MoSys Bandwidth Engine | CEI-11-SR and CEI-11-SR (overclocked) | 10.3125, 15.5 | Compliant |
| CPRI | CPRI_v_6_1_2014-07-01 | 0.6144–12.165 | Compliant |
| HDMI(2) | HDMI 2.0 | All | Compliant |
| Passive optical network (PON) | 10G-EPON, 1G-EPON, NG-PON2, XG-PON, and 2.5G-PON | 0.155–10.3125 | Compliant |
| JESD204a/b | OIF-CEI-6G, OIF-CEI-11G | 3.125–12.5 | Compliant |
| Serial RapidIO | RapidIO specification 3.1 | 1.25–10.3125 | Compliant |
| DisplayPort(2) | DP 1.2B CTS | 1.62–5.4 | Compliant |
| Fibre channel | FC-PI-4 | 1.0625–14.025 | Compliant |
| SATA Gen1, 2, 3 | Serial ATA revision 3.0 specification | 1.5, 3.0, and 6.0 | Compliant |
| SAS Gen1, 2, 3 | T10/BSR INCITS 519 | 3.0, 6.0, and 12.0 | Compliant |
| SFI-5 | OIF-SFI5-01.0 | 0.625–12.5 | Compliant |
| Aurora | CEI-6G, CEI-11G-LR | up to 11.180997 | Compliant |

**Notes:**
1. The transition time of the transmitter is faster than the IEEE Std 802.3-2012 specification.
2. This protocol requires external circuitry to achieve compliance.

*Table 63:* **GTY Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics**

| Symbol | Description | All Speed Grades | Units |
|---|---|---|---|
| $F_{GTYDRPCLK}$ | GTYDRPCLK maximum frequency. | 250 | MHz |

*Table 64:* **GTY Transceiver Reference Clock Switching Characteristics**

| Symbol | Description | Conditions | All Speed Grades | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $F_{GCLK}$ | Reference clock frequency range. | | 60 | – | 820 | MHz |
| $T_{RCLK}$ | Reference clock rise time. | 20% – 80% | – | 200 | – | ps |
| $T_{FCLK}$ | Reference clock fall time. | 80% – 20% | – | 200 | – | ps |
| $T_{DCREF}$ | Reference clock duty cycle. | Transceiver PLL only | 40 | 50 | 60 | % |

*Table 65:* **GTY Transceiver Reference Clock Oscillator Selection Phase Noise Mask(1)**

| Symbol | Description | Offset Frequency | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $QPLL_{REFCLKMASK}$ | QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency = 156.25 MHz. | 10 kHz | – | – | –112 | dBc/Hz |
| | | 100 kHz | – | – | –128 | |
| | | 1 MHz | – | – | –145 | |
| | QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency = 312.5 MHz. | 10 kHz | – | – | –103 | dBc/Hz |
| | | 100 kHz | – | – | –123 | |
| | | 1 MHz | – | – | –143 | |
| | QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency =625 MHz. | 10 kHz | – | – | –98 | dBc/Hz |
| | | 100 kHz | – | – | –117 | |
| | | 1 MHz | – | – | –140 | |
| $CPLL_{REFCLKMASK}$ | CPLL reference clock select phase noise mask at REFCLK frequency = 156.25 MHz. | 10 kHz | – | – | –112 | dBc/Hz |
| | | 100 kHz | – | – | –128 | |
| | | 1 MHz | – | – | –145 | |
| | | 50 MHz | – | – | –145 | |
| | CPLL reference clock select phase noise mask at REFCLK frequency = 312.5 MHz. | 10 kHz | – | – | –103 | dBc/Hz |
| | | 100 kHz | – | – | –123 | |
| | | 1 MHz | – | – | –143 | |
| | | 50 MHz | – | – | –145 | |
| | CPLL reference clock select phase noise mask at REFCLK frequency = 625 MHz. | 10 kHz | – | – | –98 | dBc/Hz |
| | | 100 kHz | – | – | –117 | |
| | | 1 MHz | – | – | –140 | |
| | | 50 MHz | – | – | –144 | |

**Notes:**

1. For reference clock frequencies not in this table, use the phase-noise mask for the nearest reference clock frequency.

*Table 69:* **GTY Transceiver Receiver Switching Characteristics**

| Symbol | Description | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $F_{GTYRX}$ | Serial data rate | | 0.500 | – | $F_{GTYMAX}$ | Gb/s |
| $R_{XSST}$ | Receiver spread-spectrum tracking(1) | Modulated at 33 kHz | –5000 | – | 0 | ppm |
| $R_{XRL}$ | Run length (CID) | | – | – | 256 | UI |
| $R_{XPPMTOL}$ | Data/REFCLK PPM offset tolerance | Bit rates ≤ 6.6 Gb/s | –1250 | – | 1250 | ppm |
| | | Bit rates > 6.6 Gb/s and ≤ 8.0 Gb/s | –700 | – | 700 | ppm |
| | | Bit rates > 8.0 Gb/s | –200 | – | 200 | ppm |
| **SJ Jitter Tolerance(2)** | | | | | | |
| $J_{T\_SJ32.75}$ | Sinusoidal jitter (QPLL)(3) | 32.75 Gb/s | 0.30 | – | – | UI |
| $J_{T\_SJ28.21}$ | Sinusoidal jitter (QPLL)(3) | 28.21 Gb/s | 0.30 | – | – | UI |
| $J_{T\_SJ16.375}$ | Sinusoidal jitter (QPLL)(3) | 16.375 Gb/s | 0.30 | – | – | UI |
| $J_{T\_SJ15.0}$ | Sinusoidal jitter (QPLL)(3) | 15.0 Gb/s | 0.30 | – | – | UI |
| $J_{T\_SJ14.1}$ | Sinusoidal jitter (QPLL)(3) | 14.1 Gb/s | 0.30 | – | – | UI |
| $J_{T\_SJ13.1}$ | Sinusoidal jitter (QPLL)(3) | 13.1 Gb/s | 0.30 | – | – | UI |
| $J_{T\_SJ12.5}$ | Sinusoidal jitter (QPLL)(3) | 12.5 Gb/s | 0.30 | – | – | UI |
| $J_{T\_SJ11.3}$ | Sinusoidal jitter (QPLL)(3) | 11.3 Gb/s | 0.30 | – | – | UI |
| $J_{T\_SJ10.32\_QPLL}$ | Sinusoidal jitter (QPLL)(3) | 10.32 Gb/s | 0.30 | – | – | UI |
| $J_{T\_SJ10.32\_CPLL}$ | Sinusoidal jitter (CPLL)(3) | 10.32 Gb/s | 0.30 | – | – | UI |
| $J_{T\_SJ9.953\_QPLL}$ | Sinusoidal jitter (QPLL)(3) | 9.953 Gb/s | 0.30 | – | – | UI |
| $J_{T\_SJ9.953\_CPLL}$ | Sinusoidal jitter (CPLL)(3) | 9.953 Gb/s | 0.30 | – | – | UI |
| $J_{T\_SJ8.0}$ | Sinusoidal jitter (CPLL)(3) | 8.0 Gb/s | 0.42 | – | – | UI |
| $J_{T\_SJ6.6}$ | Sinusoidal jitter (CPLL)(3) | 6.6 Gb/s | 0.44 | – | – | UI |
| $J_{T\_SJ5.0}$ | Sinusoidal jitter (CPLL)(3) | 5.0 Gb/s | 0.44 | – | – | UI |
| $J_{T\_SJ4.25}$ | Sinusoidal jitter (CPLL)(3) | 4.25 Gb/s | 0.44 | – | – | UI |
| $J_{T\_SJ3.2}$ | Sinusoidal jitter (CPLL)(3) | 3.2 Gb/s(4) | 0.45 | – | – | UI |
| $J_{T\_SJ2.5}$ | Sinusoidal jitter (CPLL)(3) | 2.5 Gb/s(5) | 0.30 | – | – | UI |
| $J_{T\_SJ1.25}$ | Sinusoidal jitter (CPLL)(3) | 1.25 Gb/s(6) | 0.30 | – | – | UI |
| $J_{T\_SJ500}$ | Sinusoidal jitter (CPLL)(3) | 500 Mb/s(7) | 0.30 | – | – | UI |
| **SJ Jitter Tolerance with Stressed Eye(2)** | | | | | | |
| $J_{T\_TJSE3.2}$ | Total jitter with stressed eye(8) | 3.2 Gb/s | 0.70 | – | – | UI |
| $J_{T\_TJSE6.6}$ | | 6.6 Gb/s | 0.70 | – | – | UI |
| $J_{T\_SJSE3.2}$ | Sinusoidal jitter with stressed eye(8) | 3.2 Gb/s | 0.10 | – | – | UI |
| $J_{T\_SJSE6.6}$ | | 6.6 Gb/s | 0.10 | – | – | UI |

**Notes:**

1. Using RXOUT_DIV = 1, 2, and 4.
2. All jitter values are based on a bit error ratio of $10^{-12}$.
3. The frequency of the injected sinusoidal jitter is 80 MHz.
4. CPLL frequency at 3.2 GHz and RXOUT_DIV = 2.
5. CPLL frequency at 2.5 GHz and RXOUT_DIV = 2.
6. CPLL frequency at 2.5 GHz and RXOUT_DIV = 4.
7. CPLL frequency at 2.0 GHz and RXOUT_DIV = 8.
8. Composite jitter with RX equalizer enabled. DFE disabled.

# GTY Transceiver Electrical Compliance

The *UltraScale Architecture GTY Transceiver User Guide* (UG578) contains recommended use modes that ensure compliance for the protocols listed in Table 70. The transceiver wizard provides the recommended settings for those use cases and for protocol specific characteristics.

*Table 70:* **GTY Transceiver Protocol List**

| Protocol | Specification | Serial Rate (Gb/s) | Electrical Compliance |
|---|---|---|---|
| CAUI-4 | IEEE 802.3-2012 | 25.78125 | Compliant |
| 28 Gb/s backplane | CEI-25G-LR | 25–28.05 | Compliant |
| Interlaken | OIF-CEI-6G, OIF-CEI-11GSR, OIF-CEI-28G-MR | 4.25–25.78125 | Compliant |
| 100GBASE-KR4 | IEEE 802.3bj-2014, CEI-25G-LR | 25.78125 | Compliant(1) |
| 100GBASE-CR4 | IEEE 802.3bj-2014, CEI-25G-LR | 25.78125 | Compliant(1) |
| 50GBASE-KR4 | IEEE 802.3by-2014, CEI-25G-LR | 25.78125 | Compliant(1) |
| 50GBASE-CR4 | IEEE 802.3by-2014, CEI-25G-LR | 25.78125 | Compliant(1) |
| 25GBASE-KR4 | IEEE 802.3by-2014, CEI-25G-LR | 25.78125 | Compliant(1) |
| 25GBASE-CR4 | IEEE 802.3by-2014, CEI-25G-LR | 25.78125 | Compliant(1) |
| OTU4 (OTL4.4) CFP2 | OIF-CEI-28G-VSR | 27.952493-32.75 | Compliant |
| OTU4 (OTL4.4) CFP | OIF-CEI-11G-MR | 11.18–13.1 | Compliant |
| CAUI-10 | IEEE 802.3-2012 | 10.3125 | Compliant |
| nPPI | IEEE 802.3-2012 | 10.3125 | Compliant |
| 10GBASE-KR(2) | IEEE 802.3-2012 | 10.3125 | Compliant |
| SFP+ | SFF-8431 (SR and LR) | 9.95328–11.10 | Compliant |
| XFP | INF-8077i, revision 4.5 | 10.3125 | Compliant |
| RXAUI | CEI-6G-SR | 6.25 | Compliant |
| XAUI | IEEE 802.3-2012 | 3.125 | Compliant |
| 1000BASE-X | IEEE 802.3-2012 | 1.25 | Compliant |
| 5.0G Ethernet | IEEE 802.3bx (PAR) | 5 | Compliant |
| 2.5G Ethernet | IEEE 802.3bx (PAR) | 2.5 | Compliant |
| HiGig, HiGig+, HiGig2 | IEEE 802.3-2012 | 3.74, 6.6 | Compliant |
| QSGMII | QSGMII v1.2 (Cisco System, ENG-46158) | 5 | Compliant |
| OTU2 | ITU G.8251 | 10.709225 | Compliant |
| OTU4 (OTL4.10) | OIF-CEI-11G-SR | 11.180997 | Compliant |
| OC-3/12/48/192 | GR-253-CORE | 0.1555–9.956 | Compliant |
| PCIe Gen1, 2, 3 | PCI Express base 3.0 | 2.5, 5.0, and 8.0 | Compliant |
| SDI(3) | SMPTE 424M-2006 | 0.27–2.97 | Compliant |
| UHD-SDI(3) | SMPTE ST-2081 6G, SMPTE ST-2082 12G | 6 and 12 | Compliant |
| Hybrid memory cube (HMC) | HMC-15G-SR | 10, 12.5, and 15.0 | Compliant |
| MoSys bandwidth engine | CEI-11-SR and CEI-11-SR (overclocked) | 10.3125, 15.5 | Compliant |
| CPRI | CPRI_v_6_1_2014-07-01 | 0.6144–12.165 | Compliant |
| Passive optical network (PON) | 10G-EPON, 1G-EPON, NG-PON2, XG-PON, and 2.5G-PON | 0.155–10.3125 | Compliant |
| JESD204a/b | OIF-CEI-6G, OIF-CEI-11G | 3.125–12.5 | Compliant |

# Integrated Interface Block for Interlaken

More information and documentation on solutions using the integrated interface block for Interlaken can be found at UltraScale Interlaken. The *UltraScale Architecture and Product Overview* (DS890) lists how many blocks are in each Kintex UltraScale+ FPGA. This section describes the following Interlaken configurations.

- 12 x 12.5 Gb/s protocol and lane logic mode (Table 71).
- 6 x 25.78125 Gb/s and 6 x 28.21 Gb/s protocol and lane logic mode (Table 72).
- 12 x 25.78125 Gb/s lane logic only mode (Table 73).

Kintex UltraScale+ FPGAs in the SFVB784, FFVA676, and FFVA1156 packages are only supported using the 12 x 12.5 Gb/s Interlaken configuration. See Table 62 for the $F_{GTYMAX}$ description.

*Table 71:* **Maximum Performance for Interlaken 12 x 12.5 Gb/s Protocol and Lane Logic Mode Designs**

| Symbol | Description | Speed Grade and $V_{CCINT}$ Operating Voltages | | | | | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 0.90V | | 0.85V | | | | 0.72V | | | | |
| | | -3 | | -2 | | -1 | | -2 | | -1 | | |
| $F_{RX\_SERDES\_CLK}$ | Receive serializer/ deserializer clock | 195.32 | | 195.32 | | 195.32 | | 195.32 | | 195.32 | | MHz |
| $F_{TX\_SERDES\_CLK}$ | Transmit serializer/ deserializer clock | 195.32 | | 195.32 | | 195.32 | | 195.32 | | 195.32 | | MHz |
| $F_{DRP\_CLK}$ | Dynamic reconfiguration port clock | 250.00 | | 250.00 | | 250.00 | | 250.00 | | 250.00 | | MHz |
| | | Min(1) | Max | Min(1) | Max | Min(1) | Max | Min(1) | Max | Min(1) | Max | |
| $F_{CORE\_CLK}$ | Interlaken core clock | 300.00 | 322.27 | 300.00 | 322.27 | 300.00 | 322.27 | 300.00 | 322.27 | 300.00 | 322.27 | MHz |
| $F_{LBUS\_CLK}$ | Interlaken local bus clock | 300.00 | 322.27 | 300.00 | 322.27 | 300.00 | 322.27 | 300.00 | 322.27 | 300.00 | 322.27 | MHz |

**Notes:**

1. These are the minimum clock frequencies at the maximum lane performance.

*Table 72:* **Maximum Performance for Interlaken 6 x 25.78125 Gb/s and 6 x 28.21 Gb/s Protocol and Lane Logic Mode Designs**

| Symbol | Description | Speed Grade and $V_{CCINT}$ Operating Voltages | | | | | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 0.90V | | 0.85V | | | | 0.72V | | | | |
| | | -3(1) | | -2(1) | | -1 | | -2 | | -1 | | |
| | | Min(2) | Max | Min(2) | Max | Min | Max | Min(2) | Max | Min | Max | |
| $F_{RX\_SERDES\_CLK}$ | Receive serializer/ deserializer clock | 440.79 | | 440.79 | | N/A | | 402.84 | | N/A | | MHz |
| $F_{TX\_SERDES\_CLK}$ | Transmit serializer/ deserializer clock | 440.79 | | 440.79 | | N/A | | 402.84 | | N/A | | MHz |
| $F_{DRP\_CLK}$ | Dynamic reconfiguration port clock | 250.00 | | 250.00 | | N/A | | 250.00 | | N/A | | MHz |
| $F_{CORE\_CLK}$ | Interlaken core clock | 412.50(3) | 479.20 | 412.50(3) | 479.20 | N/A | | 412.50 | 429.69 | N/A | | MHz |
| $F_{LBUS\_CLK}$ | Interlaken local bus clock | 300.00(4) | 349.52 | 300.00(4) | 349.52 | N/A | | 300.00 | 349.52 | N/A | | MHz |

**Notes:**

1. 6 x 28.21 mode is only supported in the -2 ($V_{CCINT}$=0.85V) and -3 ($V_{CCINT}$=0.90V) speed grades.
2. These are the minimum clock frequencies at the maximum lane performance.
3. The minimum value for CORE_CLK is 451.36 MHz for the 6 x 28.21 Gb/s protocol.
4. The minimum value for LBUS_CLK is 330.00 MHz for the 6 x 28.21 Gb/s protocol.

*Table 73:* **Maximum Performance for Interlaken 12 x 25.78125 Gb/s Lane Logic Only Mode Designs**

| Symbol | Description | Speed Grade and $V_{CCINT}$ Operating Voltages | | | | | Units |
|---|---|---|---|---|---|---|---|
| | | 0.90V | 0.85V | | 0.72V | | |
| | | -3 | -2 | -1 | -2 | -1 | |
| $F_{RX\_SERDES\_CLK}$ | Receive serializer/ deserializer clock | 402.84 | 402.84 | N/A | N/A | N/A | MHz |
| $F_{TX\_SERDES\_CLK}$ | Transmit serializer/ deserializer clock | 402.84 | 402.84 | N/A | N/A | N/A | MHz |
| $F_{DRP\_CLK}$ | Dynamic reconfiguration port clock | 250.00 | 250.00 | N/A | N/A | N/A | MHz |
| $F_{CORE\_CLK}$ | Interlaken core clock | 412.50 | 412.50 | N/A | N/A | N/A | MHz |
| $F_{LBUS\_CLK}$ | Interlaken local bus clock | 349.52 | 349.52 | N/A | N/A | N/A | MHz |

# Integrated Interface Block for 100G Ethernet MAC and PCS

More information and documentation on solutions using the integrated 100 Gb/s Ethernet block can be found at UltraScale Integrated 100G Ethernet MAC/PCS. The *UltraScale Architecture and Product Overview* (DS890) lists how many blocks are in each Kintex UltraScale+ FPGA.

*Table 74:* **Maximum Performance for 100G Ethernet Designs**

| Symbol | Description | Speed Grade and $V_{CCINT}$ Operating Voltages | | | | | Units |
|---|---|---|---|---|---|---|---|
| | | 0.90V | 0.85V | | 0.72V | | |
| | | -3 | -2(1) | -1 | -2 | -1(2) | |
| $F_{TX\_CLK}$ | Transmit clock | 390.625 | 390.625 | 322.223 | 322.223 | 322.223 | MHz |
| $F_{RX\_CLK}$ | Receive clock | 390.625 | 390.625 | 322.223 | 322.223 | 322.223 | MHz |
| $F_{RX\_SERDES\_CLK}$ | Receive serializer/deserializer clock | 390.625 | 390.625 | 322.223 | 322.223 | 322.223 | MHz |
| $F_{DRP\_CLK}$ | Dynamic reconfiguration port clock | 250.00 | 250.00 | 250.00 | 250.00 | 250.00 | MHz |

**Notes:**
1. The maximum clock frequency of 390.625 MHz only applies to the CAUI-10 interface. The maximum clock frequency for the CAUI-4 interface is 322.223 MHz.
2. The CAUI-4 interface is not supported by -1L speed grade devices where $V_{CCINT}$=0.72V.

# Integrated Interface Block for PCI Express Designs

More information and documentation on solutions for PCI Express designs can be found at PCI Express. The *UltraScale Architecture and Product Overview* (DS890) lists how many blocks are in each Kintex UltraScale+ FPGA.

*Table 75:* **Maximum Performance for PCI Express Designs(1)(2)**

| Symbol | Description | Speed Grade and $V_{CCINT}$ Operating Voltages | | | | | Units |
|---|---|---|---|---|---|---|---|
| | | 0.90V | 0.85V | | 0.72V | | |
| | | -3 | -2 | -1 | -2 | -1 | |
| $F_{PIPECLK}$ | Pipe clock maximum frequency. | 250.00 | 250.00 | 250.00 | 250.00 | 250.00 | MHz |
| $F_{CORECLK}$ | Core clock maximum frequency. | 500.00 | 500.00 | 500.00 | 250.00 | 250.00 | MHz |
| $F_{DRPCLK}$ | DRP clock maximum frequency. | 250.00 | 250.00 | 250.00 | 250.00 | 250.00 | MHz |
| $F_{MCAPCLK}$ | MCAP clock maximum frequency. | 125.00 | 125.00 | 125.00 | 125.00 | 125.00 | MHz |

**Notes:**
1. PCI Express Gen4 operation is supported for x1, x2, x4, and x8 widths.
2. PCI Express Gen4 operation is supported in -3E, -2E, and -2I speed grades.

*Table 79:* **Configuration Switching Characteristics *(Cont'd)***

| Symbol | Description | | Speed Grade and $V_{CCINT}$ Operating Voltages | | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | 0.90V | 0.85V | | 0.72V | | |
| | | | -3 | -2 | -1 | -2 | -1 | |
| **SelectMAP Mode Programming Switching** | | | | | | | | |
| $T_{SMDCCK}/T_{SMCCKD}$ | D[31:00] setup/hold. | XCKU3P, XCKU5P | 4.5/0 | 4.5/0 | 4.5/0 | 8.0/0 | 8.0/0 | ns, Min |
| | | All other devices | 3.5/0 | 3.5/0 | 3.5/0 | 4.5/0 | 4.5/0 | |
| $T_{SMCSCCK}/T_{SMCCKCS}$ | CSI_B setup/hold. | XCKU3P, XCKU5P | 4.5/0 | 4.5/0 | 4.5/0 | 7.0/0 | 7.0/0 | ns, Min |
| | | All other devices | 4.0/0 | 4.0/0 | 4.0/0 | 5.0/0 | 5.0/0 | |
| $T_{SMWCCK}/T_{SMCCKW}$ | RDWR_B setup/hold. | XCKU3P, XCKU5P | 10.0/0 | 10.0/0 | 10.0/0 | 17.0/0 | 17.0/0 | ns, Min |
| | | All other devices | 10.0/0 | 10.0/0 | 10.0/0 | 11.0/0 | 11.0/0 | |
| $T_{SMCKCSO}$ | CSO_B clock to out (330Ω pull-up resistor required). | XCKU3P, XCKU5P | 7.0 | 7.0 | 7.0 | 10.0 | 10.0 | ns, Max |
| | | All other devices | 7.0 | 7.0 | 7.0 | 7.0 | 7.0 | |
| $T_{SMCO}$ | D[31:00] clock to out in readback. | XCKU3P, XCKU5P | 8.0 | 8.0 | 8.0 | 10.0 | 10.0 | ns, Max |
| | | All other devices | 8.0 | 8.0 | 8.0 | 8.0 | 8.0 | |
| $F_{RBCCK}$ | Readback frequency. | XCKU3P, XCKU5P | 125 | 125 | 125 | 60 | 60 | MHz, Max |
| | | All other devices | 125 | 125 | 125 | 125 | 125 | |
| **Boundary-Scan Port Timing Specifications** | | | | | | | | |
| $T_{TAPTCK}/T_{TCKTAP}$ | TMS and TDI setup/hold. | | 3.0/ 2.0 | 3.0/ 2.0 | 3.0/ 2.0 | 3.0/ 2.0 | 3.0/ 2.0 | ns, Min |
| $T_{TCKTDO}$ | TCK falling edge to TDO output. | | 7.0 | 7.0 | 7.0 | 7.0 | 7.0 | ns, Max |
| $F_{TCK}$ | TCK frequency. | XCKU15P | 66 | 66 | 66 | 50 | 50 | MHz, Max |
| | | All other devices | 66 | 66 | 66 | 66 | 66 | |
| **BPI Master Flash Mode Programming Switching** | | | | | | | | |
| $T_{BPICCO}$ | A[28:00], RS[1:0], FCS_B, FOE_B, FWE_B, ADV_B clock to out. | | 10 | 10 | 10 | 10 | 10 | ns, Max |
| $T_{BPIDCC}/T_{BPICCD}$ | D[15:00] setup/hold. | XCKU3P, XCKU5P | 4.5/0 | 4.5/0 | 4.5/0 | 8.0/0 | 8.0/0 | ns, Min |
| | | All other devices | 3.5/0 | 3.5/0 | 3.5/0 | 4.5/0 | 4.5/0 | |
| **SPI Master Flash Mode Programming Switching** | | | | | | | | |
| $T_{SPIDCC}/T_{SPICCD}$ | D[03:00] setup/hold. | | 3.0/0 | 3.0/0 | 3.0/0 | 4.0/0 | 4.0/0 | ns, Min |
| $T_{SPIDCC}/T_{SPICCD}$ | D[07:04] setup/hold. | XCKU3P, XCKU5P | 4.5/0 | 4.5/0 | 4.5/0 | 8.0/0 | 8.0/0 | ns, Min |
| | | All other devices | 3.5/0 | 3.5/0 | 3.5/0 | 4.5/0 | 4.5/0 | |
| $T_{SPICCM}$ | MOSI clock to out. | | 8.0 | 8.0 | 8.0 | 8.0 | 8.0 | ns, Max |
| $T_{SPICCFC}$ | FCS_B clock to out. | | 8.0 | 8.0 | 8.0 | 8.0 | 8.0 | ns, Max |
| **DNA Port Switching** | | | | | | | | |
| $F_{DNACK}$ | DNA port frequency. | | 200 | 200 | 200 | 175 | 175 | MHz, Max |
| **STARTUPE3 Ports** | | | | | | | | |
| $T_{USRCCLKO}$ | STARTUPE3 USRCCLKO input port to CCLK pin output delay. | | 0.25/ 6.00 | 0.25/ 6.50 | 0.25/ 7.50 | 0.25/ 9.00 | 0.25/ 9.00 | ns, Min/Max |
| $T_{DO}$ | DO[3:0] ports to D03-D00 pins output delay. | | 0.25/ 6.70 | 0.25/ 7.70 | 0.25/ 8.40 | 0.25/ 10.00 | 0.25/ 10.00 | ns, Min/Max |
| $T_{DTS}$ | DTS[3:0] ports to D03-D00 pins 3-state delays. | | 0.25/ 6.70 | 0.25/ 7.70 | 0.25/ 8.40 | 0.25/ 10.00 | 0.25/ 10.00 | ns, Min/Max |