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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	EBI/EMI, I²C, MMC/SD/SDIO, SmartCard, SPI, SPIFI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	64
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	360K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc54005jbd100e

- Clock output function with divider.
- Frequency measurement unit for measuring the frequency of any on-chip or off-chip clock signal.

- Power control:
  - Programmable PMU (Power Management Unit) to minimize power consumption and to match requirements at different performance levels.
  - Reduced power modes: sleep, deep-sleep, and deep power-down.
  - Wake-up from deep-sleep modes due to activity on the USART, SPI, and I2C peripherals when operating as slaves.
  - Ultra-low power Micro-tick Timer, running from the Watchdog oscillator that can be used to wake up the device from low power modes.
  - Power-On Reset (POR).
  - Brown-Out Detect (BOD) with separate thresholds for interrupt and forced reset.
- Single power supply 1.71 V to 3.6 V.
- Power-On Reset (POR).
- Brown-Out Detect (BOD) with separate thresholds for interrupt and forced reset.
- JTAG boundary scan supported.
- 128 bit unique device serial number for identification.
- Operating temperature range −40 °C to +105 °C.
- Available in TFBGA180, TFBGA100, LQFP208, and LQFP100 packages.

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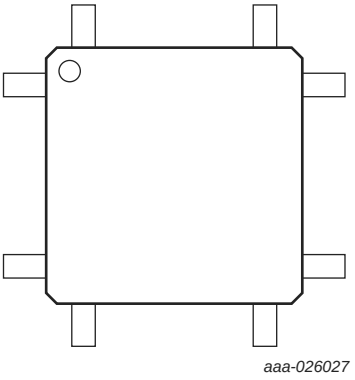

Fig 7. LQFP 208 Pin configuration

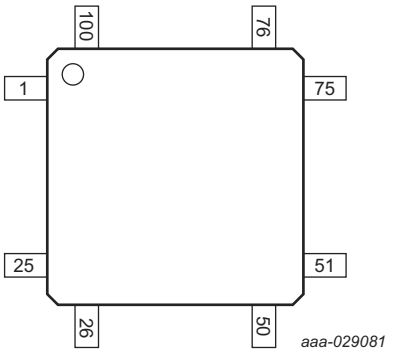

Fig 8. LQFP 100 Pin configuration

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Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state[1] [9]	Type	Description
PIO0_29	B7	B13	167	82	[2]	PU; Z	I/O	**PIO0_29 —** General-purpose digital input/output pin. **Remark:** In ISP mode, this pin is set to the Flexcomm 0 USART RXD function.
							I/O	**FC0_RXD_SDA_MOSI —** Flexcomm 0: USART receiver, I2C data I/O, SPI master-out/slave-in data.
								R — Reserved.
							O	**CT2_MAT3 —** Match output 3 from Timer 2.
							O	**SCT0_OUT8 —** SCTimer/PWM output 8.
							O	**TRACEDATA[2] —** Trace data bit 2.
PIO0_30	A2	A2	200	95	[2]	PU; Z	I/O	**PIO0_30 —** General-purpose digital input/output pin. **Remark:** In ISP mode, this pin is set to the Flexcomm 0 USART TXD function.
							I/O	**FC0_TXD_SCL_MISO —** Flexcomm 0: USART transmitter, I2C clock, SPI master-in/slave-out data.
								R — Reserved.
							O	**CT0_MAT0 —** Match output 0 from Timer 0.
							O	**SCT0_OUT9 —** SCTimer/PWM output 9.
							O	**TRACEDATA[1] —** Trace data bit 1.
PIO0_31/ ADC0_5	K3	M5	55	28	[4]	PU; Z	I/O; AI	**PIO0_31/ADC0_5 —** General-purpose digital input/output pin. ADC input channel 5 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
							I/O	**FC0_CTS_SDA_SSEL0 —** Flexcomm 0: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							I/O	**SD_D[2] —** SD/MMC data 2.
							O	**CT0_MAT1 —** Match output 1 from Timer 0.
							O	**SCT0_OUT3 —** SCTimer/PWM output 3.
							O	**TRACEDATA[0] —** Trace data bit 0.
PIO1_0/ ADC0_6	J3	N3	56	29	[4]	PU; Z	I/O; AI	**PIO1_0/ADC0_6 —** General-purpose digital input/output pin. ADC input channel 6 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
							I/O	**FC0_RTS_SCL_SSEL1 —** Flexcomm 0: USART request-to-send, I2C clock, SPI slave select 1.
							I/O	**SD_D[3] —** SD/MMC data 3.
							I	**CT0_CAP2 —** Capture 2 input to Timer 0.
							I	**SCT0_GPI4 —** Pin input 4 to SCTimer/PWM.
							O	**TRACECLK —** Trace clock.

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Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state[1] [9]	Type	Description
PIO2_0/ ADC0_7	-	P3	57	-	[4]	PU; Z	I/O; AI	**PIO2_0/ADC0_7 —** General-purpose digital input/output pin. ADC input channel 7 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
								R — Reserved.
							I/O	**FC0_RXD_SDA_MOSI —** Flexcomm 0: USART receiver, I2C data I/O, SPI master-out/slave-in data.
								R — Reserved.
							O	**CT1_CAP0 —** Capture input 0 to Timer 1.
PIO2_1/ ADC0_8	-	P4	58	-	[4]	PU; Z	I/O; AI	**PIO2_1/ADC0_8 —** General-purpose digital input/output pin. ADC input channel 8 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
								R — Reserved.
							I/O	**FC0_TXD_SCL_MISO —** Flexcomm 0: USART transmitter, I2C clock, SPI master-in/slave-out data.
								R — Reserved.
							O	**CT1_MAT0 —** Match output 0 from Timer 1.
PIO2_2	-	C3	4	-	[2]	PU; Z	I/O	**PIO2_2 —** General-purpose digital input/output pin.
							I	**ENET_CRS —** Ethernet Carrier Sense (MII interface) or Ethernet Carrier Sense/Data Valid (RMII interface).
							I/O	**FC3_SSEL3 —** Flexcomm 3: SPI slave select 3.
							O	**SCT0_OUT6 —** SCTimer/PWM output 6.
							O	**CT1_MAT1 —** Match output 1 from Timer 1.
PIO2_3	-	B1	7	-	[2]	PU; Z	I/O	**PIO2_3 —** General-purpose digital input/output pin.
							O	**ENET_TXD2 —** Ethernet transmit data 2 (MII interface).
							O	**SD_CLK —** SD/MMC clock.
							I/O	**FC1_RXD_SDA_MOSI —** Flexcomm 1: USART receiver, I2C data I/O, SPI master-out/slave-in data.
							O	**CT2_MAT0 —** Match output 0 from Timer 2.
PIO2_4	-	D3	9	-	[2]	PU; Z	I/O	**PIO2_4 —** General-purpose digital input/output pin.
							O	**ENET_TXD3 —** Ethernet transmit data 3 (MII interface).
							I/O	**SD_CMD —** SD/MMC card command I/O.
							I/O	**FC1_TXD_SCL_MISO —** Flexcomm 1: USART transmitter, I2C clock, SPI master-in/slave-out data.
							O	**CT2_MAT1 —** Match output 1 from Timer 2.

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Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state[1] [9]	Type	Description
PIO2_16	-	L8	81	-	[2][8]	PU; Z	I/O	**PIO2_16 —** General-purpose digital input/output pin.
							O	**LCD_LP —** LCD line synchronization pulse (STN). Horizontal synchronization pulse (TFT).
							O	**USB1_FRAME —** USB1 frame toggle signal.
							O	**USB1_PORTPWRN —** USB1 VBUS drive indicator (Indicates VBUS must be driven).
							O	**CT1_MAT3 —** Match output 3 from Timer 1.
							I/O	**FC8_SCK —** Flexcomm 8: USART or SPI clock.
PIO2_17	-	P10	86	-	[2]	PU; Z	I/O	**PIO2_17 —** General-purpose digital input/output pin.
							I	**LCD_CLKIN —** LCD clock input.
							O	**USB1_LEDN —** USB1-configured LED indicator (active low).
							I	**USB1_OVERCURRENTN —** USB1 bus overcurrent indicator (active low).
							I	**CT1_CAP1 —** Capture 1 input to Timer 1.
							I/O	**FC8_RXD_SDA_MOSI —** Flexcomm 8: USART receiver, I2C data I/O, SPI master-out/slave-in data.
PIO2_18	-	N10	90	-	[2]	PU; Z	I/O	**PIO2_18 —** General-purpose digital input/output pin.
							O	**LCD_VD[0] —** LCD Data [0].
							I/O	**FC3_RXD_SDA_MOSI —** Flexcomm 3: USART receiver, I2C data I/O, SPI master-out/slave-in data.
							I/O	**FC7_SCK —** Flexcomm 7: USART, SPI, or I2S clock.
							O	**CT3_MAT0 —** Match output 0 from Timer 3.
PIO2_19	-	P12	93	-	[2]	PU; Z	I/O	**PIO2_19 —** General-purpose digital input/output pin.
							O	**LCD_VD[1] —** LCD Data [1].
							I/O	**FC3_TXD_SCL_MISO —** Flexcomm 3: USART transmitter, I2C clock, SPI master-in/slave-out data.
							I/O	**FC7_RXD_SDA_MOSI_DATA —** Flexcomm 7: USART receiver, I2C data I/O, SPI master-out/slave-in data, I2S data I/O.
							O	**CT3_MAT1 —** Match output 1 from Timer 3.
PIO2_20	-	P13	95	-	[2]	PU; Z	I/O	**PIO2_20 —** General-purpose digital input/output pin.
							O	**LCD_VD[2] —** LCD Data [2].
							I/O	**FC3_RTS_SCL_SSEL1 —** Flexcomm 3: USART request-to-send, I2C clock, SPI slave select 1.
							I/O	**FC7_TXD_SCL_MISO_WS —** Flexcomm 7: USART transmitter, I2C clock, SPI master-in/slave-out data I/O, I2S word-select/frame.
							O	**CT3_MAT2 —** Match output 2 from Timer 3.
							I	**CT4_CAP0 —** Capture input 4 to Timer 0.

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Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state[1] [9]	Type	Description
PIO3_19	-	J3	44	-	[2]	PU; Z	I/O	**PIO3_19 —** General-purpose digital input/output pin.
							I/O	**FC8_RTS_SCL_SSEL1 —** Flexcomm 8: USART request-to-send, I2C clock, SPI slave select 1.
							I/O	**SD_D[7] —** SD/MMC data 7.
							O	**CT4_MAT1 —** Match output 1 from Timer 4.
							I	**CAN0_RD —** Receiver input for CAN 0.
							O	**SCT0_OUT6 —** SCTimer/PWM output 6.
PIO3_20	-	N2	46	-	[2]	PU; Z	I/O	**PIO3_20 —** General-purpose digital input/output pin.
							I/O	**FC9_SCK —** Flexcomm 9: USART or SPI clock.
							I	**SD_CARD_INT_N —**
							O	**CLKOUT —** Output of the CLKOUT function.
								R — Reserved.
							O	**SCT0_OUT7 —** SCTimer/PWM output 7.
PIO3_21/ ADC0_9	-	P5	61	-	[4]	PU; Z	I/O; AI	**PIO3_21/ADC0_9 —** General-purpose digital input/output pin. ADC input channel 9 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
							I/O	**FC9_RXD_SDA_MOSI —** Flexcomm 9: USART receiver, I2C data I/O, SPI master-out/slave-in data.
							O	**SD_BACKEND_PWR —** SD/MMC back-end power supply for embedded device.
							O	**CT4_MAT3 —** Match output 3 from Timer 4.
							I	**UTICK_CAP2 —** Micro-tick timer capture input 2.
PIO3_22/ ADC0_10	-	N5	62	-	[4]	PU; Z	I/O; AI	**PIO3_22/ADC0_10 —** General-purpose digital input/output pin. ADC input channel 10 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
							I/O	**FC9_TXD_SCL_MISO —** Flexcomm 9: USART transmitter, I2C clock, SPI master-in/slave-out data.
PIO3_23	-	C2	8	-	[3]	Z	I/O	**PIO3_23 —** General-purpose digital input/output pin.
							I/O	**FC2_CTS_SDA_SSEL0 —** Flexcomm 2: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
								R — Reserved.
							I	**UTICK_CAP3 —** Micro-tick timer capture input 3.
PIO3_24	-	E2	16	-	[3]	Z	I/O	**PIO3_24 —** General-purpose digital input/output pin.
							I/O	**FC2_RTS_SCL_SSEL1 —** Flexcomm 2: USART request-to-send, I2C clock, SPI slave select 1.
							I	**CT4_CAP0 —** Capture input 4 to Timer 0.
							I	**USB0_VBUS —** Monitors the presence of USB0 bus power.

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[1] PU = input mode, pull-up enabled (pull-up resistor pulls up pin to V_{DD}). Z = high impedance; pull-up or pull-down disabled, AI = analog input, I = input, O = output, F = floating. Reset state reflects the pin state at reset without boot code operation. For pin states in the different power modes, see Section 6.2.2 “Pin states in different power modes”. For termination on unused pins, see Section 6.2.1 “Termination of unused pins”.

[2] 5 V tolerant pad with programmable glitch filter (5 V tolerant if V_{DD} present; if V_{DD} not present, do not exceed 3.6 V); provides digital I/O functions with TTL levels and hysteresis; normal drive strength. See Figure 45. Pulse width of spikes or glitches suppressed by input filter is from 3 ns to 16 ns (simulated value).

[3] True open-drain pin. I2C-bus pins compliant with the I2C-bus specification for I2C standard mode, I2C Fast-mode, and I2C Fast-mode Plus. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I2C lines. Open-drain configuration applies to all functions on this pin.

[4] 5 V tolerant pin providing standard digital I/O functions with configurable modes, configurable hysteresis, and analog input. When configured as an analog input, the digital section of the pin is disabled, and the pin is not 5 V tolerant.

[5] Reset pad.5 V tolerant pad with glitch filter with hysteresis. Pulse width of spikes or glitches suppressed by input filter is from 3 ns to 20 ns (simulated value)

[6] 5 V tolerant transparent analog pad.

[7] The oscillator input pin (XTALIN) cannot be driven by an external clock. Must connect a crystal between XTALIN and XTALOUT.

[8] VBUS must be connected to supply voltage when using the USB peripheral.

[9] For initial device revision 0A (Boot ROM version 21.0), PU = input mode, pull-up enabled (pull-up resistor pulls up pin to VDD). For future device revision 1B (Boot ROM version 21.1), Z = high impedance; pull-up or pull-down disabled. See the Errata sheet LPC540xx (IOCON.1) for more details. For future device revision 1B (Boot ROM version 21.1), GPIO pins PIO0_12, PIO0_11, PIO0_2, PIO0_3, PIO0_4, PIO0_5, and PIO0_6 have the input buffer enabled (DIGIMODE, bit 8 is enabled in IOCON register) and will be floating by default. If unused, it is recommended to externally terminate this pins to prevent leakage.

6.2.1 Termination of unused pins

Table 5 shows how to terminate pins that are **not** used in the application. In many cases, unused pins should be connected externally or configured correctly by software to minimize the overall power consumption of the part.

Unused pins with GPIO function should be configured as outputs set to LOW with their internal pull-up disabled. To configure a GPIO pin as output and drive it LOW, select the GPIO function in the IOCON register, select output in the GPIO DIR register, and write a 0 to the GPIO PORT register for that pin. Disable the pull-up in the pin’s IOCON register.

In addition, it is recommended to configure all GPIO pins that are not bonded out on smaller packages as outputs driven LOW with their internal pull-up disabled.

Table 5. Termination of unused pins

Pin	Default state[1][2]	Recommended termination of unused pins
$\overline{\text{RESET}}$	I; PU	The $\overline{\text{RESET}}$ pin can be left unconnected if the application does not use it.
all PIOn_m (not open-drain)	I; PU; Z	Can be left unconnected if driven LOW and configured as GPIO output with pull-up disabled by software.
PIOn_m (I2C open-drain)	IA	Can be left unconnected if driven LOW and configured as GPIO output by software.
RTCXIN	-	Connect to ground. When grounded, the RTC oscillator is disabled.
RTCXOUT	-	Can be left unconnected.
XTALIN	-	Connect to ground. When grounded, the RTC oscillator is disabled.
XTALOUT	-	Can be left unconnected.
VREFP	-	Tie to VDD.
VREFN	-	Tie to VSS.
VDDA	-	Tie to VDD.
VSSA	-	Tie to VSS.

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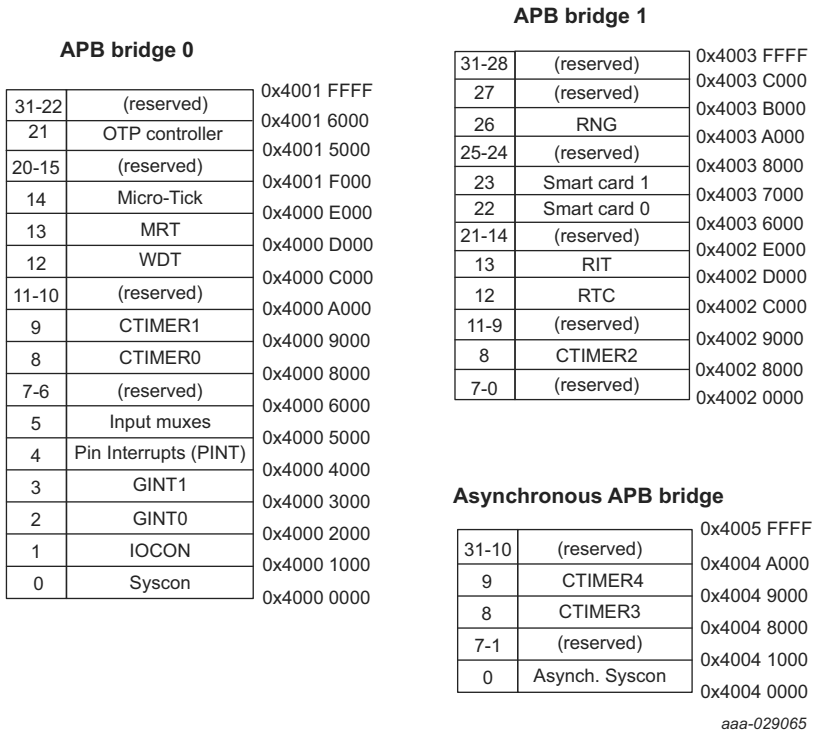

Fig 10. LPC540xx APB Memory map

7.10 System control

7.10.1 Clock sources

The LPC540xx supports one external and two internal clock sources:

- Free Running Oscillator (FRO).
- Watchdog oscillator (WDOSC).
- Crystal oscillator.

7.10.1.1 Free Running Oscillator (FRO)

The FRO 12 MHz oscillator provides the default clock at reset and provides a clean system clock shortly after the supply pins reach operating voltage.

- 12 MHz internal FRO oscillator, factory trimmed for accuracy, that can optionally be used as a system clock as well as other purposes.
- Selectable 48 MHz or 96 MHz FRO oscillator, factory trimmed for accuracy, that can optionally be used as a system clock as well as other purposes.

7.10.1.2 Watchdog oscillator (WDOSC)

The watchdog oscillator is a low-power internal oscillator. The WDOSC can be used to provide a clock to the WWDT and to the entire chip. The low-power watchdog oscillator provides a selectable frequency in the range of 6 kHz to 1.5 MHz. The accuracy of this clock is limited to ± 40% over temperature, voltage, and silicon processing variations.

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7.10.5 Clock Generation

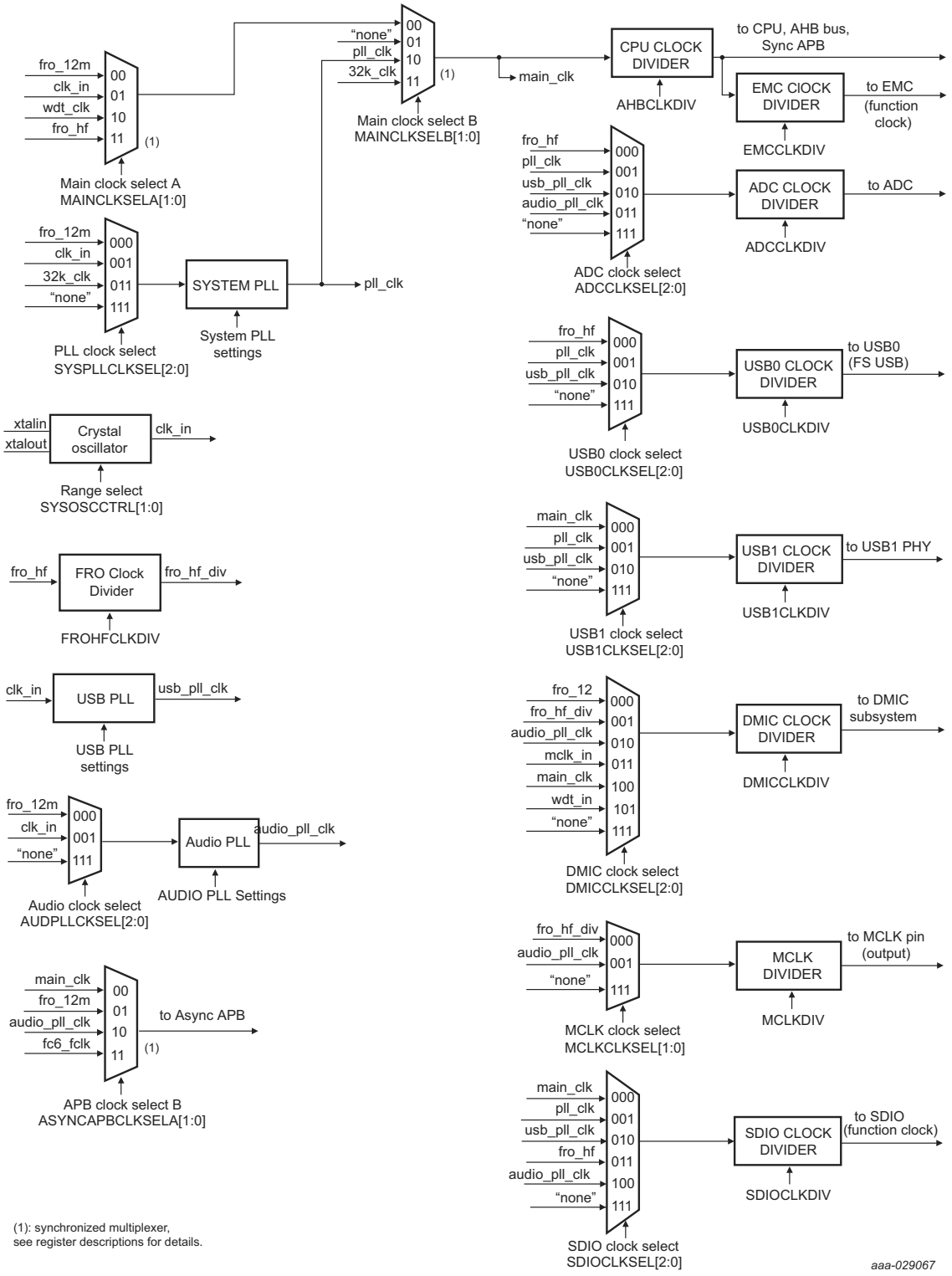

Fig 11. LPC540xx clock generation

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- Toggle on match.
- Do nothing on match.

- Up to two match registers can be used to generate timed DMA requests.
- The timer and prescaler may be configured to be cleared on a designated capture event. This feature permits easy pulse width measurement by clearing the timer on the leading edge of an input pulse and capturing the timer value on the trailing edge.
- Up to four match registers can be configured for PWM operation, allowing up to three single edged controlled PWM outputs. (The number of match outputs for each timer that are actually available on device pins may vary by device.)

7.16.2 SCTimer/PWM

The SCTimer/PWM allows a wide variety of timing, counting, output modulation, and input capture operations. The inputs and outputs of the SCTimer/PWM are shared with the capture and match inputs/outputs of the 32-bit general-purpose counter/timers.

The SCTimer/PWM can be configured as two 16-bit counters or a unified 32-bit counter. In the two-counter case, in addition to the counter value the following operational elements are independent for each half:

- State variable.
- Limit, halt, stop, and start conditions.
- Values of Match/Capture registers, plus reload or capture control values.

In the two-counter case, the following operational elements are global to the SCTimer/PWM, but the last three can use match conditions from either counter:

- Clock selection
- Inputs
- Events
- Outputs
- Interrupts

7.16.2.1 Features

- Two 16-bit counters or one 32-bit counter.
- Counter(s) clocked by bus clock or selected input.
- Up counter(s) or up-down counter(s).
- State variable allows sequencing across multiple counter cycles.
- Event combines input or output condition and/or counter match in a specified state.
- Events control outputs, interrupts, and the SCTimer/PWM states.
  - Match register 0 can be used as an automatic limit.
  - In bi-directional mode, events can be enabled based on the count direction.
  - Match events can be held until another qualifying event occurs.
- Selected event(s) can limit, halt, start, or stop a counter.
- Supports:

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Table 10. Limiting values *…continued*
In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
$P_{tot(pack)}$	total power dissipation (per package)	LQFP208, based on package heat transfer, not device power consumption	[11]	-	1.2	W
		LQFP208, based on package heat transfer, not device power consumption	[12]	-	0.95	W
		LQFP100, based on package heat transfer, not device power consumption	[11]	-	0.82	W
		LQFP100, based on package heat transfer, not device power consumption	[12]	-	0.60	W
		TFBGA180, based on package heat transfer, not device power consumption	[11]	-	0.95	W
		TFBGA180, based on package heat transfer, not device power consumption	[13]	-	1.2	W
		TFBGA100, based on package heat transfer, not device power consumption	[11]	-	0.57	W
		TFBGA100, based on package heat transfer, not device power consumption	[13]	-	0.65	W
V_{ESD}	electrostatic discharge voltage	human body model; all pins	[4]	-	2000	V

[1] The following applies to the limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

c) The limiting values are stress ratings only and operating the part at these values is not recommended and proper operation is not guaranteed. The conditions for functional operation are specified in Table 20.

[2] Maximum/minimum voltage above the maximum operating voltage (see Table 20) and below ground that can be applied for a short time (< 10 ms) to a device without leading to irrecoverable failure. Failure includes the loss of reliability and shorter lifetime of the device.

[3] The peak current is limited to 25 times the corresponding maximum current.

[4] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

[5] V_{DD} present or not present. Compliant with the I^2C-bus standard. 5.5 V can be applied to this pin when V_{DD} is powered down.

[6] Applies to all 5 V tolerant I/O pins except true open-drain pins.

[7] Including the voltage on outputs in 3-state mode.

[8] An ADC input voltage above 3.6 V can be applied for a short time without leading to immediate, unrecoverable failure. Accumulated exposure to elevated voltages at 4.6 V must be less than 10^6 s total over the lifetime of the device. Applying an elevated voltage to the ADC inputs for a long time affects the reliability of the device and reduces its lifetime.

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[9] It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin.

[10] Dependent on package type.

[11] JEDEC (4.5 in × 4 in); still air.

[12] Single layer (4.5 in × 3 in); still air.

[13] 8-layer (4.5 in × 3 in); still air.

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Table 16. Static characteristics: Power consumption in deep-sleep and deep power-down modes

T_{amb} = −40 °C to +105 °C, unless otherwise specified, 2.2 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ[1][2]	Max[3]	Unit
I_{DD}	supply current	Deep-sleep mode:					
		SRAMX (64 KB) powered T_{amb} = 25 °C		-	55	175	μA
		SRAMX (64 KB) powered T_{amb} = 105 °C		-	-	2020	μA
		Deep power-down mode					
		RTC oscillator input grounded (RTC oscillator disabled) *T_{amb} = 25 °C*		-	891	1.6	μA
		RTC oscillator input grounded (RTC oscillator disabled) *T_{amb} = 105 °C*		-	-	42	μA
		RTC oscillator running with external crystal VDD = VDDA= VREFP = 3.3 V, VBAT = 3.0 V		-	660	-	nA

[1] Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C), VDD = 3.3 V.

[2] Characterized through bench measurements using typical samples.

[3] Tested in production, VDD = 3.6 V.

Table 17. Static characteristics: Power consumption in deep power-down mode

T_{amb} = −40 °C to +105 °C, unless otherwise specified, 2.7 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ[1][2]	Max	Unit
I_{BAT}	battery supply current	deep power-down mode; RTC oscillator running with external crystal					
		VDD = VDDA= VREFP = 3.3 V, VBAT = 3.0 V		-	0	-	nA
		VDD = VDDA= VREFP = 0 V or tied to ground, VBAT = 3.0 V		-	380[3]	-	nA

[1] Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C).

[2] Characterized through bench measurements using typical samples.

[3] If VBAT> VDD, the external reset pin must be floating to prevent high VBAT leakage.

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Table 19. Typical AHB/APB peripheral power consumption [3][4][5]

T_{amb} = 25 °C, V_{DD} = 3.3 V;

Peripheral		I_{DD} in uA/MHz	I_{DD} in uA/MHz	I_{DD} in uA/MHz	I_{DD} in uA/MHz
Flexcomm Interface 3 (USART, SPI, I²C)		1.4	1.4	1.4	1.6
Flexcomm Interface 4 (USART, SPI, I²C)		1.4	1.5	1.5	1.7
Flexcomm Interface 5 (USART, SPI, I²C)		1.7	1.7	1.7	1.9
Flexcomm Interface 6 (USART, SPI, I²C, I²S)		2.0	2.0	2.0	2.3
Flexcomm Interface 7 (USART, SPI, I²C, I²S)		1.6	1.6	1.6	1.9
Flexcomm Interface 8 (USART, SPI, I²C)		1.5	1.5	1.5	1.8
Flexcomm Interface 9 (USART, SPI, I²C)		1.5	1.5	1.5	1.8
Flexcomm Interface 10 (SPI)		1.5	1.5	1.5	1.8
Sync APB peripheral		**CPU: 12 MHz, sync APB bus: 12 MHz**	**CPU: 48 MHz, sync APB bus: 48 MHz**	**CPU: 96 MHz, sync APB bus: 96 MHz**	**CPU: 180 MHz, sync APB bus: 180 MHz**
INPUTMUX	[1]	0.83	0.85	0.86	1.0
IOCON	[1]	2.67	2.65	2.65	3.13
PINT		1.1	1.1	1.1	1.3
GINT0 and GINT1		1.33	1.35	1.34	1.52
WWDT		0.42	0.42	0.42	0.46
RTC		0.3	0.3	0.3	0.3
MRT		0.3	0.3	0.3	0.3
RIT		0.1	0.1	0.1	0.1
UTICK		0.2	0.2	0.2	0.2
CTimer0		0.8	0.8	0.8	0.9
CTimer1		0.8	0.9	0.9	1.0
CTimer2		0.83	0.85	0.88	0.99
Smart card0		2.5	2.5	2.5	2.8
Smart card1		2.5	2.5	2.5	2.8
RNG		1.4	1.4	1.4	1.5
OTP controller		4.0	4.0	4.0	4.5
SHA		1.2	1.2	1.2	1.3

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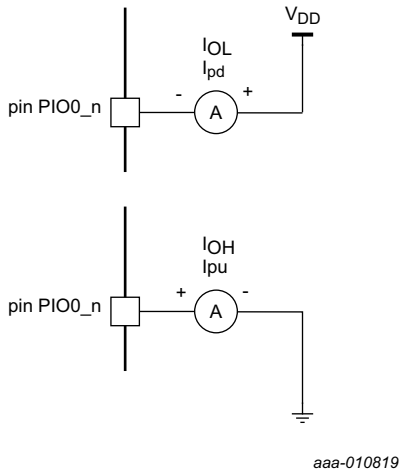
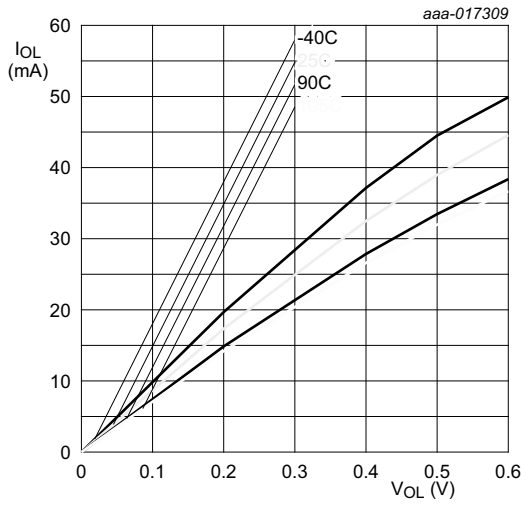
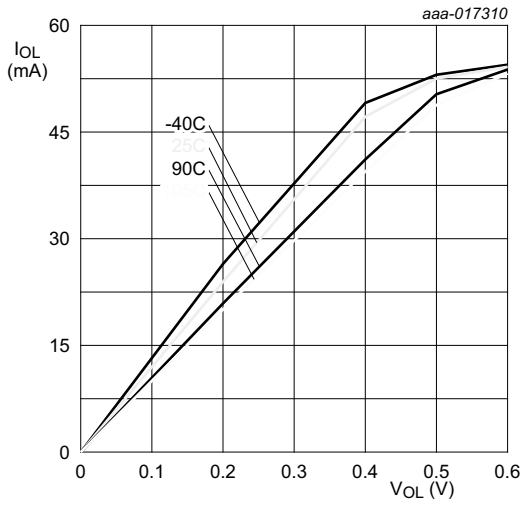


Fig 17. Pin input/output current measurement

10.4.1 Electrical pin characteristics



Conditions: V_{DD} = 1.8 V; on pins PIO0_13 to PIO0_14.



Conditions: V_{DD} = 3.3 V; on pins PIO0_13 to PIO0_16.

Fig 18. I^2C-bus pins (high current sink): Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}

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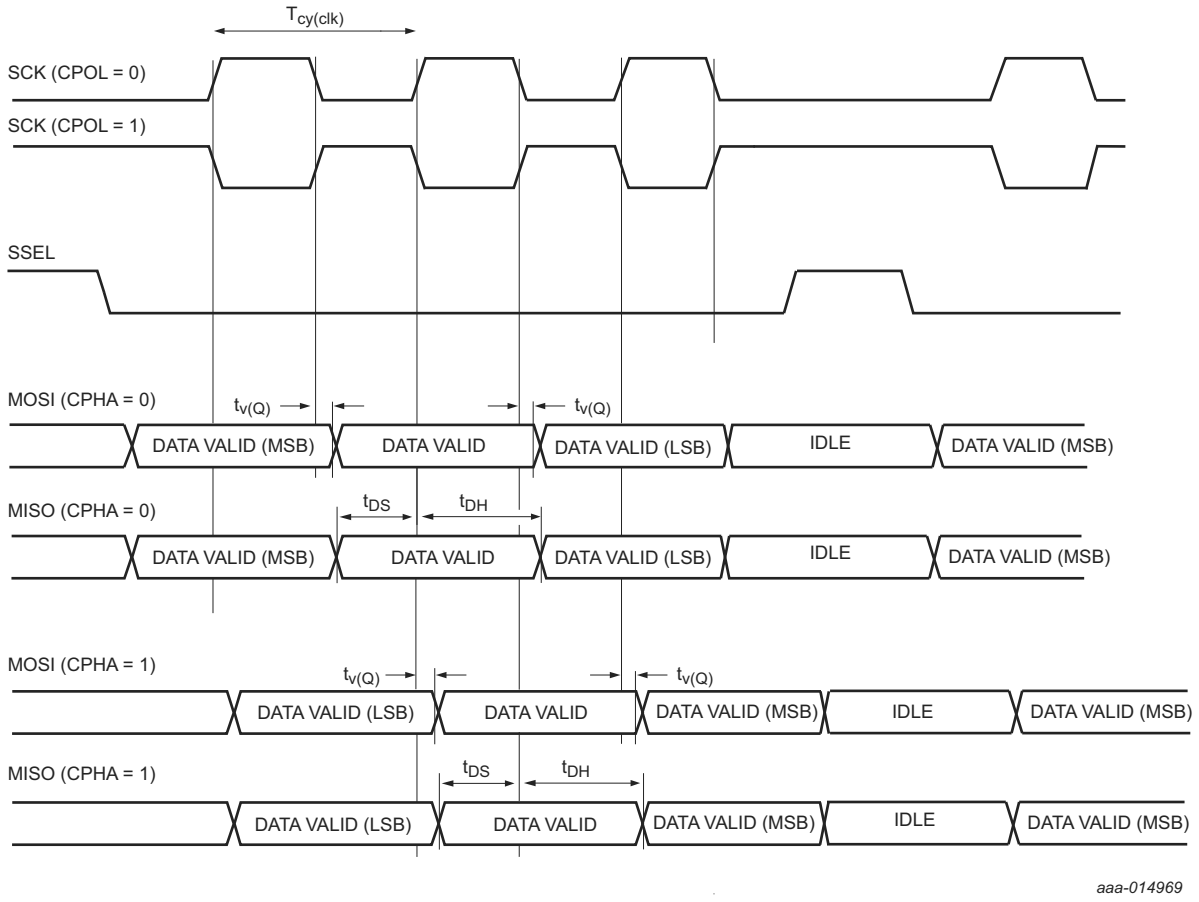

Fig 30. SPI master timing

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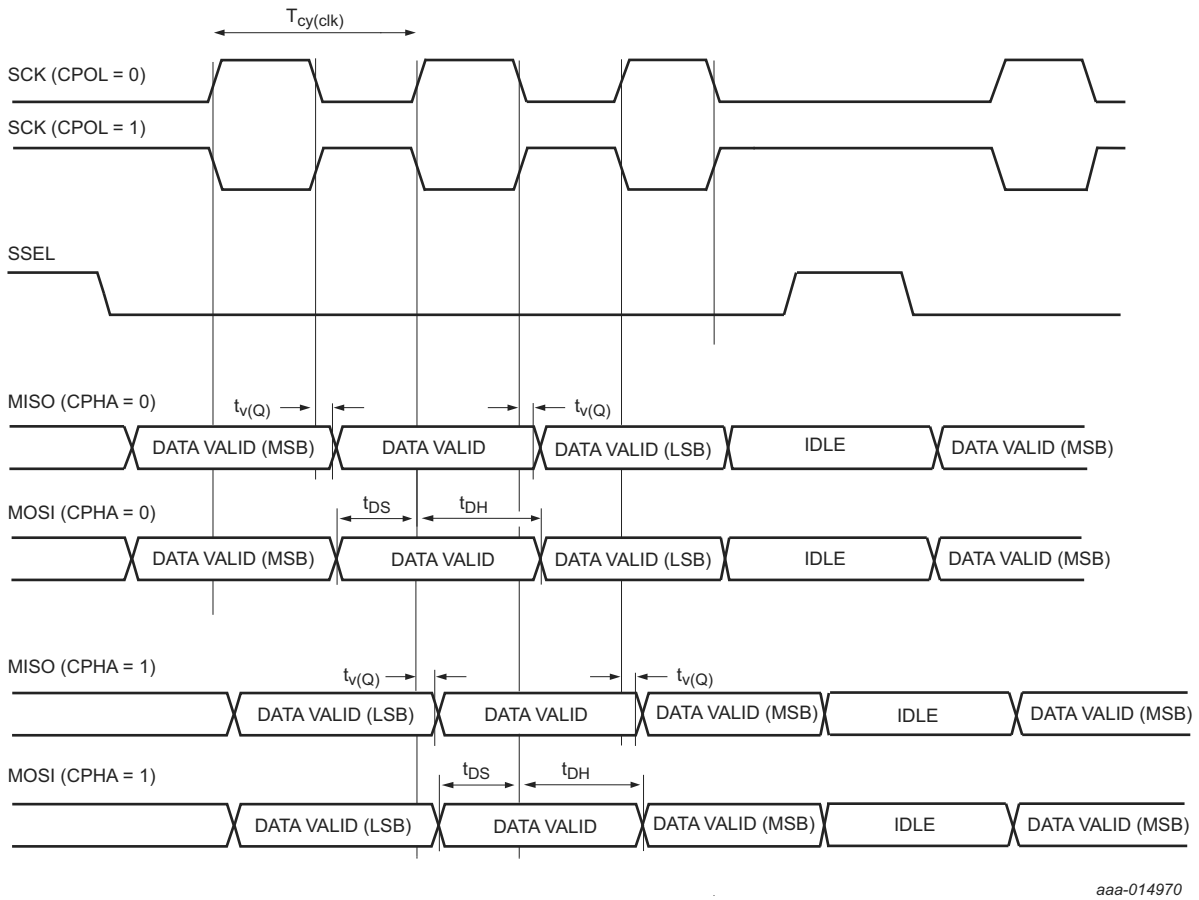

Fig 33. SPI slave timing

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12. Analog characteristics

12.1 BOD

Table 51. BOD static characteristics

T_{amb} = 25 °C; based on characterization; not tested in production.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{th}	threshold voltage	interrupt level 0					
		assertion		1.5	-	1.63	V
		de-assertion		1.55	-	1.69	V
		reset level 0					
		assertion		1.5	-	1.62	V
		de-assertion		1.55	-	1.69	V
V_{th}	threshold voltage	interrupt level 1					
		assertion		1.54	-	1.68	V
		de-assertion		1.6	-	1.75	V
		reset level 1					
		assertion		1.55	-	1.68	V
		de-assertion		1.61	-	1.74	V
V_{th}	threshold voltage	interrupt level 2					
		assertion		1.79	-	1.95	V
		de-assertion		1.85	-	2.02	V
		reset level 2					
		assertion		2.04	-	2.21	V
		de-assertion		2.19	-	2.38	V
V_{th}	threshold voltage	interrupt level 3					
		assertion		2.62	-	2.86	V
		de-assertion		2.77	-	3.03	V
		reset level 3					
		assertion		2.62	-	2.85	V
		de-assertion		2.78	-	3.02	V

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13.6.1 XTAL Printed Circuit Board (PCB) design guidelines

- Connect the crystal and external load capacitors on the PCB as close as possible to the oscillator input and output pins of the chip.
- The length of traces in the oscillation circuit should be as short as possible and must not cross other signal lines.
- Ensure that the load capacitors CX1, CX2, and CX3, in case of third overtone crystal usage, have a common ground plane.
- Loops must be made as small as possible to minimize the noise coupled in through the PCB and to keep the parasitics as small as possible.
- Lay out the ground (GND) pattern under crystal unit.
- Do not lay out other signal lines under crystal unit for multi-layered PCB.

13.7 Suggested USB interface solutions

The USB device can be connected to the USB as self-powered device (see Figure 49) or bus-powered device (see Figure 50).

On the LPC540xx, the USB_VBUS pin is 5 V tolerant only when V_{DD} is applied and at operating voltage level. Therefore, if the USB_VBUS function is connected to the USB connector and the device is self-powered, the USB_VBUS pin must be protected for situations when V_{DD} = 0 V.

If V_{DD} is always at operating level while VBUS = 5 V, the USB_VBUS pin can be connected directly to the VBUS pin on the USB connector.

For systems where V_{DD} can be 0 V and VBUS is directly applied to the VBUS pin, precautions must be taken to reduce the voltage to below 3.6 V, which is the maximum allowable voltage on the USB_VBUS pin in this case.

One method is to use a voltage divider to connect the USB_VBUS pin to the VBUS on the USB connector. The voltage divider ratio should be such that the USB_VBUS pin is greater than 0.7 V_{DD} to indicate a logic HIGH while below the 3.6 V allowable maximum voltage.

For the following operating conditions

$VBUS_{max}$ = 5.25 V

V_{DD} = 3.6 V,

the voltage divider should provide a reduction of 3.6 V/5.25 V or ~0.686 V.

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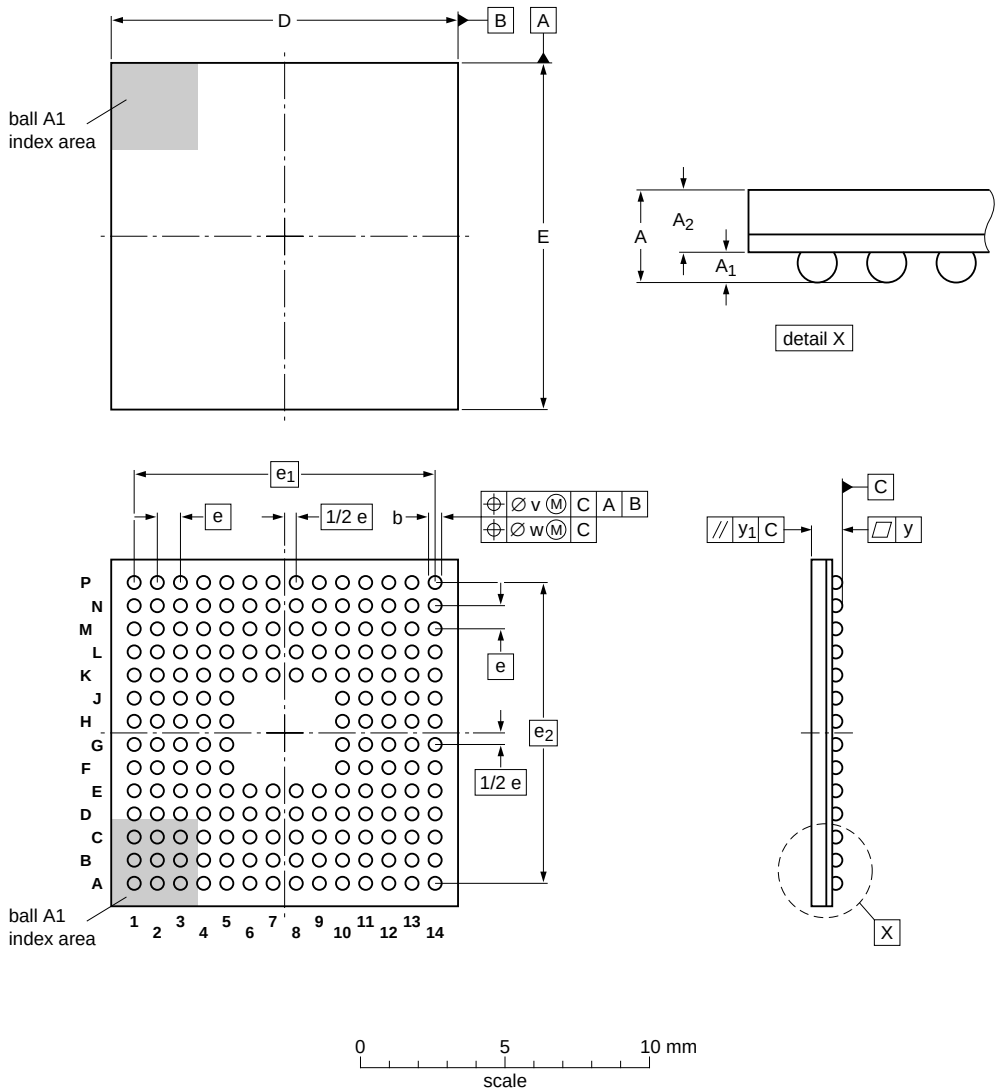
TFBGA180: thin fine-pitch ball grid array package; 180 balls **SOT570-3**



DIMENSIONS (mm are the original dimensions)

UNIT		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	max	1.20	0.40	0.80	0.50	12.1	12.1	0.8	10.4	10.4	0.15	0.05	0.12	0.1
	nom	1.06	0.35	0.71	0.45	12.0	12.0							
	min	0.95	0.30	0.65	0.40	11.9	11.9							

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT570-3						~~08-07-09~~ 10-04-15

Fig 53. TFBGA180 package

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