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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	EBI/EMI, I²C, MMC/SD/SDIO, SmartCard, SPI, SPIFI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	64
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	360K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFBGA
Supplier Device Package	100-TFBGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc54005jet100e

- Up to 171 General-Purpose Input/Output (GPIO) pins.
- GPIO registers are located on the AHB for fast access. The DMA supports GPIO ports.
- Up to eight GPIOs can be selected as Pin Interrupts (PINT), triggered by rising, falling or both input edges.
- Two GPIO Grouped Interrupts (GINT) enable an interrupt based on a logical (AND/OR) combination of input states.

- Analog peripherals:
  - 12-bit ADC with 12 input channels and with multiple internal and external trigger inputs and sample rates of up to 5.0 MSamples/sec. The ADC supports two independent conversion sequences.
  - Integrated temperature sensor connected to the ADC.
- DMIC subsystem includes a dual-channel PDM microphone interface with decimators, filtering, and hardware voice activity detection. The processed output data can be routed directly to an I^2S interface if needed.
- Timers:
  - Five 32-bit general purpose timers/counters. All five timers support up to four capture inputs and four compare outputs, PWM mode, and external count input. Specific timer events can be selected to generate DMA requests.
  - One SCTimer/PWM with eight input and ten output functions (including capture and match). Inputs and outputs can be routed to or from external pins and internally to or from selected peripherals. Internally, the SCTimer/PWM supports 16 match/captures, 16 events, and 16 states.
  - 32-bit Real-time clock (RTC) with 1 s resolution running in the always-on power domain. A timer in the RTC can be used for wake-up from all low power modes including deep power-down, with 1 ms resolution.
  - Multiple-channel multi-rate 24-bit timer (MRT) for repetitive interrupt generation at up to four programmable, fixed rates.
  - Windowed Watchdog Timer (WWDT).
  - Repetitive Interrupt Timer (RIT) for debug time stamping and for general purpose use.
- Security features:
  - Secure Hash Algorithm (SHA1/SHA2) module supports boot with dedicated DMA controller.
- Clock generation:
  - 12 MHz internal Free Running Oscillator (FRO). This oscillator provides a selectable 48 MHz or 96 MHz output, and a 12 MHz output (divided down from the selected higher frequency) that can be used as a system clock. The FRO is trimmed to ±1 % accuracy over the entire voltage and temperature range.
  - Crystal oscillator with an operating range of 1 MHz to 25 MHz.
  - Watchdog Oscillator (WDTOSC) with a frequency range of 6 kHz to 1.5 MHz.
  - 32.768 kHz low-power RTC oscillator.
  - System PLL allows CPU operation up to the maximum CPU rate and can run from the main oscillator, the internal FRO, the watchdog oscillator or the 32.768 KHz RTC oscillator.
  - Two additional PLLs for USB clock and audio subsystem.
  - Independent clocks for the SPIFI interface, ADC, USBs, and the audio subsystem.

4. Marking

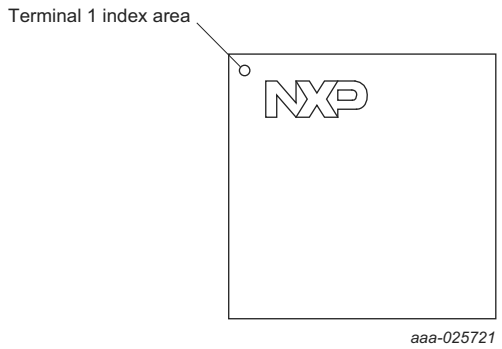


Fig 1. TFBGA180 and TFBGA 100 package markings

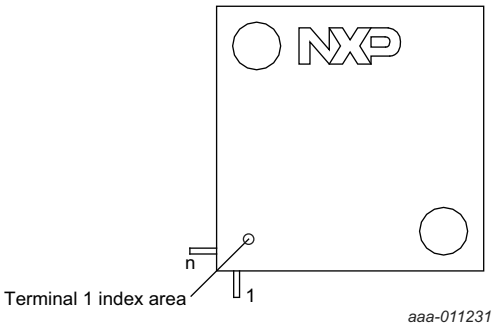


Fig 2. LQFP208 package marking

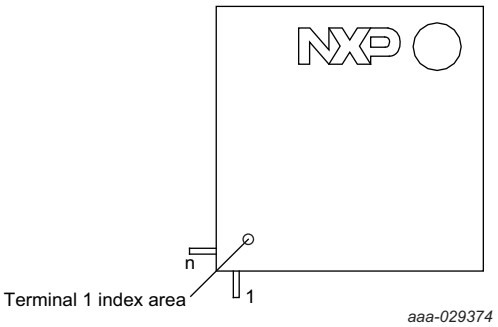


Fig 3. LQFP100 package marking

The LPC540xx TFBGA180 and TFBGA100 packages have the following top-side marking:

- First line: LPC540xxJ
- Second line: ET180 or ET100
- Third line: xxxxxxxxxxxx
- Fourth line: xxxyywwx[R]x
  - yyww: Date code with yy = year and ww = week.
  - xR = boot code version and device revision.

The LPC540xx LQFP208 and LQFP100 packages have the following top-side marking:

- First line: LPC540xxJ
- Second line: BD208 or BD100
- Third line: xxxxxxxxxxxx
- Fourth line: xxxyywwx[R]x
  - yyww: Date code with yy = year and ww = week.
  - xR = Boot code version and device revision.

6. Pinning information

6.1 Pinning

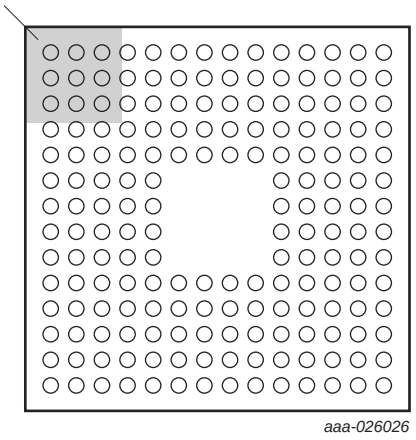


Fig 5. TFBGA 180 Pin configuration

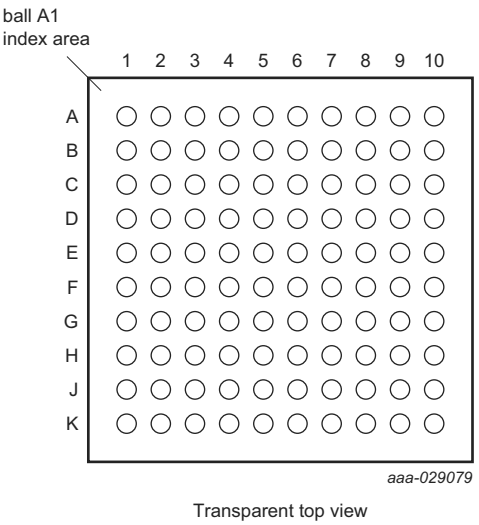


Fig 6. TFBGA 100 Pin configuration

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state[1] [9]	Type	Description
PIO0_6/ TDO	A4	A5	191	90	[2]	PU; Z	I/O	**PIO0_6 —** General-purpose digital input/output pin. In boundary scan mode: TDO (Test Data Out). **Remark:** The state of this pin at Reset in conjunction with PIO0_4 and PIO0_5 will determine the boot source for the part or if ISP handler is invoked. See the Boot Process chapter in UM11060 for more details.
							I/O	**FC3_SCK —** Flexcomm 3: USART or SPI clock.
							I	**CT3_CAP1 —** Capture input 1 to Timer 3.
							O	**CT4_MAT0 —** Match output 0 from Timer 4.
							I	**SCT0_GPI6 —** Pin input 6 to SCTimer/PWM.
								R — Reserved.
							I/O	**EMC_D[4] —** External Memory interface data [4].
							I	**ENET_RX_DV —** Ethernet receive data valid.
PIO0_7	F9	H12	125	61	[2]	PU; Z	I/O	**PIO0_7 —** General-purpose digital input/output pin.
							I/O	**FC3_RTS_SCL_SSEL1 —** Flexcomm 3: USART request-to-send, I2C clock, SPI slave select 1.
							O	**SD_CLK —** SD/MMC clock.
							I/O	**FC5_SCK —** Flexcomm 5: USART or SPI clock.
							I/O	**FC1_SCK —** Flexcomm 1: USART or SPI clock.
							O	**PDM1_CLK —** Clock for PDM interface 1, for digital microphone.
							I/O	**EMC_D[5] —** External Memory interface data [5].
							I	**ENET_RX_CLK —** Ethernet Receive Clock (MII interface) or Ethernet Reference Clock (RMII interface).
PIO0_8	E9	H10	133	64	[2]	PU; Z	I/O	**PIO0_8 —** General-purpose digital input/output pin.
							I/O	**FC3_SSEL3 —** Flexcomm 3: SPI slave select 3.
							I/O	**SD_CMD —** SD/MMC card command I/O.
							I/O	**FC5_RXD_SDA_MOSI —** Flexcomm 5: USART receiver, I2C data I/O, SPI master-out/slave-in data.
							O	**SWO —** Serial Wire Debug trace output.
							I	**PDM1_DATA —** Data for PDM interface 1 (digital microphone).
							I/O	**EMC_D[6] —** External Memory interface data [6].

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state[1] [9]	Type	Description
PIO0_9	E10	G12	136	65	[2]	PU; Z	I/O	**PIO0_9 —** General-purpose digital input/output pin.
							I/O	**FC3_SSEL2 —** Flexcomm 3: SPI slave select 2.
							O	**SD_POW_EN —** SD/MMC card power enable.
							I/O	**FC5_TXD_SCL_MISO —** Flexcomm 5: USART transmitter, I2C clock, SPI master-in/slave-out data.
								R — Reserved.
							I/O	**SCI1_IO —** SmartCard Interface 1 data I/O.
							I/O	**EMC_D[7] —** External Memory interface data [7].
PIO0_10/ ADC0_0	J1	P2	50	23	[4]	PU; Z	I/O; AI	**PIO0_10/ADC0_0 —** General-purpose digital input/output pin. ADC input channel 0 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
							I/O	**FC6_SCK —** Flexcomm 6: USART, SPI, or I2S clock.
							I	**CT2_CAP2 —** Capture input 2 to Timer 2.
							O	**CT2_MAT0 —** Match output 0 from Timer 2.
							I/O	**FC1_TXD_SCL_MISO —** Flexcomm 1: USART transmitter, I2C clock, SPI master-in/slave-out data.
								R — Reserved.
							O	**SWO —** Serial Wire Debug trace output.
PIO0_11/ ADC0_1	K1	L3	51	24	[4]	PU; Z	I/O; AI	**PIO0_11/ADC0_1 —** General-purpose digital input/output pin. ADC input channel 1 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
							I/O	**FC6_RXD_SDA_MOSI_DATA —** Flexcomm 6: USART receiver, I2C data I/O, SPI master-out/slave-in data, I2S data I/O.
							O	**CT2_MAT2 —** Match output 2 from Timer 2.
							I	**FREQME_GPIO_CLK_A —** Frequency Measure pin clock input A.
								R — Reserved.
								R — Reserved.
							I	**SWCLK —** Serial Wire Debug clock. This is the default function after booting.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state[1] [9]	Type	Description
PIO2_21	-	L10	99	-	[2]	PU; Z	I/O	**PIO2_21 —** General-purpose digital input/output pin.
							O	**LCD_VD[3] —** LCD Data [3].
							I/O	**FC3_CTS_SDA_SSEL0 —** Flexcomm 3: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							I/O	**MCLK —** MCLK input or output for I2S and/or digital microphone.
							O	**CT3_MAT3 —** Match output 3 from Timer 3.
PIO2_22	-	K10	113	-	[2]	PU; Z	I/O	**PIO2_22 —** General-purpose digital input/output pin.
							O	**LCD_VD[4] —** LCD Data [4].
							O	**SCT0_OUT7 —** SCTimer/PWM output 7.
								R — Reserved.
							I	**CT2_CAP0 —** Capture input 0 to Timer 2.
								R — Reserved.
								FC10_SSEL1 — Flexcomm 10: SPI Slave Select 1.
PIO2_23	-	M14	115	-	[2]	PU; Z	I/O	**PIO2_23 —** General-purpose digital input/output pin.
							O	**LCD_VD[5] —** LCD Data [5].
							O	**SCT0_OUT8 —** SCTimer/PWM output 8.
								R — Reserved.
								R — Reserved.
								R — Reserved.
							I/O	**FC10_SSEL2 —** Flexcomm 10: SPI Slave Select 2.
PIO2_24	-	K14	118	-	[2]	PU; Z	I/O	**PIO2_24 —** General-purpose digital input/output pin.
							O	**LCD_VD[6] —** LCD Data [6].
							O	**SCT0_OUT9 —** SCTimer/PWM output 9.
								R — Reserved.
								R — Reserved.
								R — Reserved.
							I/O	**FC10_SSEL3 —** Flexcomm 10: SPI Slave Select 3.
PIO2_25	-	J11	121	-	[2][8]	PU; Z	I/O	**PIO2_25 —** General-purpose digital input/output pin.
							O	**LCD_VD[7] —** LCD Data [7].
							I	**USB0_VBUS —** Monitors the presence of USB0 bus power.
PIO2_26	-	H11	124	-	[2]	PU; Z	I/O	**PIO2_26 —** General-purpose digital input/output pin.
							O	**LCD_VD[8] —** LCD Data [8].
								R — Reserved.
							I/O	**FC3_SCK —** Flexcomm 3: USART or SPI clock.
							I	**CT2_CAP1 —** Capture input 1 to Timer 2.

Table 5. Termination of unused pins

Pin	Default state[1][2]	Recommended termination of unused pins
VBAT	-	Tie to VDD.
USBn_DP	F	Can be left unconnected. If USB interface is not used, pin can be left unconnected except in deep power-down mode where it must be externally pulled low. When the USB PHY is disabled, the pins are floating.
USBn_DM	F	Can be left unconnected. If USB interface is not used, pin can be left unconnected except in deep power-down mode where it must be externally pulled low. When the USB PHY is disabled, the pins are floating.
USB1_AVSCC	F	Tie to VSS.
USB1_VBUS	F	Tie to VDD.
USB1_AVDDC3V3	F	Tie to VDD.
USB1_AVDDTX3V3	F	Tie to VDD.
USB1_AVSSTX3V3	F	Tie to VSS.
USB1_ID	F	Can be left unconnected. If USB interface is not used, pin can be left unconnected.

[1] I = Input, IA = Inactive (no pull-up/pull-down enabled), PU = Pull-Up enabled, F = Floating

[2] For initial device revision 0A (Boot ROM version 21.0), PU = input mode, pull-up enabled (pull-up resistor pulls up pin to VDD). For future device revision 1B (Boot ROM version 21.1), Z = high impedance; pull-up or pull-down disabled. See the Errata sheet LPC540xx (IOCON.1) for more details. For future device revision 1B (Boot ROM version 21.1), GPIO pins PIO0_12, PIO0_11, PIO0_2, PIO0_3, PIO0_4, PIO0_5, and PIO0_6 have the input buffer enabled (DIGIMODE, bit 8 is enabled in IOCON register) and will be floating by default. If unused, it is recommended to externally terminate this pins to prevent leakage.

6.2.2 Pin states in different power modes

Table 6. Pin states in different power modes

Pin	Active	Sleep	Deep-sleep	Deep power-down[3]
PIOn_m pins (not I2C)	As configured in the IOCON[1]. Default: internal pull-up enabled or high Z [2].			Floating
PIO0_13 to PIO0_14 (open-drain I2C-bus pins)	As configured in the IOCON[1].			Floating
PIO3_23 to PIO3_24 (open-drain I2C-bus pins)	As configured in the IOCON[1].			Floating
$\overline{\text{RESET}}$	Reset function enabled. Default: input, internal pull-up enabled. Reset function disabled.			

[1] Default and programmed pin states are retained in sleep and deep-sleep.

[2] For initial device revision 0A (Boot ROM version 21.0), PU = input mode, pull-up enabled (pull-up resistor pulls up pin to VDD). For future device revision 1B (Boot ROM version 21.1), Z = high impedance; pull-up or pull-down disabled. See the Errata sheet LPC540xx (IOCON.1) for more details. For future device revision 1B (Boot ROM version 21.1), GPIO pins PIO0_12, PIO0_11, PIO0_2, PIO0_3, PIO0_4, PIO0_5, and PIO0_6 have the input buffer enabled (DIGIMODE, bit 8 is enabled in IOCON register) and will be floating by default. If unused, it is recommended to externally terminate this pins to prevent leakage.

[3] If VBAT> VDD, the external reset pin must be floating to prevent high VBAT leakage.

7.10.1.3 Crystal oscillator

The LPC540xx include four independent oscillators. These are the main oscillator, the FRO, the watchdog oscillator, and the RTC oscillator.

Following reset, the LPC540xx will operate from the Internal FRO until switched by software. This allows systems to operate without any external crystal and the boot loader code to operate at a known frequency. See Figure 11 and Figure 12 for an overview of the LPC540xx clock generation.

7.10.2 System PLL (PLL0)

The system PLL accepts an input clock frequency in the range of 32.768 kHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO).

The PLL can be enabled or disabled by software.

7.10.3 USB PLL (PLL1)

The USB PLL accepts an input clock frequency in the range of 1 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO).

The PLL can be enabled or disabled by software.

7.10.4 Audio PLL (PLL2)

The audio PLL accepts an input clock frequency in the range of 1 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO).

The PLL can be enabled or disabled by software.

7.14.8.2 SPI serial I/O controller

Features

- Maximum data rates of 48 Mbit/s in master mode and 14 Mbit/s in slave mode for SPI functions. (Flexcomm Interface 0-9).
- Maximum data rates of 50 Mbit/s in master mode and 50 Mbit/s in slave mode for SPI functions (Flexcomm Interface10).
- Data frames of 1 to 16 bits supported directly. Larger frames supported by software or DMA set-up.
- Master and slave operation.
- Data can be transmitted to a slave without the need to read incoming data. This can be useful while setting up an SPI memory.
- Control information can optionally be written along with data. This allows very versatile operation, including “any length” frames.
- Four Slave Select input/outputs with selectable polarity and flexible usage.
- Activity on the SPI in slave mode allows wake-up from deep-sleep mode on any enabled interrupt.

Remark: Texas Instruments SSI and National Microwire modes are not supported.

7.14.8.3 I^2C-bus interface

The I^2C-bus is bidirectional for inter-IC control using only two wires: a serial clock line (SCL) and a serial data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (for example, an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^2C is a multi-master bus and can be controlled by more than one bus master connected to it.

Features

- All I2Cs support standard, Fast-mode, and Fast-mode Plus with data rates of up to 1 Mbit/s.
- All I2Cs support high-speed slave mode with data rates of up to 3.4 Mbit/s.
- Independent Master, Slave, and Monitor functions.
- Supports both Multi-master and Multi-master with Slave functions.
- Multiple I^2C slave addresses supported in hardware.
- One slave address can be selectively qualified with a bit mask or an address range in order to respond to multiple I^2C-bus addresses.
- 10-bit addressing supported with software assist.
- Supports SMBus.
- Activity on the I2C in slave mode allows wake-up from deep-sleep mode on any enabled interrupt.

7.20.1.1 Features

- Secure Hash Algorithm (SHA1/SHA2) module with dedicated DMA controller.
- Used with an HMAC to support a challenge/response or to validate a message.
- Can be used to verify external memory that has not been compromised.

7.21 Emulation and debugging

Debug and trace functions are integrated into the ARM Cortex-M4. Serial wire debug and trace functions are supported. The ARM Cortex-M4 is configured to support up to eight breakpoints and four watch points.

The ARM SYSREQ reset is supported and causes the processor to reset the peripherals, execute the boot code, restart from address 0x0000 0000, and break at the user entry point.

The SWD pins are multiplexed with other digital I/O pins. On reset, the pins assume the SWD functions by default.

registers. All other blocks are disabled and no code accessing the peripheral is executed. The supply currents are shown for system clock frequencies of 12 MHz, 48 MHz, 96 MHz and 180MHz.

Table 18. Typical peripheral power consumption[1][2]

V_{DD} = 3.3 V; T_{amb} = 25 °C

Peripheral	I_{DD} in uA
FRO	100
WDT OSC	2.0
BOD	2.0

[1] The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled using PDRUNCFG0/1 registers. All other blocks are disabled and no code accessing the peripheral is executed.

[2] Typical ratings are not guaranteed. Characterized through bench measurements using typical samples.

Table 19. Typical AHB/APB peripheral power consumption [3][4][5]

T_{amb} = 25 °C, V_{DD} = 3.3 V;

Peripheral		I_{DD} in uA/MHz	I_{DD} in uA/MHz	I_{DD} in uA/MHz	I_{DD} in uA/MHz
AHB peripheral		**CPU: 12 MHz, sync APB bus: 12 MHz**	**CPU: 48 MHz, sync APB bus: 48 MHz**	**CPU: 96 MHz, sync APB bus: 96 MHz**	**CPU: 180 MHz, sync APB bus: 180 MHz**
USB0 device		0.3	0.3	0.3	0.4
USB1 device		4.4	4.4	4.4	5.0
DMIC		0.2	0.2	0.2	0.2
GPIO0	[1]	0.9	0.9	0.9	1.0
GPIO1	[1]	0.8	0.8	0.8	1.0
GPIO2	[1]	1.0	1.0	1.0	1.1
GPIO3	[1]	1.1	1.1	1.1	1.3
GPIO4	[1]	1.0	1.0	1.0	1.2
GPIO5	[1]	0.7	0.7	0.7	0.8
DMA		0.7	0.7	0.7	0.8
CRC		1.0	1.0	1.0	1.0
ADC0		1.6	1.6	1.6	1.9
SCTimer/PWM		4.5	4.5	4.5	5.3
Ethernet AVB		24.0	24.0	24.0	28.0
LCD		13.0	13.0	13.0	15.0
EMC		39.0	39.0	39.0	45.4
CAN0		10.8	10.8	10.8	12.6
CAN1		10.7	10.7	10.7	12.4
SD/MMC		7.9	7.9	7.9	9.3
Flexcomm Interface 0 (USART, SPI, I^2C)		1.6	1.6	1.6	1.9
Flexcomm Interface1 (USART, SPI, I^2C)		1.6	1.6	1.6	1.8
Flexcomm Interface 2 (USART, SPI, I^2C)		1.7	1.7	1.7	1.9

[2] $T_{cy(clk)}$ = 1/EMC_CLK (see *UM11060* LPC540xx *manual*).

[3] Latest of address valid, $\overline{\text{EMC\_CSx}}$ LOW, $\overline{\text{EMC\_OE}}$ LOW, $\overline{\text{EMC\_BLSx}}$ LOW (PB = 1).

[4] After End Of Read (EOR): Earliest of $\overline{\text{EMC\_CSx}}$ HIGH, $\overline{\text{EMC\_OE}}$ HIGH, $\overline{\text{EMC\_BLSx}}$ HIGH (PB = 1), address invalid.

[5] End Of Write (EOW): Earliest of address invalid, $\overline{\text{EMC\_CSx}}$ HIGH, $\overline{\text{EMC\_BLSx}}$ HIGH (PB = 1).

[6] The byte lane state bit, PB, enables different types of memory to be connected (see *the STATICCONFIG[0:3] register in the UM11060* LPC540xx *manual*).

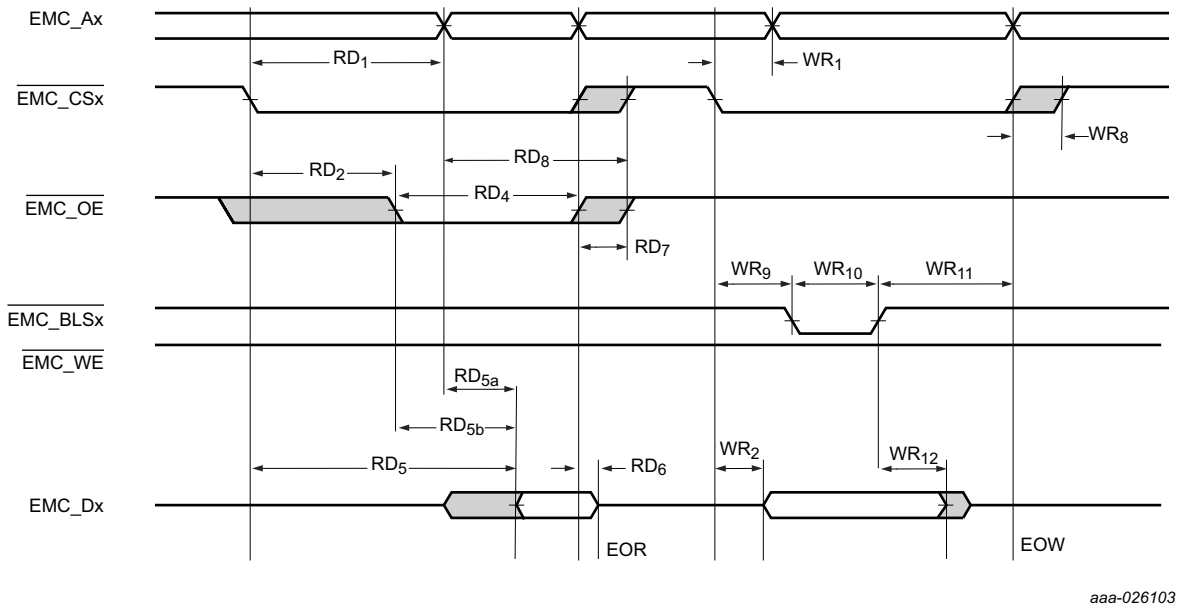


Fig 23. External static memory read/write access (PB = 0)

11.4 System PLL (PLL0)

Table 28. PLL lock times and current

T_{amb} = −40 °C to +105 °C, unless otherwise specified. V_{DD} = 1.71 V to 3.6 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
PLL0 configuration: input frequency 12 MHz; output frequency 100 MHz							
$t_{lock(PLL0)}$	PLL0 lock time		[1]			96	µs
$I_{DD(PLL0)}$	PLL0 current	when locked	[1][2]	-	-	2.0	mA
PLL0 configuration: input frequency 32 kHz; output frequency 100 MHz							
$t_{lock(PLL0)}$	PLL0 lock time		[1]	-	-	108	µs
$I_{DD(PLL0)}$	PLL0 current	when locked	[1][2]	-	-	1.6	mA

[1] Data based on characterization results, not tested in production.

[2] PLL current measured using lowest CCO frequency to obtain the desired output frequency.

Table 29. Dynamic characteristics of the PLL0[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Reference clock input							
F_{in}	input frequency			32.768 kHz	-	25 MHz	
Clock output							
f_o	output frequency	for PLL0 clkout output	[2]	4.3	-	550	MHz
d_o	output duty cycle	for PLL0 clkout output		46	-	54	%
f_{CCO}	CCO frequency			275	-	550	MHz
Lock detector output							
$\Delta_{lock(PFD)}$	PFD lock criterion		[3]	1	2	4	ns
Dynamic parameters at $f_{out} = f_{CCO}$ = 540 MHz; standard bandwidth settings							
$J_{rms\text{-}interval}$	RMS interval jitter	f_{ref} = 10 MHz	[4][5]	-	15	30	ps
$J_{pp\text{-}period}$	peak-to-peak, period jitter	f_{ref} = 10 MHz	[4][5]	-	40	80	ps

[1] Data based on characterization results, not tested in production.

[2] Excluding under- and overshoot which may occur when the PLL is not in lock.

[3] A phase difference between the inputs of the PFD (clkref and clkfb) smaller than the PFD lock criterion means lock output is HIGH.

[4] Actual jitter dependent on amplitude and spectrum of substrate noise.

[5] Input clock coming from a crystal oscillator with less than 250 ps peak-to-peak period jitter.

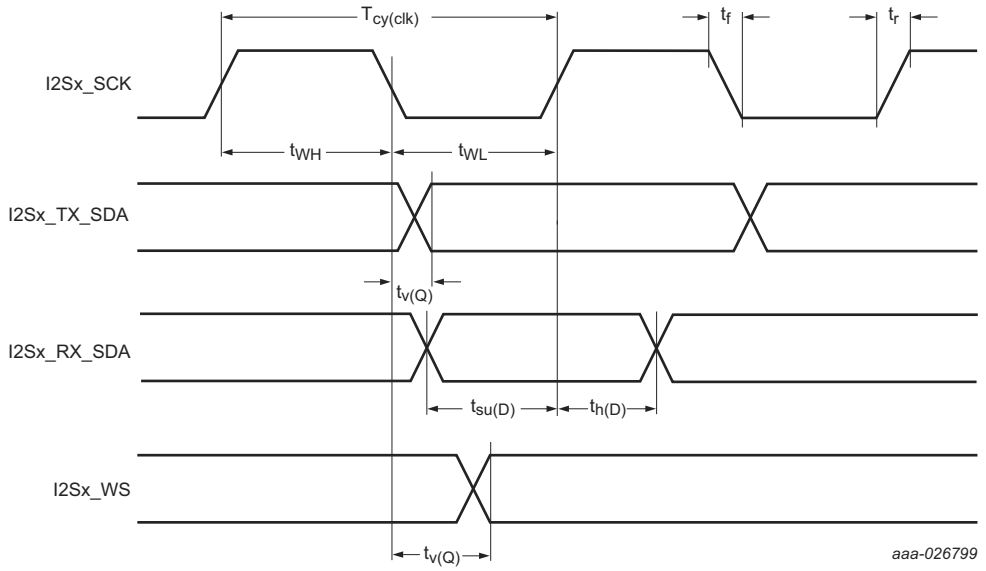


Fig 28. I²S-bus timing (master)

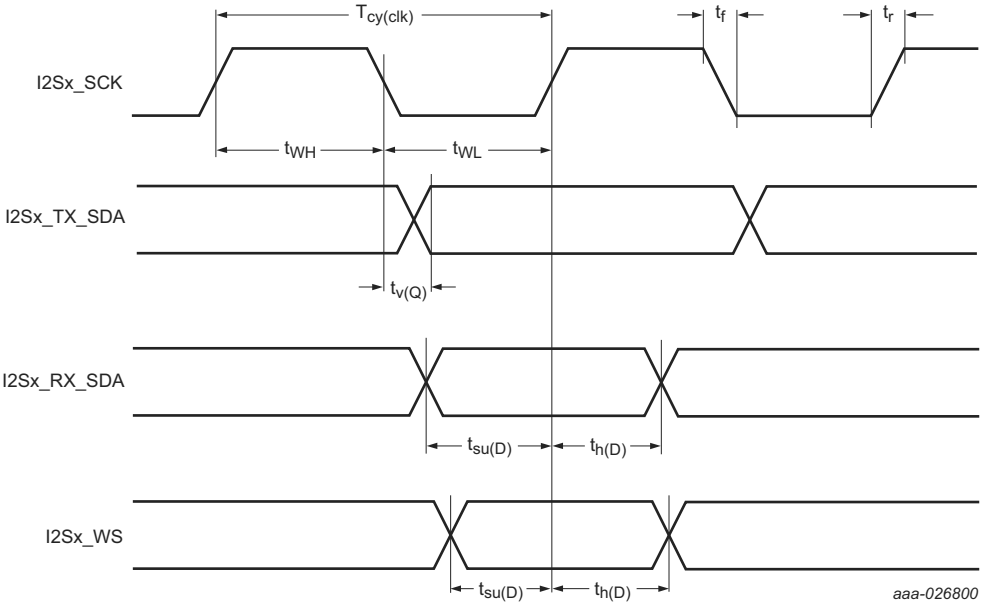


Fig 29. I²S-bus timing (slave)

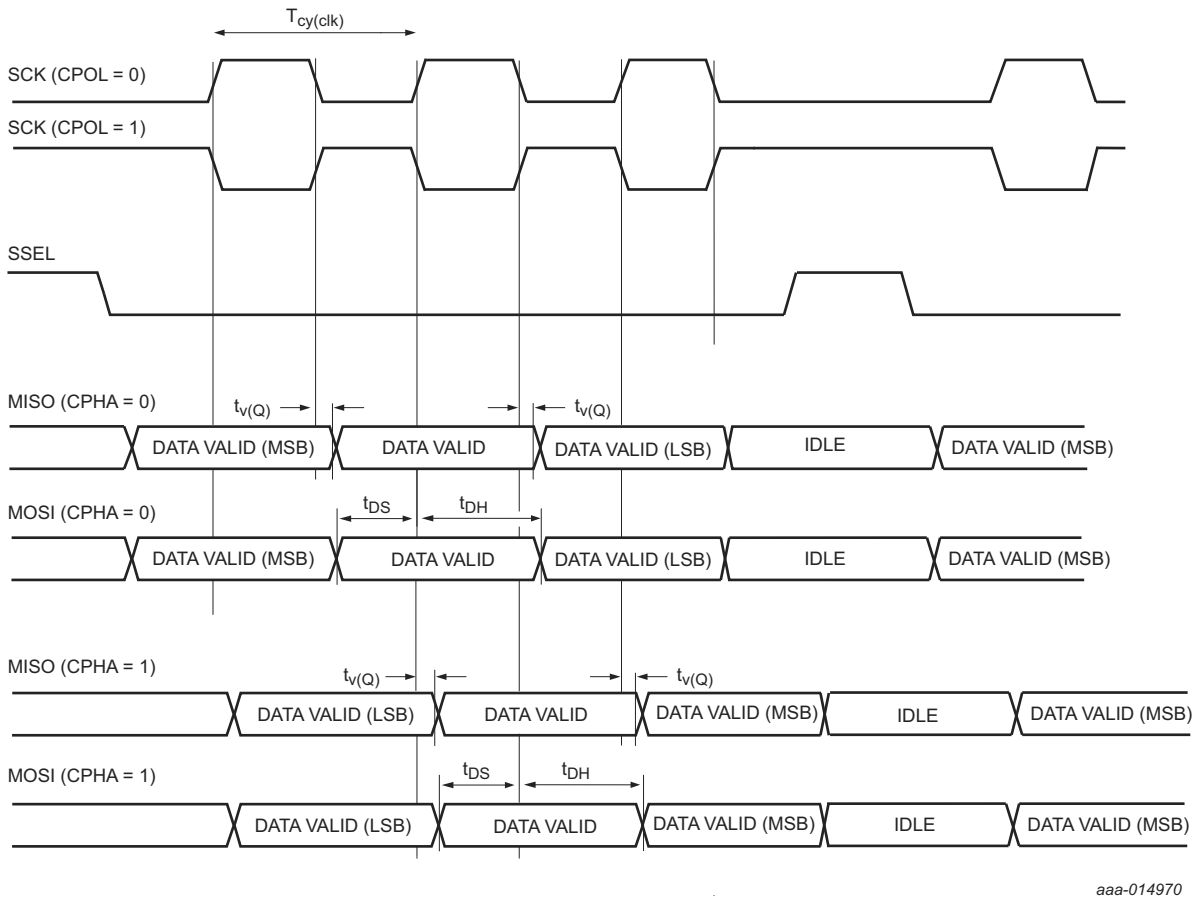


Fig 33. SPI slave timing

Table 48. Dynamic characteristics: Ethernet

T_{amb} = −40 °C to 105 °C, V_{DD} = 2.7 V to 3.6 V. C_L = 30 pF balanced loading on all pins; Input slew = 1 ns, SLEW setting = standard mode for all pins; Parameters sampled at the 90 % and 10 % level of the rising or falling edge. Based on simulation.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_h	data input hold time	for ENET_RXDn, ENET_RX_ER, ENET_RX_DV	[1][2]				
		CCLK ≤ 100 MHz		−1.2	-	0	ns
		CCLK > 100 MHz		−1.2	-	0	ns
$t_{v(Q)}$	data output valid time	for ENET_TXDn, ENET_TX_EN, ENET_TX_ER	[1][2]				
		CCLK ≤ 100 MHz		10.0	-	18.2	ns
		CCLK > 100 MHz		10.0	-	18.2	ns

[1] Output drivers can drive a load ≥ 25 pF accommodating over 12 inch of PCB trace and the input capacitance of the receiving device.

[2] Timing values are given from the point at which the clock signal waveform crosses 1.4 V to the valid input or output level.

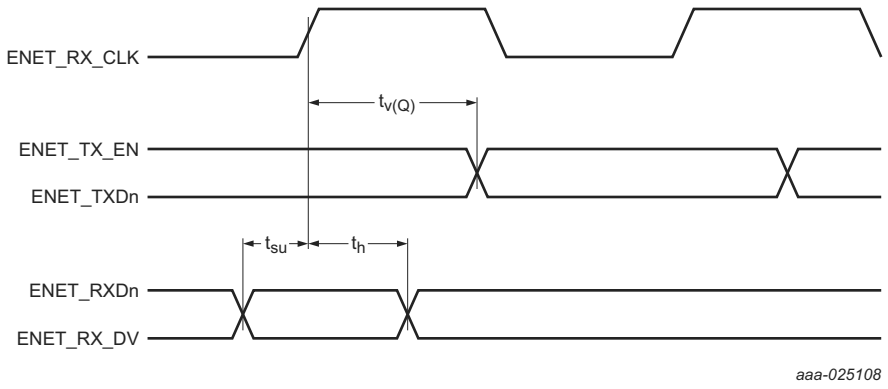


Fig 38. Ethernet RMII timing

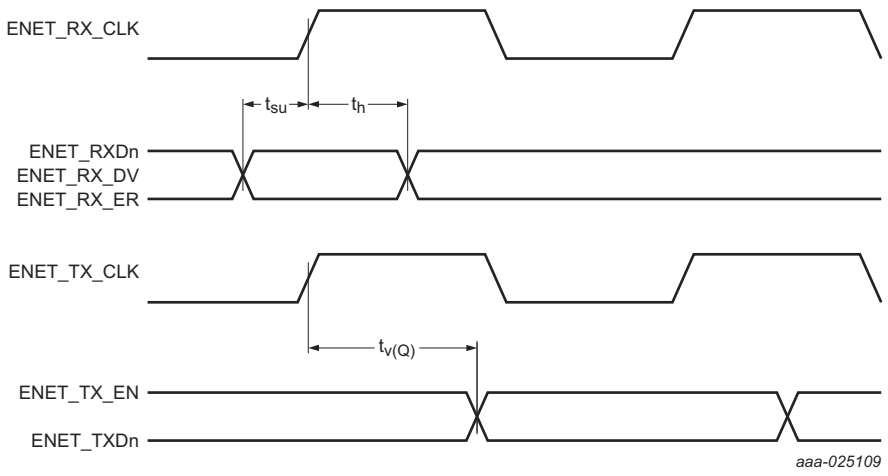


Fig 39. Ethernet MII timing

13. Application information

13.1 Start-up behavior

Figure 44 shows the start-up timing after reset. The FRO 12 MHz oscillator provides the default clock at Reset and provides a clean system clock shortly after the supply pins reach operating voltage.

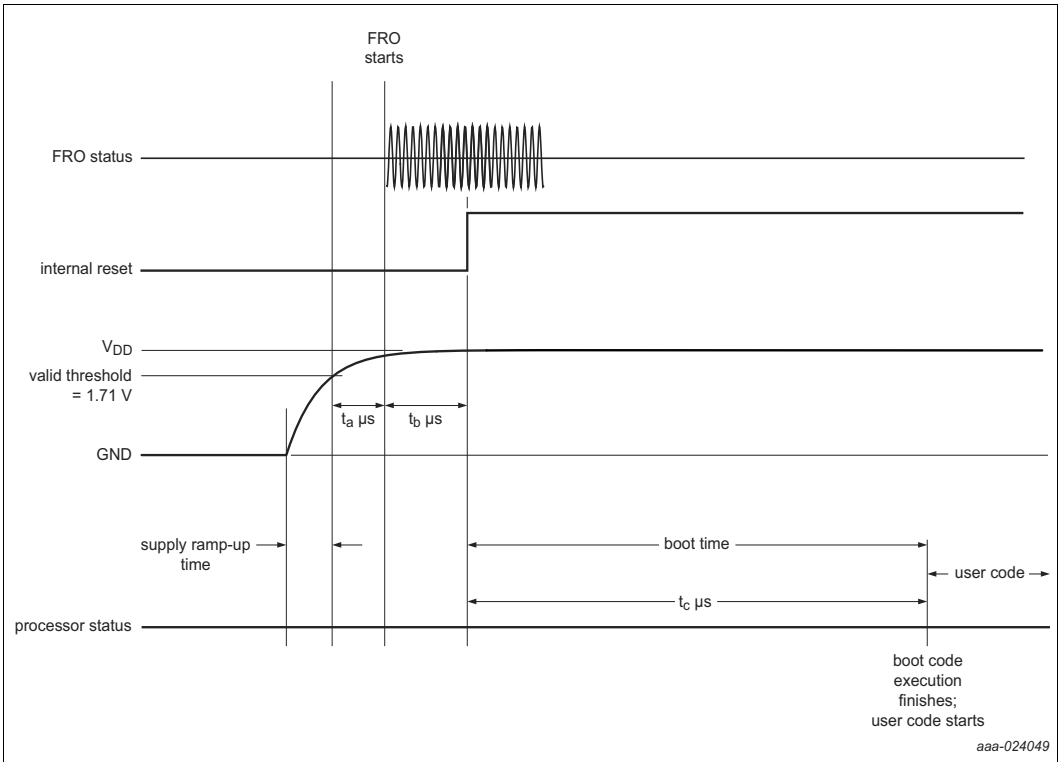
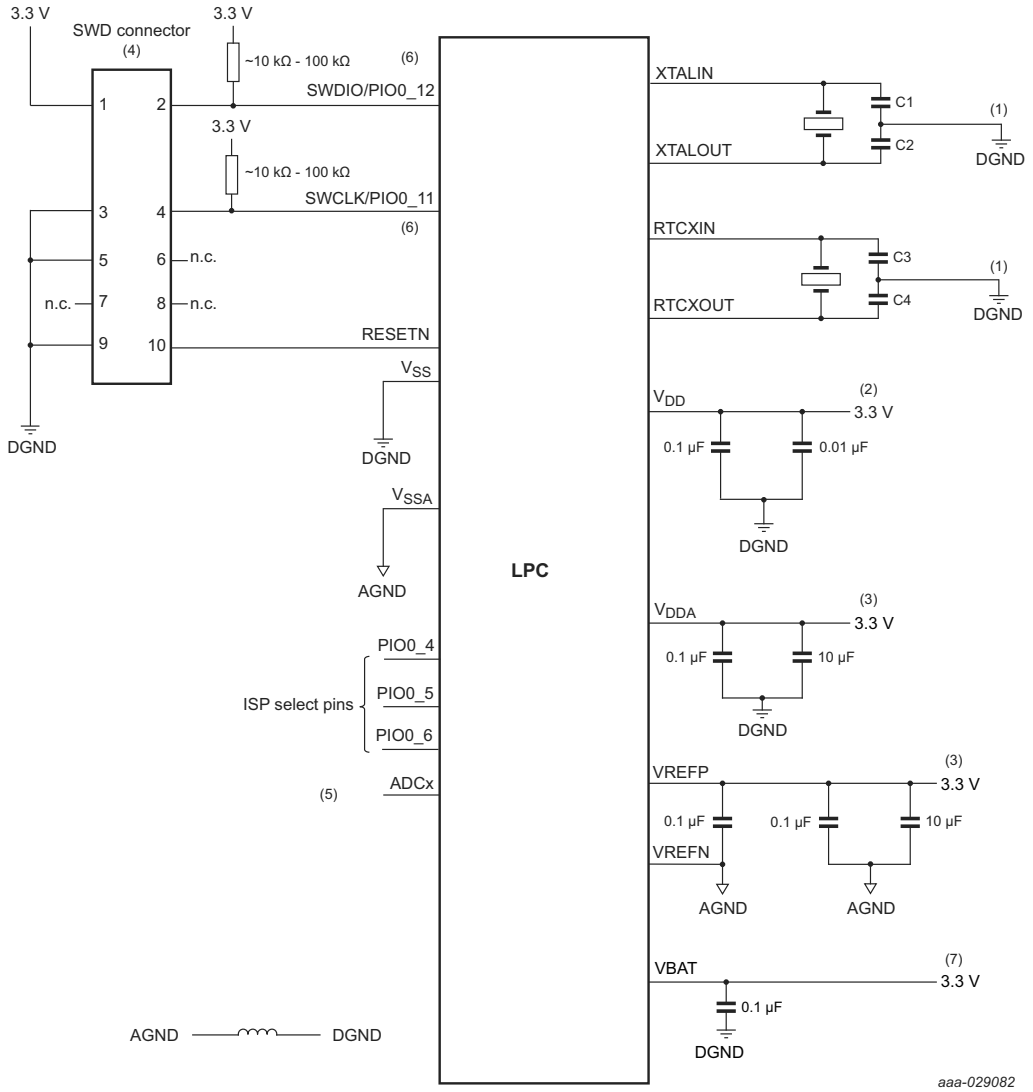


Fig 44. Start-up timing

Table 56. Typical start-up timing parameters

Parameter	Description	Value
t_a	FRO start time	≤ 20 µs
t_b	Internal reset de-asserted	151 µs



(1) See Section 13.6 “XTAL oscillator” for the values of C1, C2, C3, and C4.

(2) Position the decoupling capacitors of 0.1 µF and 0.01 µF as close as possible to the V_{DD} pin. Add one set of decoupling capacitors to each V_{DD} pin.

(3) Position the decoupling capacitors of 0.1 µF as close as possible to the VREFN and V_{DDA} pins. The 10 µF bypass capacitor filters the power line. Tie V_{DDA} and VREFP to V_{DD} if the ADC is not used. Tie VREFN to V_{SS} if ADC is not used.

(4) Uses the ARM 10-pin interface for SWD.

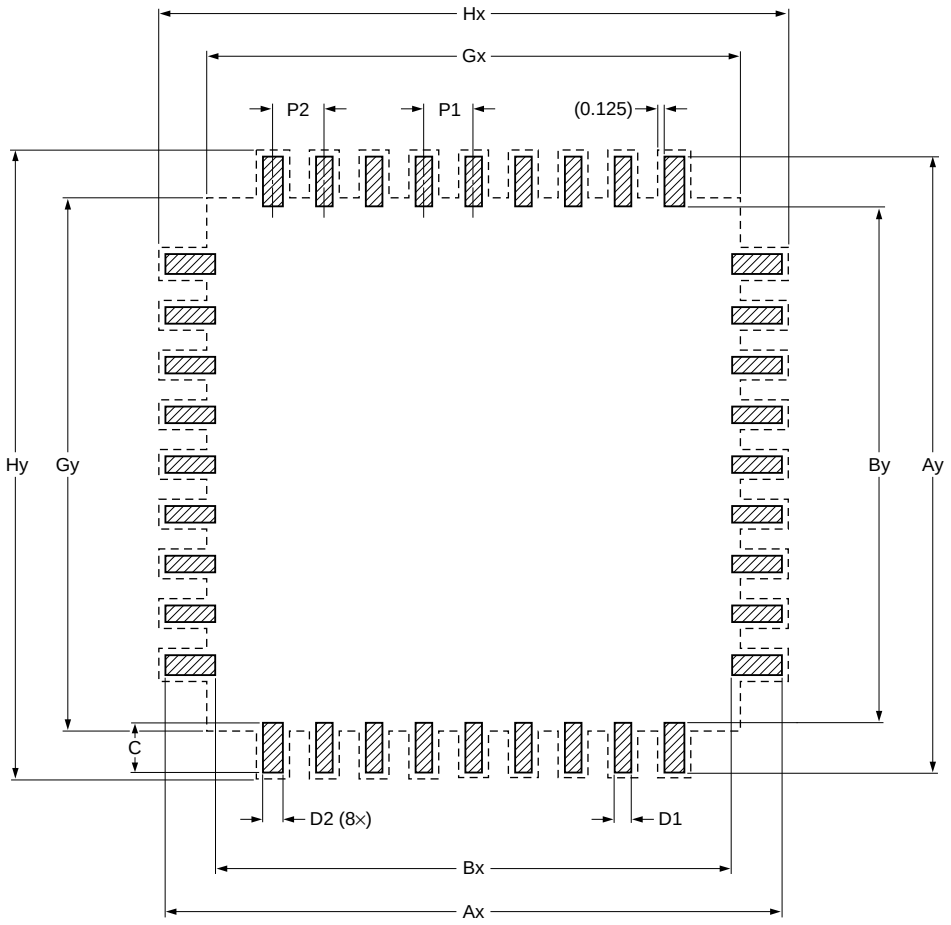
(5) When measuring signals of low frequency, use a low-pass filter to remove noise and to improve ADC performance. Also see Ref. 3.

(6) External pull-up resistors on SWDIO and SWCLK pins are optional because these pins have an internal pull-up enabled by default on initial device revision 0A (Boot ROM version 21.0). For future device revision 1B (Boot ROM version 21.1), these pins are in high Z mode (internal pull-up and pull-down disabled). See the Errata sheet LPC540xx (IOCON.1) for more details. For future device revision 1B (Boot ROM version 21.1), GPIO pins SWDIO/PIO0_12, SWCLK/PIO0_11, PIO0_2, PIO0_3, PIO0_4, PIO0_5, and PIO0_6 have the input buffer enabled (DIGIMODE, bit 8 is enabled in IOCON register) and will be floating by default. If unused, it is recommended to externally terminate this pins to prevent leakage.

(7) Position the decoupling capacitor of 0.1 µF as close as possible to the V_{BAT} pin. Tie V_{BAT} to V_{DD} if not used.

Fig 46. Power, clock, and debug connections

Footprint information for reflow soldering of LQFP100 package **SOT407-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	17.300	17.300	14.300	14.300	1.500	0.280	0.400	14.500	14.500	17.550	17.550

sot407-1

Fig 56. Reflow soldering of the LQFP100 package

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