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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SmartCard, SPI, SPIFI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	64
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	360K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc54016jbd100e

- General-purpose One-Time Programmable (OTP) memory for user application specific data

- ROM API support:
  - In-Application Programming (IAP) and In-System Programming (ISP).
  - ROM-based USB drivers (HID, CDC, MSC, and DFU).
  - Supports serial interface booting (UART, I2C, SPI) from an application processor, automated booting from NOR flash (quad SPIFI, 8/16/32-bit external parallel flash), and USB booting (full-speed, high-speed).
  - FRO API for selecting FRO output frequency.
  - OTP API for programming OTP memory.
  - Random Number Generator (RNG) API.
- Execute in place (XIP) from SPIFI NOR flash (in quad, dual SPIFI mode or single-bit SPI mode), and parallel NOR flash.
- Serial interfaces:
  - Flexcomm Interface contains up to 11 serial peripherals. Each Flexcomm Interface (except flexcomm 10, which is dedicated for SPI) can be selected by software to be a USART, SPI, or I2C interface. Two Flexcomm Interfaces also include an I2S interface. Each Flexcomm Interface includes a FIFO that supports USART, SPI, and I2S if supported by that Flexcomm Interface. A variety of clocking options are available to each Flexcomm Interface and include a shared fractional baud-rate generator.
  - I2C-bus interfaces support Fast-mode and Fast-mode Plus with data rates of up to 1Mbit/s and with multiple address recognition and monitor mode. Two sets of true I2C pads also support High Speed Mode (3.4 Mbit/s) as a slave.
  - Two ISO 7816 Smart Card Interfaces with DMA support.
  - USB 2.0 high-speed host/device controller with on-chip high-speed PHY.
  - USB 2.0 full-speed host/device controller with on-chip PHY and dedicated DMA controller supporting crystal-less operation in device mode using software library. See Technical note TN00033 for more details.
  - SPIFI with XIP feature uses up to four data lines to access off-chip SPI/DSPI/QSPI flash memory at a much higher rate than standard SPI or SSP interfaces.
  - Ethernet MAC with MII/RMII interface with Audio Video Bridging (AVB) support and dedicated DMA controller.
  - Two CAN FD modules with dedicated DMA controller.
- Digital peripherals:
  - DMA controller with 32 channels and up to 24 programmable triggers, able to access all memories and DMA-capable peripherals.
  - LCD Controller supporting both Super-Twisted Nematic (STN) and Thin-Film Transistor (TFT) displays. It has a dedicated DMA controller, selectable display resolution (up to 1024 x 768 pixels), and supports up to 24-bit true-color mode.
  - External Memory Controller (EMC) provides support for asynchronous static memory devices such as RAM, ROM and flash, in addition to dynamic memories such as single data rate SDRAM with an SDRAM clock of up to 100 MHz. EMC bus width (bit) on TFBGA180, TFBGA100, and LQFP100 packages supports up to 8/16 data line wide static memory.
  - Secured digital input/output (SD/MMC and SDIO) card interface with DMA support.
  - CRC engine block can calculate a CRC on supplied data using one of three standard polynomials with DMA support.

3.1 Ordering options

Table 2. Ordering options

Type number	Package Name	SRAM/kB	FS USB	HS USB	Ethernet AVB	Classic CAN	CAN FD	LCD	EMC data bus width (bit)	Flexcomm Interface	GPIO	SHA
LPC54018 devices (HS/FS USB, Ethernet, CAN 2.0+CAN FD, LCD, SHA)												
LPC54018JET180	TFBGA180	360	yes	yes	yes	yes	yes	yes	8/16	11	145	yes
LPC54018JBD208	LQFP208	360	yes	yes	yes	yes	yes	yes	8/16/32	11	171	yes
LPC54016 devices (HS/FS USB, Ethernet, CAN 2.0+CAN FD, SHA)												
LPC54016JET180	TFBGA180	360	yes	yes	yes	yes	yes	-	8/16	11	145	yes
LPC54016JBD208	LQFP208	360	yes	yes	yes	yes	yes	-	8/16/32	11	171	yes
LPC54016JBD100	LQFP100	360	yes	yes	yes	yes	yes	-	8/16	10	64	yes
LPC54016JET100	TFBGA100	360	yes	yes	yes	yes	yes	-	8/16	10	64	yes
LPC54005 devices (HS/FS USB, SHA)												
LPC54005JET100	TFBGA100	360	yes	yes	-	-	-	-	8/16	10	64	yes
LPC54005JBD100	LQFP100	360	yes	yes	-	-	-	-	8/16	10	64	yes

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state[1] [9]	Type	Description
PIO0_12/ ADC0_2	J2	M3	52	25	[4]	PU; Z	I/O; AI	**PIO0_12/ADC0_2 —** General-purpose digital input/output pin. ADC input channel 2 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
							I/O	**FC3_TXD_SCL_MISO —** Flexcomm 3: USART transmitter, I2C clock, SPI master-in/slave-out data.
								R — Reserved.
							I	**FREQME_GPIO_CLK_B —** Frequency Measure pin clock input B.
							I	**SCT0_GPI7 —** Pin input 7 to SCTimer/PWM.
								R — Reserved.
							I/O	**SWDIO —** Serial Wire Debug I/O. This is the default function after booting.
PIO0_13	C10	F11	141	67	[3]	Z	I/O	**PIO0_13 —** General-purpose digital input/output pin. **Remark:** In ISP mode, this pin is set to the Flexcomm 1 I2C SDA function.
							I/O	**FC1_CTS_SDA_SSEL0 —** Flexcomm 1: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							I	**UTICK_CAP0 —** Micro-tick timer capture input 0.
							I	**CT0_CAP0 —** Capture input 0 to Timer 0.
							I	**SCT0_GPI0 —** Pin input 0 to SCTimer/PWM.
								R — Reserved.
								R — Reserved.
							I	**ENET_RXD0 —** Ethernet receive data 0.
PIO0_14	D9	E13	144	69	[3]	Z	I/O	**PIO0_14 —** General-purpose digital input/output pin. **Remark:** In ISP mode, this pin is set to the Flexcomm 1 I2C SCL function.
							I/O	**FC1_RTS_SCL_SSEL1 —** Flexcomm 1: USART request-to-send, I2C clock, SPI slave select 1.
							I	**UTICK_CAP1 —** Micro-tick timer capture input 1.
							I	**CT0_CAP1 —** Capture input 1 to Timer 0.
							I	**SCT0_GPI1 —** Pin input 1 to SCTimer/PWM.
								R — Reserved.
								R — Reserved.
							I	**ENET_RXD1 —** Ethernet receive data 1.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state[1] [9]	Type	Description
PIO0_18	C9	C14	150	72	[2]	PU; Z	I/O	**PIO0_18 —** General-purpose digital input/output pin.
							I/O	**FC4_CTS_SDA_SSEL0 —** Flexcomm 4: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							I	**SD_WR_PRT —** SD/MMC write protect.
							O	**CT1_MAT0 —** Match output 0 from Timer 1.
							O	**SCT0_OUT1 —** SCTimer/PWM output 1.
							O	**SCI1_SCLK —** SmartCard Interface 1 clock.
							O	**EMC_A[0] —** External memory interface address 0.
PIO0_19	C5	C6	193	91	[2]	PU; Z	I/O	**PIO0_19 —** General-purpose digital input/output pin.
							I/O	**FC4_RTS_SCL_SSEL1 —** Flexcomm 4: USART request-to-send, I2C clock, SPI slave select 1.
							I	**UTICK_CAP0 —** Micro-tick timer capture input 0.
							O	**CT0_MAT2 —** Match output 2 from Timer 0.
							O	**SCT0_OUT2 —** SCTimer/PWM output 2.
								R — Reserved.
							O	**EMC_A[1] —** External memory interface address 1.
							I/O	**FC7_TXD_SCL_MISO_WS —** Flexcomm 7: USART transmitter, I2C clock, SPI master-in/slave-out data I/O, I2S word-select/frame.
PIO0_20	C8	D13	153	74	[2]	PU; Z	I/O	**PIO0_20 —** General-purpose digital input/output pin.
							I/O	**FC3_CTS_SDA_SSEL0 —** Flexcomm 3: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							O	**CT1_MAT1 —** Match output 1 from Timer 1.
							I	**CT3_CAP3 —** Capture input 3 to Timer 3.
							I	**SCT0_GPI2 —** Pin input 2 to SCTimer/PWM.
							I/O	**SCI0_IO —** SmartCard Interface 0 data I/O.
							O	**EMC_A[2] —** External memory interface address 2.
							I/O	**FC7_RXD_SDA_MOSI_DATA —** Flexcomm 7: USART receiver, I2C data I/O, SPI master-out/slave-in data, I2S data I/O.
PIO0_21	B9	C13	158	77	[2]	PU; Z	I/O	**PIO0_21 —** General-purpose digital input/output pin.
							I/O	**FC3_RTS_SCL_SSEL1 —** Flexcomm 3: USART request-to-send, I2C clock, SPI slave select 1.
							I	**UTICK_CAP3 —** Micro-tick timer capture input 3.
							O	**CT3_MAT3 —** Match output 3 from Timer 3.
							I	**SCT0_GPI3 —** Pin input 3 to SCTimer/PWM.
							O	**SCI0_SCLK —** SmartCard Interface 0 clock.
							O	**EMC_A[3] —** External memory interface address 3.
							I/O	**FC7_SCK —** Flexcomm 7: USART, SPI, or I2S clock.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state[1] [9]	Type	Description
PIO1_20	G2	M1	35	17	[2]	PU; Z	I/O	**PIO1_20 —** General-purpose digital input/output pin.
							I/O	**FC7_RTS_SCL_SSEL1 —** Flexcomm 7: USART request-to-send, I2C clock, SPI slave select 1.
								R — Reserved.
							I	**CT3_CAP2 —** Capture 2 input to Timer 3.
								R — Reserved.
							I/O	**FC4_TXD_SCL_MISO —** Flexcomm 4: USART transmitter, I2C clock, SPI master-in/slave-out data.
							I/O	**EMC_D[9] —** External Memory interface data [9].
PIO1_21	K6	N8	74	37	[2]	PU; Z	I/O	**PIO1_21 —** General-purpose digital input/output pin.
							I/O	**FC7_CTS_SDA_SSEL0 —** Flexcomm 7: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
								R — Reserved.
							O	**CT3_MAT2 —** Match output 2 from Timer 3.
								R — Reserved.
							I/O	**FC4_RXD_SDA_MOSI —** Flexcomm 4: USART receiver, I2C data I/O, SPI master-out/slave-in data.
							I/O	**EMC_D[10] —** External Memory interface data [10].
PIO1_22	K8	P11	89	43	[2]	PU; Z	I/O	**PIO1_22 —** General-purpose digital input/output pin.
							I/O	**FC8_RTS_SCL_SSEL1 —** Flexcomm 8: USART request-to-send, I2C clock, SPI slave select 1.
							I/O	**SD_CMD —** SD/MMC card command I/O.
							O	**CT2_MAT3 —** Match output 3 from Timer 2.
							I	**SCT0_GPI5 —** Pin input 5 to SCTimer/PWM.
							I/O	**FC4_SSEL3 —** Flexcomm 4: SPI slave select 3.
							O	**EMC_CKE[1] —** External memory interface SDRAM clock enable 1.
PIO1_23	K10	M10	97	46	[2]	PU; Z	I/O	**PIO1_23 —** General-purpose digital input/output pin.
							I/O	**FC2_SCK —** Flexcomm 2: USART or SPI clock.
							O	**SCT0_OUT0 —** SCTimer/PWM output 0.
								R — Reserved.
							I/O	**ENET_MDIO —** Ethernet management data I/O.
							I/O	**FC3_SSEL2 —** Flexcomm 3: SPI slave select 2.
							O	**EMC_A[11] —** External memory interface address 11.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state[1] [9]	Type	Description
PIO1_24	G8	N14	111	57	[2]	PU; Z	I/O	**PIO1_24 —** General-purpose digital input/output pin.
							I/O	**FC2_RXD_SDA_MOSI —** Flexcomm 2: USART receiver, I2C data I/O, SPI master-out/slave-in data.
							O	**SCT0_OUT1 —** SCTimer/PWM output 1.
								R — Reserved.
								R — Reserved.
							I/O	**FC3_SSEL3 —** Flexcomm 3: SPI slave select 3.
							O	**EMC_A[12] —** External memory interface address 12.
PIO1_25	G10	M12	119	59	[2]	PU; Z	I/O	**PIO1_25 —** General-purpose digital input/output pin.
							I/O	**FC2_TXD_SCL_MISO —** Flexcomm 2: USART transmitter, I2C clock, SPI master-in/slave-out data.
							O	**SCT0_OUT2 —** SCTimer/PWM output 2.
								R — Reserved.
							I	**UTICK_CAP0 —** Micro-tick timer capture input 0.
								R — Reserved.
							O	**EMC_A[13] —** External memory interface address 13.
PIO1_26	E8	J10	131	63	[2]	PU; Z	I/O	**PIO1_26 —** General-purpose digital input/output pin.
							I/O	**FC2_CTS_SDA_SSEL0 —** Flexcomm 2: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							O	**SCT0_OUT3 —** SCTimer/PWM output 3.
							I	**CT0_CAP3 —** Capture 3 input to Timer 0.
							I	**UTICK_CAP1 —** Micro-tick timer capture input 1.
								R — Reserved.
							O	**EMC_A[8] —** External memory interface address 8.
PIO1_27	D8	F10	142	68	[2]	PU; Z	I/O	**PIO1_27 —** General-purpose digital input/output pin.
							I/O	**FC2_RTS_SCL_SSEL1 —** Flexcomm 2: USART request-to-send, I2C clock, SPI slave select 1.
							I/O	**SD_D[4] —** SD/MMC data 4.
							O	**CT0_MAT3 —** Match output 3 from Timer 0.
							O	**CLKOUT —** Output of the CLKOUT function.
								R — Reserved.
							O	**EMC_A[9] —** External memory interface address 9.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state[1] [9]	Type	Description
PIO4_5	-	E10	154	-	[2]	PU; Z	I/O	**PIO4_5 —** General-purpose digital input/output pin.
								R — Reserved.
							I/O	**FC9_CTS_SDA_SSEL0 —** Flexcomm 9: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							I/O	**FC0_CTS_SDA_SSEL0 —** Flexcomm 0: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							O	**CT4_MAT3 —** Match output 3 from Timer 4.
							I	**SCT0_GPI6 —** Pin input 6 to SCTimer/PWM.
							O	**EMC_CKE[2] —** External memory interface SDRAM clock enable 2.
PIO4_6	-	D10	161	-	[2]	PU; Z	I/O	**PIO4_6 —** General-purpose digital input/output pin.
								R — Reserved.
							I/O	**FC9_RTS_SCL_SSEL1 —** Flexcomm 9: USART request-to-send, I2C clock, SPI slave select 1.
								R — Reserved.
								R — Reserved.
							I	**SCT0_GPI7 —** Pin input 7 to SCTimer/PWM.
							O	**EMC_CKE[3] —** External memory interface SDRAM clock enable 3.
PIO4_7	-	A14	166	-	[2][8]	PU; Z	I/O	**PIO4_7 —** General-purpose digital input/output pin.
								R — Reserved.
							I	**CT4_CAP3 —** Capture input 3 to Timer 4.
							O	**USB0_PORTPWRN —** USB0 VBUS drive indicator (Indicates VBUS must be driven).
							O	**USB0_FRAME —** USB0 frame toggle signal.
							I	**SCT0_GPI0 —** Pin input 0 to SCTimer/PWM.
PIO4_8	-	B14	170	-	[2]	PU; Z	I/O	**PIO4_8 —** General-purpose digital input/output pin.
							O	**ENET_TXD0 —** Ethernet transmit data 0.
							I/O	**FC2_SCK —** Flexcomm 2: USART or SPI clock.
							I	**USB0_OVERCURRENTN —** USB0 bus overcurrent indicator (active low).
							O	**USB0_LEDN —** USB0-configured LED indicator (active low).
							I	**SCT0_GPI1 —** Pin input 1 to SCTimer/PWM.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state[1] [9]	Type	Description
PIO4_27	-	-	85	-	[2]	PU; Z	I/O	**PIO4_27 —** General-purpose digital input/output pin.
							O	**ENET_TX_EN —** Ethernet transmit enable (RMII/MII interface).
							I/O	**SD_D[2] —** SD/MMC data 2.
								R — Reserved.
							I/O	**FC1_SCK —** Flexcomm 1: USART or SPI clock.
							I	**CT1_CAP0 —** Capture input 0 to Timer 1.
							I/O	**EMC_D[22] —** External Memory interface data [22].
PIO4_28	-	-	92	-	[2]	PU; Z	I/O	**PIO4_28 —** General-purpose digital input/output pin.
							O	**ENET_TX_ER —** Ethernet Transmit Error (MII interface).
							I/O	**SD_D[3] —** SD/MMC data 3.
								R — Reserved.
							I/O	**FC1_RXD_SDA_MOSI —** Flexcomm 1: USART receiver, I2C data I/O, SPI master-out/slave-in data.
							I	**CT1_CAP1 —** Capture 1 input to Timer 1.
							I/O	**EMC_D[23] —** External Memory interface data [23].
PIO4_29	-	-	102	-	[2]	PU; Z	I/O	**PIO4_29 —** General-purpose digital input/output pin.
							I	**ENET_RX_ER —** Ethernet receive error (RMII/MII interface).
							I/O	**SD_D[4] —** SD/MMC data 4.
								R — Reserved.
							I/O	**FC1_TXD_SCL_MISO —** Flexcomm 1: USART transmitter, I2C clock, SPI master-in/slave-out data.
							I	**CT1_CAP2 —** Capture 2 input to Timer 1.
							I/O	**EMC_D[24] —** External Memory interface data [24].
PIO4_30	-	-	80	-	[2]	PU; Z	I/O	**PIO4_30 —** General-purpose digital input/output pin.
							I	**ENET_TX_CLK —** Ethernet Transmit Clock (MII interface).
							I/O	**SD_D[5] —** SD/MMC data 5.
							O	**CT3_MAT0 —** Match output 0 from Timer 3.
							I/O	**FC1_RTS_SCL_SSEL1 —** Flexcomm 1: USART request-to-send, I2C clock, SPI slave select 1.
							I	**CT1_CAP3 —** Capture 3 input to Timer 1.
							I/O	**EMC_D[25] —** External Memory interface data [25].

[1] PU = input mode, pull-up enabled (pull-up resistor pulls up pin to V_{DD}). Z = high impedance; pull-up or pull-down disabled, AI = analog input, I = input, O = output, F = floating. Reset state reflects the pin state at reset without boot code operation. For pin states in the different power modes, see Section 6.2.2 “Pin states in different power modes”. For termination on unused pins, see Section 6.2.1 “Termination of unused pins”.

[2] 5 V tolerant pad with programmable glitch filter (5 V tolerant if V_{DD} present; if V_{DD} not present, do not exceed 3.6 V); provides digital I/O functions with TTL levels and hysteresis; normal drive strength. See Figure 45. Pulse width of spikes or glitches suppressed by input filter is from 3 ns to 16 ns (simulated value).

[3] True open-drain pin. I2C-bus pins compliant with the I2C-bus specification for I2C standard mode, I2C Fast-mode, and I2C Fast-mode Plus. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I2C lines. Open-drain configuration applies to all functions on this pin.

[4] 5 V tolerant pin providing standard digital I/O functions with configurable modes, configurable hysteresis, and analog input. When configured as an analog input, the digital section of the pin is disabled, and the pin is not 5 V tolerant.

[5] Reset pad.5 V tolerant pad with glitch filter with hysteresis. Pulse width of spikes or glitches suppressed by input filter is from 3 ns to 20 ns (simulated value)

[6] 5 V tolerant transparent analog pad.

[7] The oscillator input pin (XTALIN) cannot be driven by an external clock. Must connect a crystal between XTALIN and XTALOUT.

[8] VBUS must be connected to supply voltage when using the USB peripheral.

[9] For initial device revision 0A (Boot ROM version 21.0), PU = input mode, pull-up enabled (pull-up resistor pulls up pin to VDD). For future device revision 1B (Boot ROM version 21.1), Z = high impedance; pull-up or pull-down disabled. See the Errata sheet LPC540xx (IOCON.1) for more details. For future device revision 1B (Boot ROM version 21.1), GPIO pins PIO0_12, PIO0_11, PIO0_2, PIO0_3, PIO0_4, PIO0_5, and PIO0_6 have the input buffer enabled (DIGIMODE, bit 8 is enabled in IOCON register) and will be floating by default. If unused, it is recommended to externally terminate this pins to prevent leakage.

6.2.1 Termination of unused pins

Table 5 shows how to terminate pins that are **not** used in the application. In many cases, unused pins should be connected externally or configured correctly by software to minimize the overall power consumption of the part.

Unused pins with GPIO function should be configured as outputs set to LOW with their internal pull-up disabled. To configure a GPIO pin as output and drive it LOW, select the GPIO function in the IOCON register, select output in the GPIO DIR register, and write a 0 to the GPIO PORT register for that pin. Disable the pull-up in the pin’s IOCON register.

In addition, it is recommended to configure all GPIO pins that are not bonded out on smaller packages as outputs driven LOW with their internal pull-up disabled.

Table 5. Termination of unused pins

Pin	Default state[1][2]	Recommended termination of unused pins
$\overline{\text{RESET}}$	I; PU	The $\overline{\text{RESET}}$ pin can be left unconnected if the application does not use it.
all PIOn_m (not open-drain)	I; PU; Z	Can be left unconnected if driven LOW and configured as GPIO output with pull-up disabled by software.
PIOn_m (I2C open-drain)	IA	Can be left unconnected if driven LOW and configured as GPIO output by software.
RTCXIN	-	Connect to ground. When grounded, the RTC oscillator is disabled.
RTCXOUT	-	Can be left unconnected.
XTALIN	-	Connect to ground. When grounded, the RTC oscillator is disabled.
XTALOUT	-	Can be left unconnected.
VREFP	-	Tie to VDD.
VREFN	-	Tie to VSS.
VDDA	-	Tie to VDD.
VSSA	-	Tie to VSS.

7.9 Memory mapping

The LPC540xx incorporates several distinct memory regions. The APB peripheral area is 512 kB in size and is divided to allow for up to 32 peripherals.Each peripheral is allocated 4 kB of space simplifying the address decoding. The registers incorporated into the CPU, such as NVIC, SysTick, and sleep mode control, are located on the private peripheral bus.

The ARM Cortex-M4 processor has a single 4 GB address space. The following table shows how this space is used on the LPC540xx.

Table 7. Memory usage and details

Address range	General Use	Address range details and description	
0x0000 0000 to 0x1FFF FFFF	SRAMX	0x0000 0000 - 0x0002 FFFF	I&D SRAM bank (192 kB).
	Boot ROM	0x0300 0000 - 0x0300 FFFF	Boot ROM with API services in a 64 kB space.
	SPI Flash Interface (SPIFI)	0x1000 0000 - 0x17FF FFFF	SPIFI memory mapped access space (128 MB).
0x2000 0000 to 0x3FFF FFFF	Main SRAM Banks	0x2000 0000 - 0x2002 7FFF	SRAM0, SRAM1, SRAM2, SRAM3 banks (Total 160 kB).
	SRAM bit band alias addressing	0x2200 0000 - 0x23FF FFFF	SRAM bit band alias addressing (32 MB).
	SRAM Bank	0x4010 0000 0x4010 2000	USB SRAM (8 kB).
0x4000 0000 to 0x7FFF FFFF	APB peripherals	0x4000 0000 - 0x4001 FFFF	APB slave group 0 up to 32 peripheral blocks of 4 kB each (128 kB).
		0x4002 0000 - 0x4003 FFFF	APB slave group 1 up to 32 peripheral blocks of 4 kB each (128 kB).
		0x4004 0000 - 0x4005 FFFF	APB asynchronous slave group 2 up to 32 peripheral blocks of 4 kB each (128 kB).
	AHB peripherals	0x4008 0000 - 0x400B FFFF	AHB peripherals (256 kB).
	Peripheral bit band alias addressing	0x4200 0000 - 0x43FF FFFF	Peripheral bit band alias addressing (32 MB).

Table 7. Memory usage and details *…continued*

Address range	General Use	Address range details and description	
0x8000 0000 to 0xDFFF FFFF	Off-chip Memory via the External Memory Controller	Four static memory chip selects:	
		0x8000 0000 - 0x83FF FFFF	Static memory chip select 0 (up to 64 MB)[1]
		0x8800 0000 - 0x8BFF FFFF	Static memory chip select 1 (up to 64 MB)[2]
		0x9000 0000 – 0x93FF FFFF	Static memory chip select 2 (up to 64 MB).
		0x9800 0000 - 0x9BFF FFFF	Static memory chip select 3 (up to 64 MB).
		Four dynamic memory chip selects:	
		0xA000 0000 - 0xA7FF FFFF	Dynamic memory chip select 0 (up to 256 MB).
		0xA800 0000 - 0xAFFF FFFF	Dynamic memory chip select 1 (up to 256 MB).
		0xB000 0000 - 0xB7FF FFFF	Dynamic memory chip select 2 (up to 256 MB).
		0xB800 0000 - 0xBFFF FFFF	Dynamic memory chip select 3 (up to 256 MB).
0xE000 0000 to 0xE00F FFFF	Cortex-M4 Private Peripheral Bus	0xE000 0000 - 0xE00F FFFF	Cortex-M4 related functions, includes the NVIC and System Tick Timer.

[1] Can be up to 256 MB, upper address 0x8FFF FFFF, if the address shift mode is enabled. See the EMCSYSCTRL register bit 0 in the *LPC540xx user manual*.

[2] Can be up to 128 MB, upper address 0x97FF FFFF, if the address shift mode is enabled. See the EMCSYSCTRL register bit 0 in the *LPC540xx user manual*.

Figure 9 shows the overall map of the entire address space from the user program viewpoint following reset.

signals, and are configured together for either transmit or receive operation, using the same mode, same data configuration and frame configuration. All such channel pairs can participate in a time division multiplexing (TDM) arrangement. For cases requiring an MCLK input and/or output, this is handled outside of the I^2S block in the system level clocking scheme.

Features

- A Flexcomm Interface may implement one or more I^2S channel pairs, the first of which could be a master or a slave, and the rest of which would be slaves. All channel pairs are configured together for either transmit or receive and other shared attributes. The number of channel pairs is defined for each Flexcomm Interface, and may be from 0 to 4.
- Configurable data size for all channels within one Flexcomm Interface, from 4 bits to 32 bits. Each channel pair can also be configured independently to act as a single channel (mono as opposed to stereo operation).
- All channel pairs within one Flexcomm Interface share a single bit clock (SCK) and word select/frame trigger (WS), and data line (SDA).
- Data for all I^2S traffic within one Flexcomm Interface uses the Flexcomm Interface FIFO. The FIFO depth is 8 entries.
- Left justified and right justified data modes.
- DMA support using FIFO level triggering.
- TDM (Time Division Multiplexing) with a several stereo slots and/or mono slots is supported. Each channel pair can act as any data slot. Multiple channel pairs can participate as different slots on one TDM data line.
- The bit clock and WS can be selectively inverted.
- Sampling frequencies supported depends on the specific device configuration and applications constraints (for example, system clock frequency and PLL availability.) but generally supports standard audio data rates.

Remark: The Flexcomm Interface function clock frequency should not be above 48 MHz.

7.15 Digital peripheral

7.15.1 LCD controller

The LCD controller provides all of the necessary control signals to interface directly to various color and monochrome LCD panels. Both STN (single and dual panel) and TFT panels can be operated. The display resolution is selectable and can be up to 1024 × 768 pixels. Several color modes are provided, up to a 24-bit true-color non-palettized mode. An on-chip 512 byte color palette allows reducing bus utilization (that is, memory size of the displayed data) while still supporting many colors.

The LCD interface includes its own DMA controller to allow it to operate independently of the CPU and other system functions. A built-in FIFO acts as a buffer for display data, providing flexibility for system timing. Hardware cursor support can further reduce the amount of CPU time required to operate the display.

7.15.1.1 Features

- AHB master interface to access frame buffer.

- 8 inputs
- 10 outputs
- 16 match/capture registers
- 16 events
- 16 states

- PWM capabilities including dead time and emergency abort functions

7.16.3 Windowed WatchDog Timer (WWDT)

The purpose of the watchdog is to reset the controller if software fails to periodically service it within a programmable time window.

7.16.3.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.
- Optional warning interrupt can be generated at a programmable time prior to watchdog time-out.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect feed sequence causes reset or interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The Watchdog Clock (WDCLK) uses the WDOSC as the clock source.

7.16.4 Real Time Clock (RTC) timer

The RTC timer is a 32-bit timer which counts down from a preset value to zero. At zero, the preset value is reloaded and the counter continues. The RTC timer uses the 32.768 kHz clock input to create a 1 Hz or 1 kHz clock.

7.16.5 Multi-Rate Timer (MRT)

The Multi-Rate Timer (MRT) provides a repetitive interrupt timer with four channels. Each channel can be programmed with an independent time interval, and each channel operates independently from the other channels.

7.16.5.1 Features

- 24-bit interrupt timer.
- Four channels independently counting down from individually set values.
- Repeat and one-shot interrupt modes.

Table 16. Static characteristics: Power consumption in deep-sleep and deep power-down modes

T_{amb} = −40 °C to +105 °C, unless otherwise specified, 2.2 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ[1][2]	Max[3]	Unit
I_{DD}	supply current	Deep-sleep mode:					
		SRAMX (64 KB) powered T_{amb} = 25 °C		-	55	175	μA
		SRAMX (64 KB) powered T_{amb} = 105 °C		-	-	2020	μA
		Deep power-down mode					
		RTC oscillator input grounded (RTC oscillator disabled) *T_{amb} = 25 °C*		-	891	1.6	μA
		RTC oscillator input grounded (RTC oscillator disabled) *T_{amb} = 105 °C*		-	-	42	μA
		RTC oscillator running with external crystal VDD = VDDA= VREFP = 3.3 V, VBAT = 3.0 V		-	660	-	nA

[1] Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C), VDD = 3.3 V.

[2] Characterized through bench measurements using typical samples.

[3] Tested in production, VDD = 3.6 V.

Table 17. Static characteristics: Power consumption in deep power-down mode

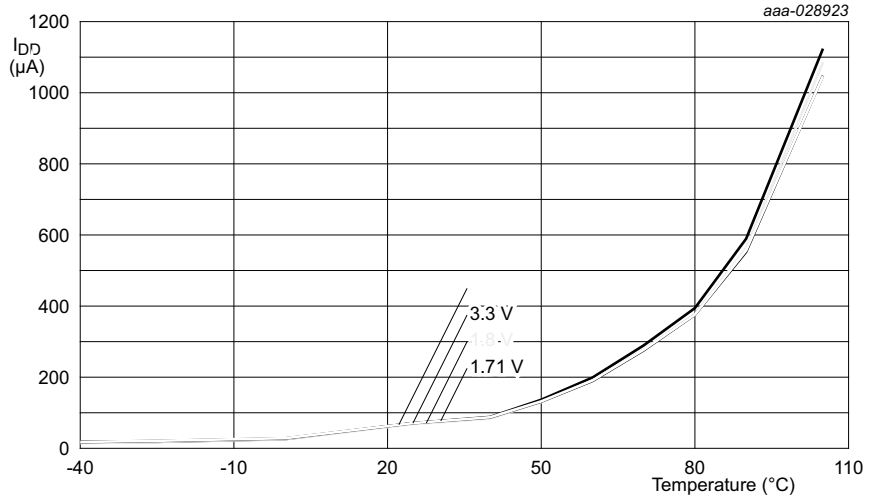
T_{amb} = −40 °C to +105 °C, unless otherwise specified, 2.7 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ[1][2]	Max	Unit
I_{BAT}	battery supply current	deep power-down mode; RTC oscillator running with external crystal					
		VDD = VDDA= VREFP = 3.3 V, VBAT = 3.0 V		-	0	-	nA
		VDD = VDDA= VREFP = 0 V or tied to ground, VBAT = 3.0 V		-	380[3]	-	nA

[1] Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C).

[2] Characterized through bench measurements using typical samples.

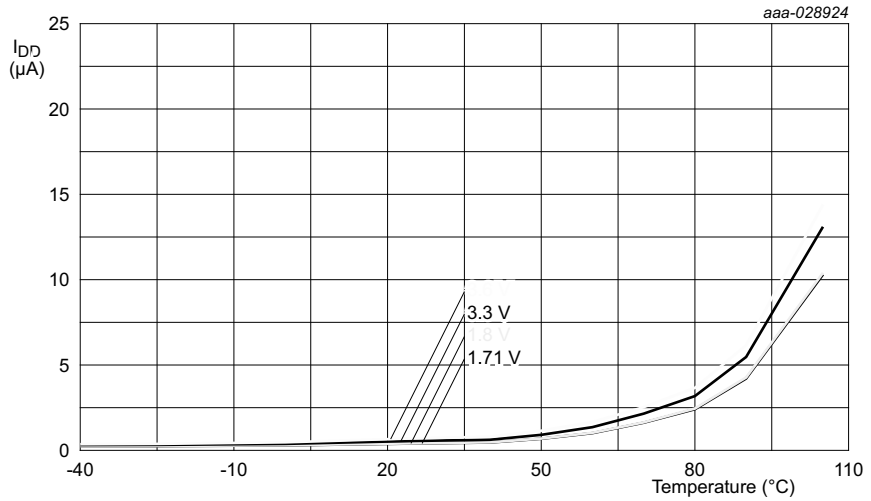
[3] If VBAT> VDD, the external reset pin must be floating to prevent high VBAT leakage.



Conditions: BOD disabled; all oscillators and analog blocks disabled; all SRAM disabled except 64 KB SRAMX.

Remark: At hot temperature and below 2.0 V, the supply current increases slightly because of reduction of available RBB (reverse body bias) voltage.

Fig 15. Deep-sleep mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}



RTC disabled (RTC oscillator input grounded).

Fig 16. Deep power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}

Table 18 shows the typical peripheral power consumption measured on a typical sample at Tamb = 25 °C and VDD = 3.3 V. The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled using ASYNCAPBCLKCTRL, AHBCLKCTRL0/1/2, and PDRUNCFG0/1

Table 33. Dynamic characteristics of the PLL2[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Reference clock input							
F_{in}	input frequency			1	-	25	MHz
Clock output							
f_o	output frequency	for PLL2 clkout output	[2]	4.3	-	550	MHz
d_o	output duty cycle	for PLL2 clkout output		46	-	54	%
f_{CCO}	CCO frequency			275	-	550	MHz
Lock detector output							
$\Delta_{lock(PFD)}$	PFD lock criterion		[3]	1	2	4	ns
Dynamic parameters at $f_{out} = f_{CCO}$ = 540 MHz; standard bandwidth settings							
$J_{rms\text{-}interval}$	RMS interval jitter	f_{ref} = 10 MHz	[4][5]	-	15	30	ps
$J_{pp\text{-}period}$	peak-to-peak, period jitter	f_{ref} = 10 MHz	[4][5]	-	40	80	ps

[1] Data based on characterization results, not tested in production.

[2] Excluding under- and overshoot which may occur when the PLL is not in lock.

[3] A phase difference between the inputs of the PFD (clkref and clkfb) smaller than the PFD lock criterion means lock output is HIGH.

[4] Actual jitter dependent on amplitude and spectrum of substrate noise.

[5] Input clock coming from a crystal oscillator with less than 250 ps peak-to-peak period jitter.

11.7 FRO

The FRO is trimmed to ±1 % accuracy over the entire voltage and temperature range.

Table 34. Dynamic characteristic: FRO

T_{amb} = −40 °C to +105 °C; 1.71 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
$f_{osc(RC)}$	FRO clock frequency	-	11.88	12	12.12	MHz
$f_{osc(RC)}$	FRO clock frequency	-	47.52	48	48.48	MHz
$f_{osc(RC)}$	FRO clock frequency	-	95.04	96	96.96	MHz

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

11.8 Crystal oscillator

Table 35. Dynamic characteristic: oscillator

T_{amb} = −40 °C to +105 °C; 1.71 V ≤ V_{DD} ≤ 3.6 V.[1]

Symbol	Parameter	Conditions		Min	Typ[2]	Max	Unit
Low-frequency mode (1-20 MHz)[4]							
$t_{jit(per)}$	period jitter time	5 MHz crystal	[3]	-	13.2	-	ps
		10 MHz crystal		-	6.6	-	ps
		15 MHz crystal		-	4.8	-	ps

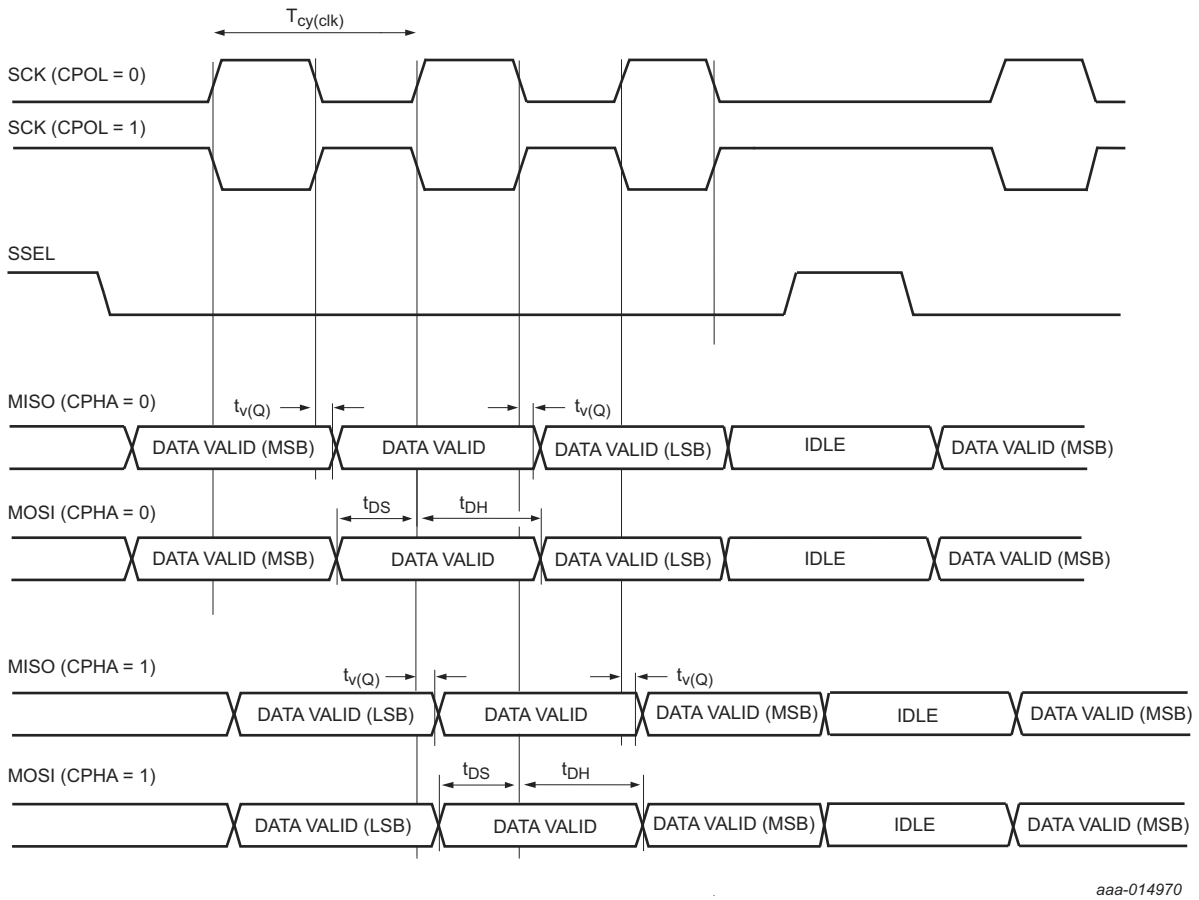


Fig 31. SPI slave timing

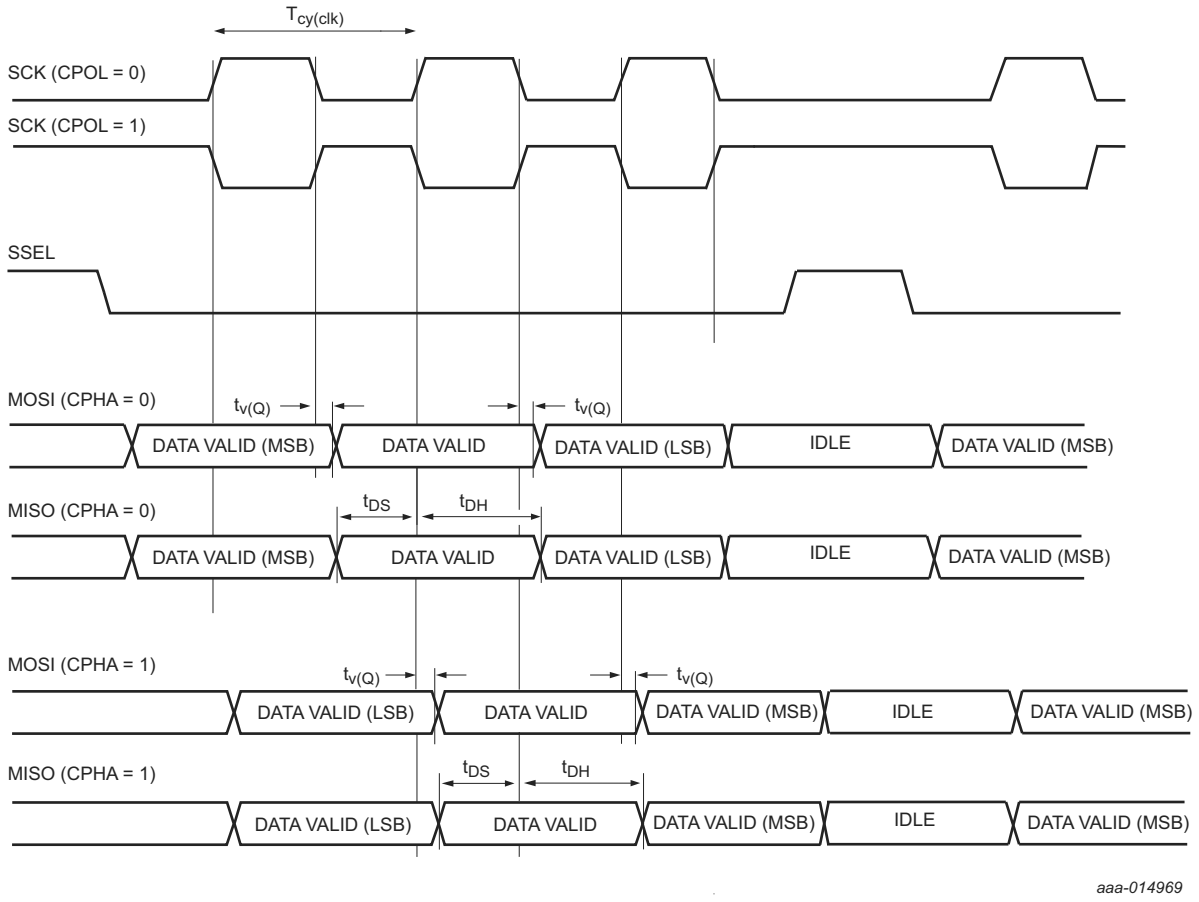


Fig 32. SPI master timing

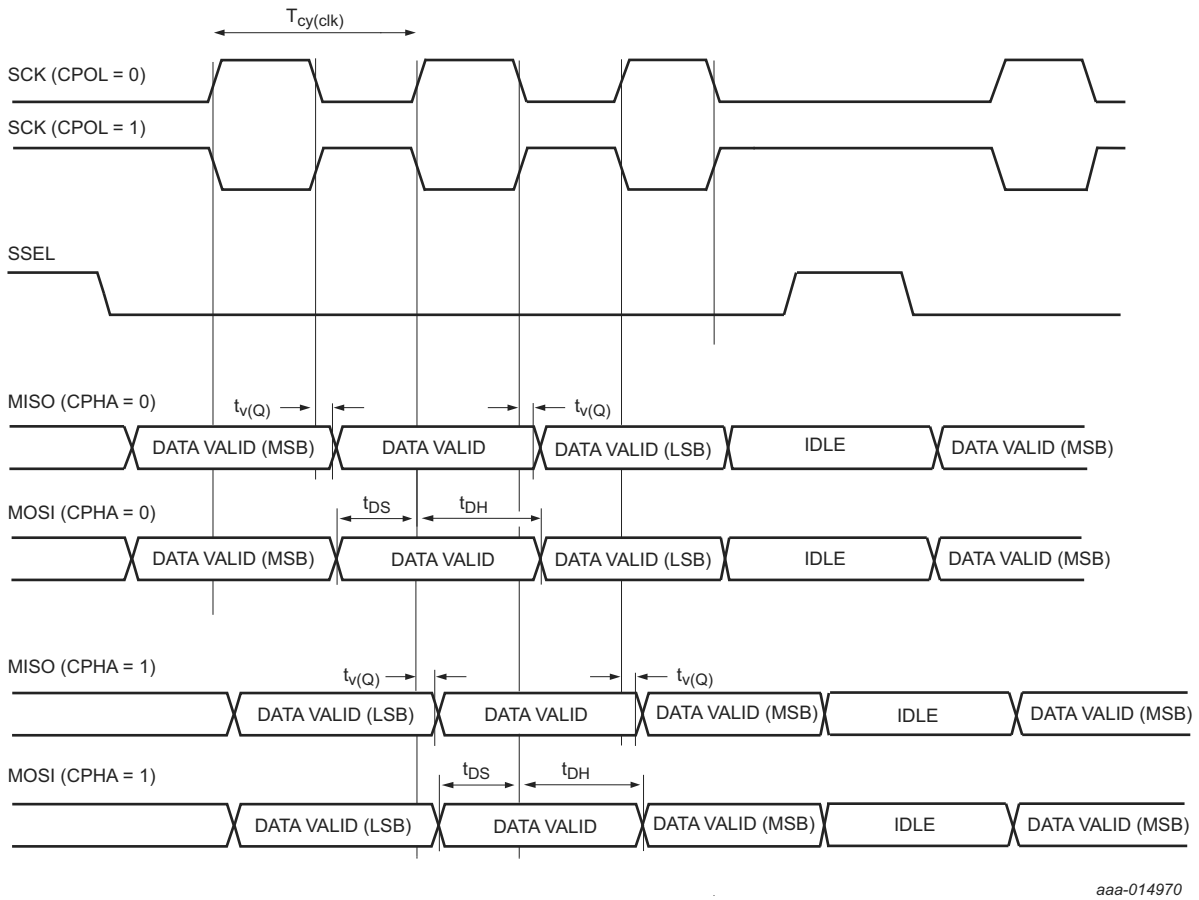
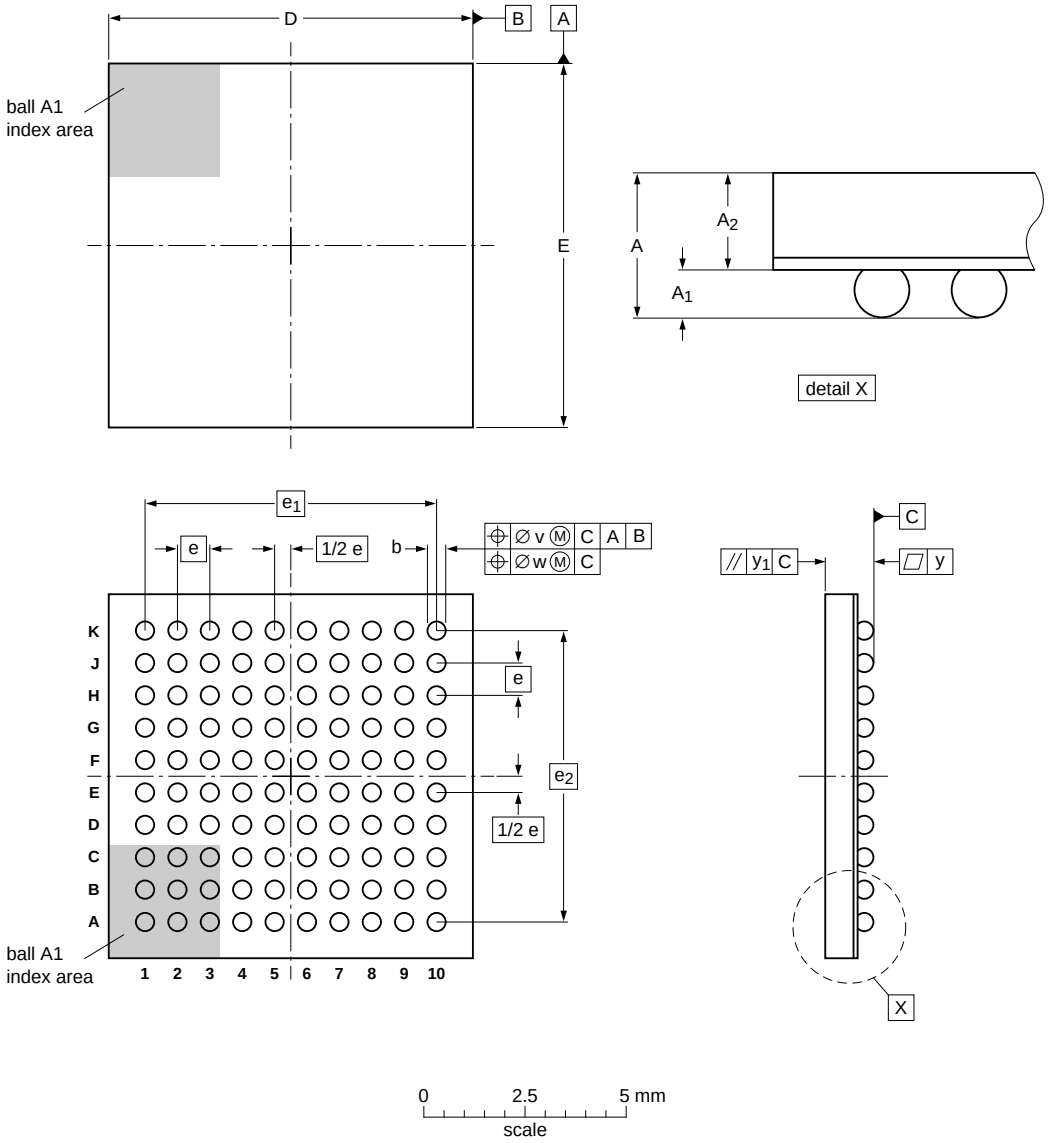


Fig 33. SPI slave timing

TFBGA100: plastic thin fine-pitch ball grid array package; 100 balls; body 9 x 9 x 0.7 mm **SOT926-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.2	0.4 0.3	0.8 0.65	0.5 0.4	9.1 8.9	9.1 8.9	0.8	7.2	7.2	0.15	0.05	0.08	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT926-1	- - -	- - -	- - -			~~05-12-09~~ 05-12-22

Fig 54. TFBGA100 package