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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	-
Core Size	-
Speed	-
Connectivity	-
Peripherals	-
Number of I/O	-
Program Memory Size	-
Program Memory Type	-
EEPROM Size	-
RAM Size	-
Voltage - Supply (Vcc/Vdd)	-
Data Converters	-
Oscillator Type	-
Operating Temperature	-
Mounting Type	-
Package / Case	-
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc54016jet180e

4. Marking

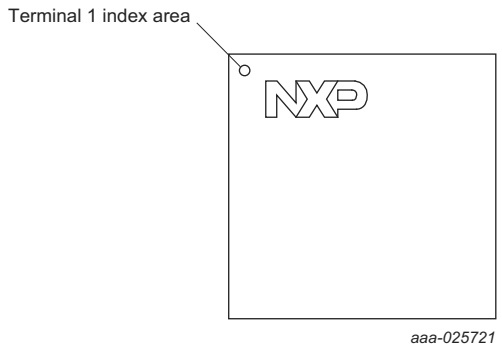


Fig 1. TFBGA180 and TFBGA 100 package markings

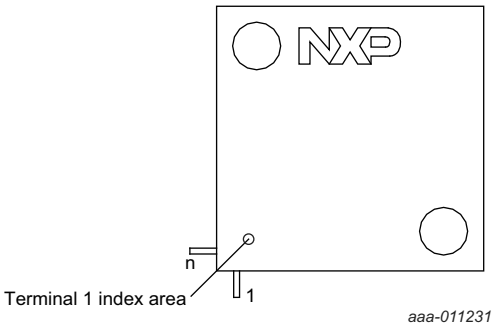


Fig 2. LQFP208 package marking

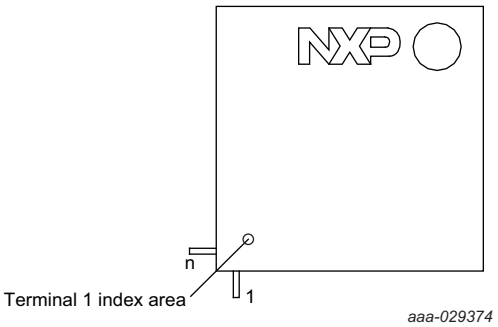


Fig 3. LQFP100 package marking

The LPC540xx TFBGA180 and TFBGA100 packages have the following top-side marking:

- First line: LPC540xxJ
- Second line: ET180 or ET100
- Third line: xxxxxxxxxxxx
- Fourth line: xxxyywwx[R]x
  - yyww: Date code with yy = year and ww = week.
  - xR = boot code version and device revision.

The LPC540xx LQFP208 and LQFP100 packages have the following top-side marking:

- First line: LPC540xxJ
- Second line: BD208 or BD100
- Third line: xxxxxxxxxxxx
- Fourth line: xxxyywwx[R]x
  - yyww: Date code with yy = year and ww = week.
  - xR = Boot code version and device revision.

Table 3. Device revision table

Revision identifier (R)	Revision description
0A	Initial device revision with Boot ROM version 21.0

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state[1] [9]	Type	Description
PIO0_3/ TCK	A6	A10	178	85	[2]	PU; Z	I/O	**PIO0_3 —** General-purpose digital input/output pin. In boundary scan mode: TCK (Test Clock In). **Remark:** In ISP mode, this pin is set to the Flexcomm 3 SPI MOSI function.
							I/O	**FC3_RXD_SDA_MOSI —** Flexcomm 3: USART receiver, I2C data I/O, SPI master-out/slave-in data.
							O	**CT0_MAT1 —** Match output 1 from Timer 0.
							O	**SCT0_OUT1 —** SCTimer/PWM output 1.
							I	**SCT0_GPI3 —** Pin input 3 to SCTimer/PWM.
								R — Reserved.
							I/O	**EMC_D[1] —** External Memory interface data [1].
PIO0_4/ TMS	B6	C8	185	87	[2]	PU; Z	I/O	**PIO0_4 —** General-purpose digital input/output pin. In boundary scan mode: TMS (Test Mode Select). **Remark:** The state of this pin at Reset in conjunction with PIO0_5 and PIO0_6 will determine the boot source for the part or if ISP handler is invoked. See the Boot Process chapter in UM11060 for more details.
							I	**CAN0_RD —** Receiver input for CAN 0.
							I/O	**FC4_SCK —** Flexcomm 4: USART or SPI clock.
							I	**CT3_CAP0 —** Capture input 0 to Timer 3.
							I	**SCT0_GPI4 —** Pin input 4 to SCTimer/PWM.
								R — Reserved.
							I/O	**EMC_D[2] —** External Memory interface data [2].
							O	**ENET_MDC —** Ethernet management data clock.
PIO0_5/ TDI	A5	E7	189	89	[2]	PU; Z	I/O	**PIO0_5 —** General-purpose digital input/output pin. In boundary scan mode: TDI (Test Data In). **Remark:** The state of this pin at Reset in conjunction with PIO0_4 and PIO0_6 will determine the boot source for the part or if ISP handler is invoked. See the Boot Process chapter in UM11060 for more details.
							O	**CAN0_TD —** Transmitter output for CAN 0.
							I/O	**FC4_RXD_SDA_MOSI —** Flexcomm 4: USART receiver, I2C data I/O, SPI master-out/slave-in data.
							O	**CT3_MAT0 —** Match output 0 from Timer 3.
							I	**SCT0_GPI5 —** Pin input 5 to SCTimer/PWM.
								R — Reserved.
							I/O	**EMC_D[3] —** External Memory interface data [3].
							I/O	**ENET_MDIO —** Ethernet management data I/O.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state[1] [9]	Type	Description
PIO0_6/ TDO	A4	A5	191	90	[2]	PU; Z	I/O	**PIO0_6 —** General-purpose digital input/output pin. In boundary scan mode: TDO (Test Data Out). **Remark:** The state of this pin at Reset in conjunction with PIO0_4 and PIO0_5 will determine the boot source for the part or if ISP handler is invoked. See the Boot Process chapter in UM11060 for more details.
							I/O	**FC3_SCK —** Flexcomm 3: USART or SPI clock.
							I	**CT3_CAP1 —** Capture input 1 to Timer 3.
							O	**CT4_MAT0 —** Match output 0 from Timer 4.
							I	**SCT0_GPI6 —** Pin input 6 to SCTimer/PWM.
								R — Reserved.
							I/O	**EMC_D[4] —** External Memory interface data [4].
							I	**ENET_RX_DV —** Ethernet receive data valid.
PIO0_7	F9	H12	125	61	[2]	PU; Z	I/O	**PIO0_7 —** General-purpose digital input/output pin.
							I/O	**FC3_RTS_SCL_SSEL1 —** Flexcomm 3: USART request-to-send, I2C clock, SPI slave select 1.
							O	**SD_CLK —** SD/MMC clock.
							I/O	**FC5_SCK —** Flexcomm 5: USART or SPI clock.
							I/O	**FC1_SCK —** Flexcomm 1: USART or SPI clock.
							O	**PDM1_CLK —** Clock for PDM interface 1, for digital microphone.
							I/O	**EMC_D[5] —** External Memory interface data [5].
							I	**ENET_RX_CLK —** Ethernet Receive Clock (MII interface) or Ethernet Reference Clock (RMII interface).
PIO0_8	E9	H10	133	64	[2]	PU; Z	I/O	**PIO0_8 —** General-purpose digital input/output pin.
							I/O	**FC3_SSEL3 —** Flexcomm 3: SPI slave select 3.
							I/O	**SD_CMD —** SD/MMC card command I/O.
							I/O	**FC5_RXD_SDA_MOSI —** Flexcomm 5: USART receiver, I2C data I/O, SPI master-out/slave-in data.
							O	**SWO —** Serial Wire Debug trace output.
							I	**PDM1_DATA —** Data for PDM interface 1 (digital microphone).
							I/O	**EMC_D[6] —** External Memory interface data [6].

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state[1] [9]	Type	Description
PIO0_22	B8	B12	163	80	[2][8]	PU; Z	I/O	**PIO0_22 —** General-purpose digital input/output pin.
							I/O	**FC6_TXD_SCL_MISO_WS —** Flexcomm 6: USART transmitter, I2C clock, SPI master-in/slave-out data I/O, I2S word-select/frame.
							I	**UTICK_CAP1 —** Micro-tick timer capture input 1.
							I	**CT3_CAP3 —** Capture input 3 to Timer 3.
							O	**SCT0_OUT3 —** SCTimer/PWM output 3.
								R — Reserved.
								R — Reserved.
							I	**USB0_VBUS —** Monitors the presence of USB0 bus power.
PIO0_23/ ADC0_11	K5	N7	71	35	[4]	PU; Z	I/O; AI	**PIO0_23/ADC0_11 —** General-purpose digital input/output pin. ADC input channel 11 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
							I/O	**MCLK —** MCLK input or output for I2S and/or digital microphone.
							O	**CT1_MAT2 —** Match output 2 from Timer 1.
							O	**CT3_MAT3 —** Match output 3 from Timer 3.
							O	**SCT0_OUT4 —** SCTimer/PWM output 4.
							I/O	**FC0_CTS_SDA_SSEL0 —** Flexcomm 0: USART clear-to-send, I2C data I/O, SPI slave select 0.
							I/O	**SPIFI_CSN —** SPI Flash Interface chip select (active low).
PIO0_24	J5	M7	76	38	[2]	PU; Z	I/O	**PIO0_24 —** General-purpose digital input/output pin.
							I/O	**FC0_RXD_SDA_MOSI —** Flexcomm 0: USART receiver, I2C data I/O, SPI master-out/slave-in data.
							I/O	**SD_D[0] —** SD/MMC data 0.
							I	**CT2_CAP0 —** Capture input 0 to Timer 2.
							I	**SCT0_GPI0 —** Pin input 0 to SCTimer/PWM.
								R — Reserved.
							I/O	**SPIFI_IO0 —** Data bit 0 for the SPI Flash Interface.
PIO0_25	J6	K8	83	40	[2]	PU; Z	I/O	**PIO0_25 —** General-purpose digital input/output pin.
							I/O	**FC0_TXD_SCL_MISO —** Flexcomm 0: USART transmitter, I2C clock, SPI master-in/slave-out data.
							I/O	**SD_D[1] —** SD/MMC data 1.
							I	**CT2_CAP1 —** Capture input 1 to Timer 2.
							I	**SCT0_GPI1 —** Pin input 1 to SCTimer/PWM.
								R — Reserved.
							I/O	**SPIFI_IO1 —** Data bit 1 for the SPI Flash Interface.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state[1] [9]	Type	Description
PIO1_12	F8	K9	128	62	[2]	PU; Z	I/O	**PIO1_12 —** General-purpose digital input/output pin.
							I	**ENET_RXD0 —** Ethernet receive data 0.
							I/O	**FC6_SCK —** Flexcomm 6: USART, SPI, or I2S clock.
							O	**CT1_MAT1 —** Match output 1 from Timer 1.
							O	**USB0_PORTPWRN —** USB0 VBUS drive indicator (Indicates VBUS must be driven).
							O	**EMC_DYCSN[0] —** External Memory interface SDRAM chip select 0 (active low).
PIO1_13	D10	G10	139	66	[2]	PU; Z	I/O	**PIO1_13 —** General-purpose digital input/output pin.
							I	**ENET_RXD1 —** Ethernet receive data 1.
							I/O	**FC6_RXD_SDA_MOSI_DATA —** Flexcomm 6: USART receiver, I2C data I/O, SPI master-out/slave-in data, I2S data I/O.
							I	**CT1_CAP2 —** Capture 2 input to Timer 1.
							I	**USB0_OVERCURRENTN —** USB0 bus overcurrent indicator (active low).
							O	**USB0_FRAME —** USB0 frame toggle signal.
							O	**EMC_DQM[0] —** External memory interface data mask 0.
PIO1_14	A9	C12	160	78	[2]	PU; Z	I/O	**PIO1_14 —** General-purpose digital input/output pin.
							I	**ENET_RX_DV —** Ethernet receive data valid.
							I	**UTICK_CAP2 —** Micro-tick timer capture input 2.
							O	**CT1_MAT2 —** Match output 2 from Timer 1.
							I/O	**FC5_CTS_SDA_SSEL0 —** Flexcomm 5: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							O	**USB0_LEDN —** USB0-configured LED indicator (active low).
							O	**EMC_DQM[1] —** External memory interface data mask 0.
PIO1_15	C7	A11	176	84	[2]	PU; Z	I/O	**PIO1_15 —** General-purpose digital input/output pin.
							I	**ENET_RX_CLK —** Ethernet Receive Clock (MII interface) or Ethernet Reference Clock (RMII interface).
							I	**UTICK_CAP3 —** Micro-tick timer capture input 3.
							I	**CT1_CAP3 —** Capture 3 input to Timer 1.
							I/O	**FC5_RTS_SCL_SSEL1 —** Flexcomm 5: USART request-to-send, I2C clock, SPI slave select 1.
							I/O	**FC4_RTS_SCL_SSEL1 —** Flexcomm 4: USART request-to-send, I2C clock, SPI slave select 1.
							O	**EMC_CKE[0] —** External memory interface SDRAM clock enable 0.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state[1] [9]	Type	Description
PIO1_24	G8	N14	111	57	[2]	PU; Z	I/O	**PIO1_24 —** General-purpose digital input/output pin.
							I/O	**FC2_RXD_SDA_MOSI —** Flexcomm 2: USART receiver, I2C data I/O, SPI master-out/slave-in data.
							O	**SCT0_OUT1 —** SCTimer/PWM output 1.
								R — Reserved.
								R — Reserved.
							I/O	**FC3_SSEL3 —** Flexcomm 3: SPI slave select 3.
							O	**EMC_A[12] —** External memory interface address 12.
PIO1_25	G10	M12	119	59	[2]	PU; Z	I/O	**PIO1_25 —** General-purpose digital input/output pin.
							I/O	**FC2_TXD_SCL_MISO —** Flexcomm 2: USART transmitter, I2C clock, SPI master-in/slave-out data.
							O	**SCT0_OUT2 —** SCTimer/PWM output 2.
								R — Reserved.
							I	**UTICK_CAP0 —** Micro-tick timer capture input 0.
								R — Reserved.
							O	**EMC_A[13] —** External memory interface address 13.
PIO1_26	E8	J10	131	63	[2]	PU; Z	I/O	**PIO1_26 —** General-purpose digital input/output pin.
							I/O	**FC2_CTS_SDA_SSEL0 —** Flexcomm 2: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							O	**SCT0_OUT3 —** SCTimer/PWM output 3.
							I	**CT0_CAP3 —** Capture 3 input to Timer 0.
							I	**UTICK_CAP1 —** Micro-tick timer capture input 1.
								R — Reserved.
							O	**EMC_A[8] —** External memory interface address 8.
PIO1_27	D8	F10	142	68	[2]	PU; Z	I/O	**PIO1_27 —** General-purpose digital input/output pin.
							I/O	**FC2_RTS_SCL_SSEL1 —** Flexcomm 2: USART request-to-send, I2C clock, SPI slave select 1.
							I/O	**SD_D[4] —** SD/MMC data 4.
							O	**CT0_MAT3 —** Match output 3 from Timer 0.
							O	**CLKOUT —** Output of the CLKOUT function.
								R — Reserved.
							O	**EMC_A[9] —** External memory interface address 9.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state[1] [9]	Type	Description
PIO3_29	-	L13	112	-	[2]	PU; Z	I/O	**PIO3_29 —** General-purpose digital input/output pin.
								R — Reserved.
							O	**SCT0_OUT3 —** SCTimer/PWM output 3.
							I/O	**FC4_RTS_SCL_SSEL1 —** Flexcomm 4: USART request-to-send, I2C clock, SPI slave select 1.
								R — Reserved.
								R — Reserved.
							O	**EMC_A[18] —** External memory interface address 18.
PIO3_30	-	K13	116	-	[2]	PU; Z	I/O	**PIO3_30 —** General-purpose digital input/output pin.
							I/O	**FC9_CTS_SDA_SSEL0 —** Flexcomm 9: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							O	**SCT0_OUT4 —** SCTimer/PWM output 4.
							I/O	**FC4_SSEL2 —** Flexcomm 4: SPI slave select 2.
								R — Reserved.
								R — Reserved.
							O	**EMC_A[19] —** External memory interface address 19.
PIO3_31	-	J14	123	-	[2]	PU; Z	I/O	**PIO3_31 —** General-purpose digital input/output pin.
							I/O	**FC9_RTS_SCL_SSEL1 —** Flexcomm 9: USART request-to-send, I2C clock, SPI slave select 1.
							O	**SCT0_OUT5 —** SCTimer/PWM output 5.
							O	**CT4_MAT2 —** Match output 2 from Timer 4.
								R — Reserved.
							I	**SCT0_GPI0 —** Pin input 0 to SCTimer/PWM.
							O	**EMC_A[20] —** External memory interface address 20.
PIO4_0	-	H13	127	-	[2]	PU; Z	I/O	**PIO4_0 —** General-purpose digital input/output pin.
								R — Reserved.
							I/O	**FC6_CTS_SDA_SSEL0 —** Flexcomm 6: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							I	**CT4_CAP1 —** Capture input 4 to Timer 1.
								R — Reserved.
							I	**SCT0_GPI1 —** Pin input 1 to SCTimer/PWM.
							O	**EMC_CSN[1] —** External memory interface static chip select 1(active low).

Table 8 shows the peripheral configuration in reduced power modes.

Table 8. Peripheral configuration in reduced power modes

Peripheral	Reduced power mode		
	Sleep	Deep-sleep	Deep power-down
FRO	Software configured	Software configured	Off
BOD	Software configured	Software configured	Off
PLL	Software configured	Off	Off
Watchdog osc and WWDT	Software configured	Software configured	Off
Micro-tick Timer	Software configured	Software configured	Off
DMA	Active	Configurable some for operations.	Off
USART	Software configured	Off; but can create a wake-up interrupt in synchronous slave mode or 32 kHz clock mode	Off
SPI	Software configured	Off; but can create a wake-up interrupt in slave mode	Off
I2C	Software configured	Off; but can create a wake-up interrupt in slave mode	Off
USB0	Software configured	Software configured	Off
USB1	Software configured	Software configured	Off
Ethernet	Software configured	Off	Off
DMIC	Software configured	Software configured	Off
Other digital peripherals	Software configured	Off	Off
RTC oscillator	Software configured	Software configured	Software configured

- Supports DMA access.
- Provides XIP (execute in place) feature to execute code directly from serial flash.

7.14.5 CAN Flexible Data (CAN FD) interface

The LPC540xx contains two CAN FD interfaces, CAN FD 1 and CAN FD 2.

7.14.5.1 Features

- Conforms with CAN protocol version 2.0 part A, B and ISO 11898-1.
- CAN FD with up to 64 data bytes supported.
- CAN Error Logging.
- AUTOSAR support.
- SAE J1939 support.
- Improved acceptance filtering.

7.14.6 DMIC subsystem

7.14.6.1 Features

- Pulse-Density Modulation (PDM) data input for left and/or right channels on 1 or 2 buses.
- Flexible decimation.
- 16 entry FIFO for each channel.
- DC blocking or unaltered DC bias can be selected.
- Data can be transferred using DMA from deep-sleep mode without waking up the CPU, then automatically returning to deep-sleep mode.
- Data can be streamed directly to I^2S on Flexcomm Interface 7.

7.14.7 Smart card interface

7.14.7.1 Features

- Two DMA supported ISO 7816 Smart Card Interfaces.
- Both asynchronous protocols, T = 0 and T = 1 are supported.

7.14.8 Flexcomm Interface serial communication

7.14.8.1 Features

- USART with asynchronous operation or synchronous master or slave operation.
- SPI master or slave, with up to 4 slave selects.
- I^2C, including separate master, slave, and monitor functions.
- Two I2S functions using Flexcomm Interface 6 and Flexcomm Interface 7.
- Data for USART, SPI, and I2S traffic uses the Flexcomm Interface FIFO. The I^2C function does not use the FIFO.

Table 25. Dynamic characteristics: Dynamic external memory interface, read strategy bits (RD bits) = 01 [2]

C_L = 10 pF balanced loading on all pins, T_{amb} = −40 °C to 105 °C, V_{DD} = 2.7 V to 3.6 V. Max EMC clock = 100 MHz. Input slew = 1 ns; SLEW set to fast-mode. Parameters sampled at the 90 % and 10 % level of the rising or falling edge. Excluding delays introduced by external device and PCB. Values based on simulation. t_{cmddly} is programmable delay value for EMC command outputs in command delayed mode; t_{fbdly} is programmable delay value for the feedback clock that controls input data sampling.

Symbol	Parameter		Min	Typ	Max	Unit
For RD = 1						
Common to read and write cycles						
$T_{cy(clk)}$	clock cycle time	[1]	10	-	-	ns
$t_{d(SV)}$	chip select valid delay time		-	-	t_{cmddly} + 3.7	ns
$t_{h(S)}$	chip select hold time		t_{cmddly} + 1.7	-	-	ns
$t_{d(RASV)}$	row address strobe valid delay time		-	-	t_{cmddly} + 4.1	ns
$t_{h(RAS)}$	row address strobe hold time		t_{cmddly} + 1.8	-	-	ns
$t_{d(CASV)}$	column address strobe valid delay time		-	-	t_{cmddly} + 4.4	ns
$t_{h(CAS)}$	column address strobe hold time		t_{cmddly} + 1.9	-	-	ns
$t_{d(WV)}$	write valid delay time		-	-	t_{cmddly} + 5.1	ns
$t_{h(W)}$	write hold time		t_{cmddly} + 2.4	-	-	ns
$t_{d(AV)}$	address valid delay time		-	-	t_{cmddly} + 4.8	ns
$t_{h(A)}$	address hold time		t_{cmddly} + 1.7	-	-	ns
Read cycle parameters						
$t_{su(D)}$	data input set-up time		0.5	-	-	ns
$t_{h(D)}$	data input hold time		2.1	-	-	ns
Write cycle parameters						
$t_{d(QV)}$	data output valid delay time		-	-	8.1	ns
$t_{h(Q)}$	data output hold time		−1.7	-	-	ns

[1] Refers to SDRAM clock signal EMC_CLKOUTn where n = 0 and 1.

[2] See Table 27 for internal programmable delay.

Table 26. Dynamic characteristics: Dynamic external memory interface, read strategy bits (RD bits) = 01 [2]

C_L = 20 pF balanced loading on all pins, T_{amb} = −40 °C to 105 °C, V_{DD} = 2.7 V to 3.6 V. Max EMC clock = 100 MHz. Input slew = 1 ns; SLEW set to fast-mode. Parameters sampled at the 90 % and 10 % level of the rising or falling edge. Excluding delays introduced by external device and PCB. Values based on simulation. t_{cmddly} is programmable delay value for EMC command outputs in command delayed mode; t_{fbdly} is programmable delay value for the feedback clock that controls input data sampling.

Symbol	Parameter		Min	Typ	Max	Unit
For RD = 1						
Common to read and write cycles						
$T_{cy(clk)}$	clock cycle time	[1]	10	-	-	ns
$t_{d(SV)}$	chip select valid delay time		-	-	t_{cmddly} + 4.9	ns
$t_{h(S)}$	chip select hold time		t_{cmddly} + 2.4	-	-	ns
$t_{d(RASV)}$	row address strobe valid delay time		-	-	t_{cmddly} + 5.4	ns
$t_{h(RAS)}$	row address strobe hold time		t_{cmddly} + 2.5	-	-	ns
$t_{d(CASV)}$	column address strobe valid delay time		-	-	t_{cmddly} + 5.6	ns
$t_{h(CAS)}$	column address strobe hold time		t_{cmddly} + 2.6	-	-	ns
$t_{d(WV)}$	write valid delay time		-	-	t_{cmddly} + 6.3	ns
$t_{h(W)}$	write hold time		t_{cmddly} + 3.1	-	-	ns
$t_{d(AV)}$	address valid delay time		-	-	t_{cmddly} + 6.1	ns
$t_{h(A)}$	address hold time		t_{cmddly} + 2.4	-	-	ns
Read cycle parameters						
$t_{su(D)}$	data input set-up time		0.5	-	-	ns
$t_{h(D)}$	data input hold time		2.1	-	-	ns
Write cycle parameters						
$t_{d(QV)}$	data output valid delay time		-	-	9.3	ns
$t_{h(Q)}$	data output hold time		−2.4	-	-	ns

[1] Refers to SDRAM clock signal EMC_CLKOUTn where n = 0 and 1.

[2] See Table 27 for internal programmable delay.

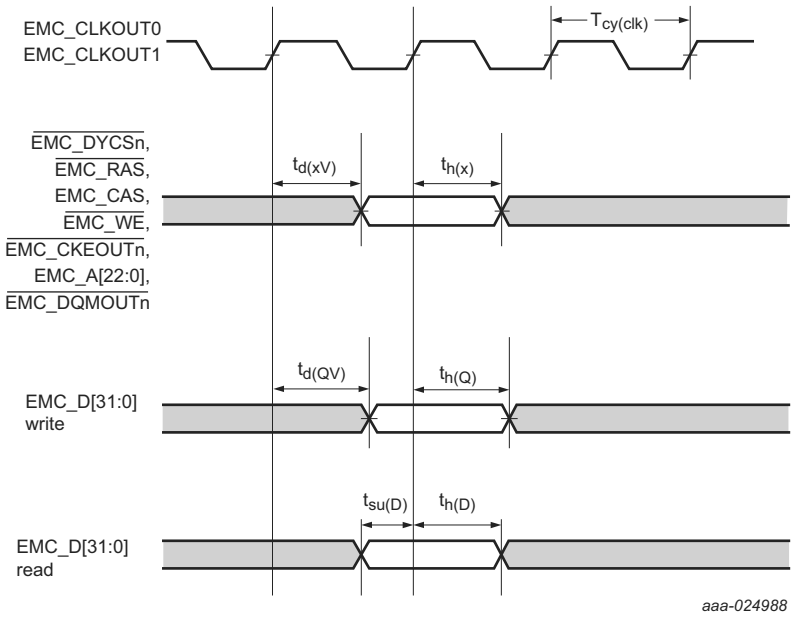


Fig 26. Dynamic external memory interface signal timing

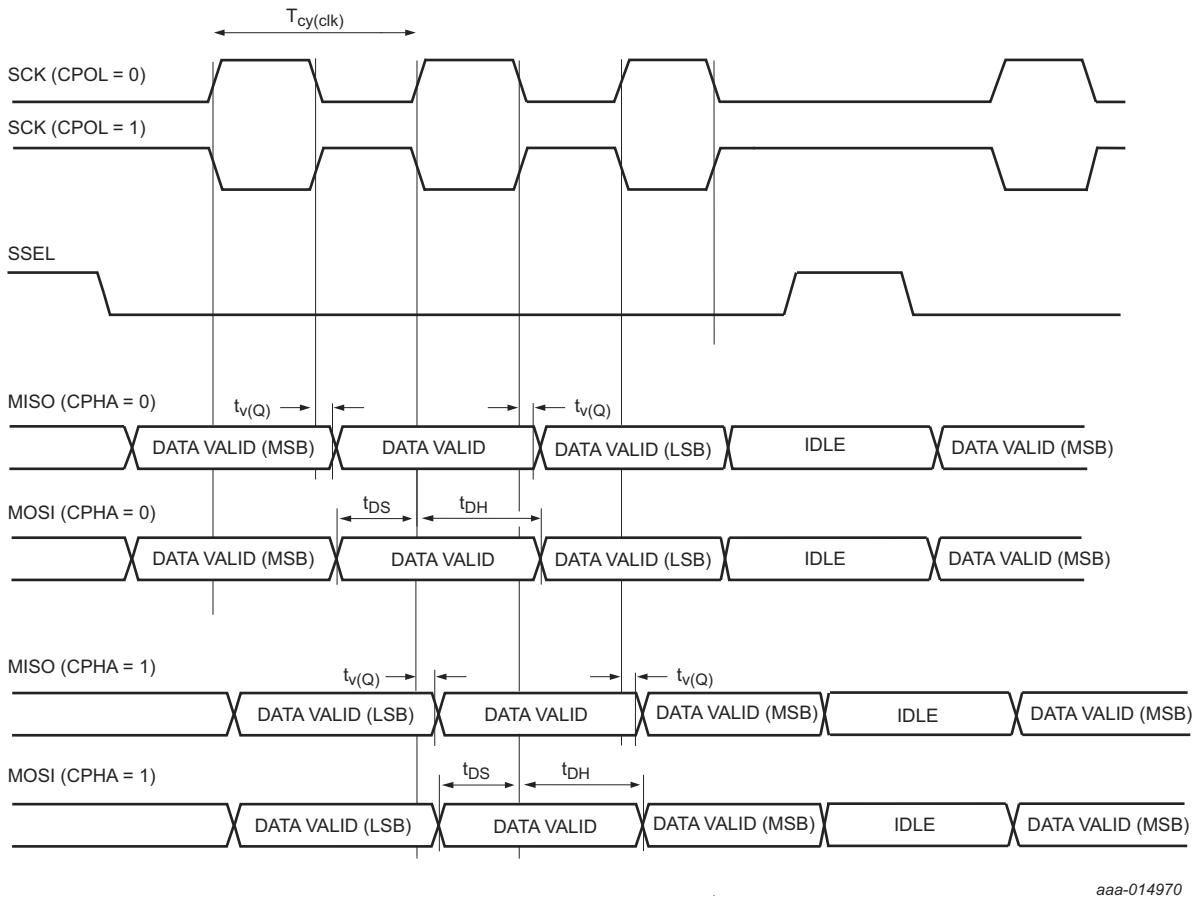


Fig 31. SPI slave timing

11.15 SPIFI

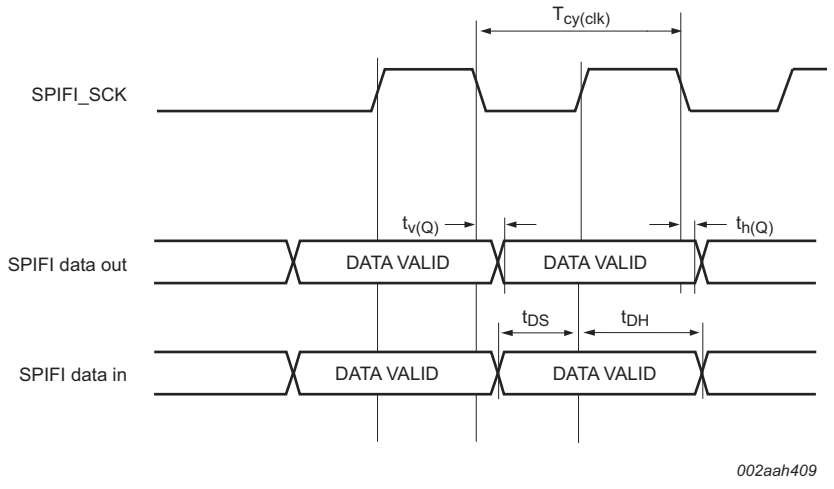
The actual SPIFI bit rate depends on the delays introduced by the external trace, the external device, system clock (CCLK), and capacitive loading. Excluding delays introduced by external device and PCB, the maximum supported bit rate for SPIFI mode is 100 Mbit/s.

Table 42. Dynamic characteristics: SPIFI[1]

T_{amb} = −40 °C to 105 °C; V_{DD} = 1.71 V to 3.6 V; C_L = 30 pF balanced loading on all pins; Input slew = 1 ns, SLEW set to standard mode for all pins; Parameters sampled at the 50 % level of the rising or falling edge.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SPIFI 1.71 V ≤ VDD ≤ 2.7 V						
t_{DS}	data set-up time	CCLK ≤ 100 MHz	4	-	-	ns
		CCLK > 100 MHz	4	-	-	ns
t_{DH}	data hold time	CCLK ≤ 100 MHz	6.4	-	-	ns
		CCLK > 100 MHz	6.6	-	-	ns
$t_{v(Q)}$	data output valid time	CCLK ≤ 100 MHz	5.7	-	13.7	ns
		CCLK > 100 MHz	5.7	-	13.7	ns
SPIFI 2.7 V ≤ VDD ≤ 3.6 V						
t_{DS}	data set-up time	CCLK ≤ 100 MHz	4	-	-	ns
		CCLK > 100 MHz	4	-	-	ns
t_{DH}	data hold time	CCLK ≤ 100 MHz	3.5	-	-	ns
		CCLK > 100 MHz	3.6	-	-	ns
$t_{v(Q)}$	data output valid time	CCLK ≤ 100 MHz	3.3	-	11.5	ns
		CCLK > 100 MHz	3.3	-	11.5	ns

[1] Based on simulation; not tested in production.



In mode 0, MODE3 bit (23) in SPIFI CTRL register is set to '0' (default). The SPIFI drives SCK low after the rising edge at which the last bit of each command is captured, and keeps it LOW while CS is HIGH.

Fig 34. SPIFI control register (Mode 0)

11.16 DMIC subsystem

Table 43. Dynamic characteristics[1]

T_{amb} = −40 °C to 105 °C; V_{DD} = 2.7 V to 3.6 V; C_L = 30 pF balanced loading on all pins; Input slew = 1 ns, SLEW set to standard mode for all pins; Bypass bit = 0; Parameters sampled at the 90 % and 10 % level of the rising or falling edge.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{DS}	data set-up time	CCLK ≤ 100 MHz	14.3	-	-	ns
		CCLK > 100 MHz	14.3	-	-	ns
t_{DH}	data hold time	CCLK ≤ 100 MHz	0	-	-	ns
		CCLK > 100 MHz	0	-	-	ns

[1] Based on simulated values.

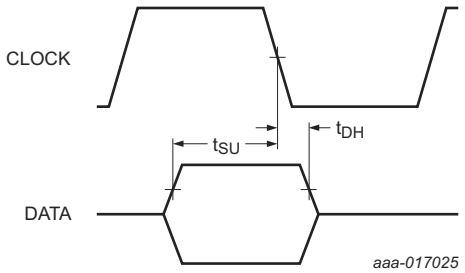


Fig 35. DMIC timing diagram

11.17 Smart card interface

Table 44. Dynamic characteristics[1]

T_{amb} = −40 °C to 105 °C; V_{DD} = 1.71 V to 3.6 V; C_L = 30 pF balanced loading on all pins; Input slew = 1 ns, SLEW setting = standard mode for all pins; Parameters sampled at the 90 % and 10 % level of the rising or falling edge.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
2.7 V ≤ VDD ≤ 3.6 V						
t_{DS}	data set-up time	CCLK ≤ 100 MHz	2.1	-	-	ns
		CCLK > 100 MHz	2.1	-	-	ns
t_{DH}	data hold time	CCLK ≤ 100 MHz	0	-	-	ns
		CCLK > 100 MHz	0	-	-	ns
$t_{v(Q)}$	data output valid time	CCLK ≤ 100 MHz	11.0	-	22.5	ns
		CCLK > 100 MHz	11.0	-	22.5	ns

[1] Based on simulated values. V_{DD} = 2.7 V - 3.6 V.

11.18 USART interface

The actual USART bit rate depends on the delays introduced by the external trace, the external device, system clock (CCLK), and capacitive loading. Excluding delays introduced by external device and PCB, the maximum supported bit rate for USART master synchronous mode is 24 Mbit/s, and the maximum supported bit rate for USART slave synchronous mode is 12.5 Mbit/s.

Table 45. USART dynamic characteristics[1]

T_{amb} = −40 °C to 105 °C; V_{DD} = 1.71 V to 3.6 V; C_L = 30 pF balanced loading on all pins; Input slew = 1 ns, SLEW setting = standard mode for all pins; Parameters sampled at the 50 % level of the rising or falling edge.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
USART master (in synchronous mode) 1.71 V ≤ VDD ≤ 2.7 V						
$t_{su(D)}$	data input set-up time	CCLK ≤ 100 MHz	21.2	-	-	ns
		CCLK > 100 MHz	19.7	-	-	ns
$t_{h(D)}$	data input hold time	CCLK ≤ 100 MHz	0	-	-	ns
		CCLK > 100 MHz	0	-	-	ns
$t_{v(Q)}$	data output valid time	CCLK ≤ 100 MHz	0	-	4.9	ns
		CCLK > 100 MHz	0	-	4.5	ns
USART slave (in synchronous mode)1.71 V ≤ VDD ≤ 2.7 V						
$t_{su(D)}$	data input set-up time	CCLK ≤ 100 MHz	1.7	-	-	ns
		CCLK > 100 MHz	1.5	-	-	ns
$t_{h(D)}$	data input hold time	CCLK ≤ 100 MHz	1.2	-	-	ns
		CCLK > 100 MHz	1.4	-	-	ns
$t_{v(Q)}$	data output valid time	CCLK ≤ 100 MHz	20.2	-	39.5	ns
		CCLK > 100 MHz	19.3	-	37.7	ns
USART master (in synchronous mode) 2.7 V ≤ VDD ≤ 3.6 V						
$t_{su(D)}$	data input set-up time	CCLK ≤ 100 MHz	20.5	-	-	ns
		CCLK > 100 MHz	18.9	-	-	ns
$t_{h(D)}$	data input hold time	CCLK ≤ 100 MHz	0	-	-	ns
		CCLK > 100 MHz	0	-	-	ns
$t_{v(Q)}$	data output valid time	CCLK ≤ 100 MHz	1.5	-	3.6	ns
		CCLK > 100 MHz	1.3	-	3.2	ns
USART slave (in synchronous mode) 2.7 V ≤ VDD ≤ 3.6 V						
$t_{su(D)}$	data input set-up time	CCLK ≤ 100 MHz	1.2	-	-	ns
		CCLK > 100 MHz	1	-	-	ns
$t_{h(D)}$	data input hold time	CCLK ≤ 100 MHz	0	-	-	ns
		CCLK > 100 MHz	0	-	-	ns
$t_{v(Q)}$	data output valid time	CCLK ≤ 100 MHz	15.2	-	26.1	ns
		CCLK > 100 MHz	14.3	-	24.2	ns

[1] Based on characterization; not tested in production.

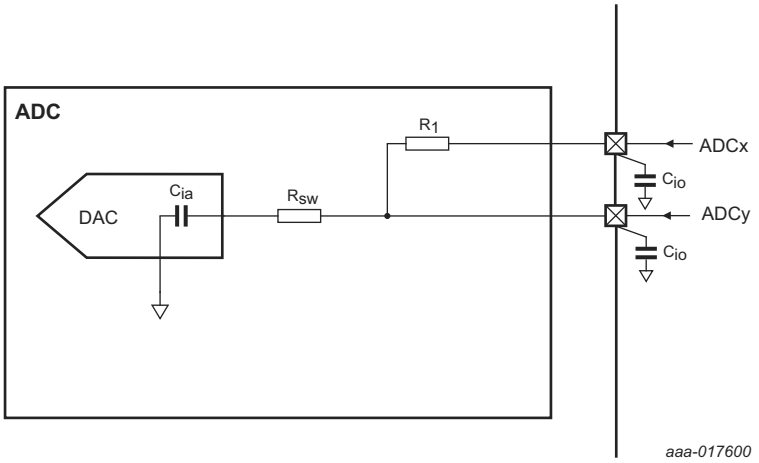


Fig 42. ADC input impedance

12.3 Temperature sensor

Table 54. Temperature sensor static and dynamic characteristics
$V_{DD} = V_{DDA} = 1.71$ V to 3.6 V

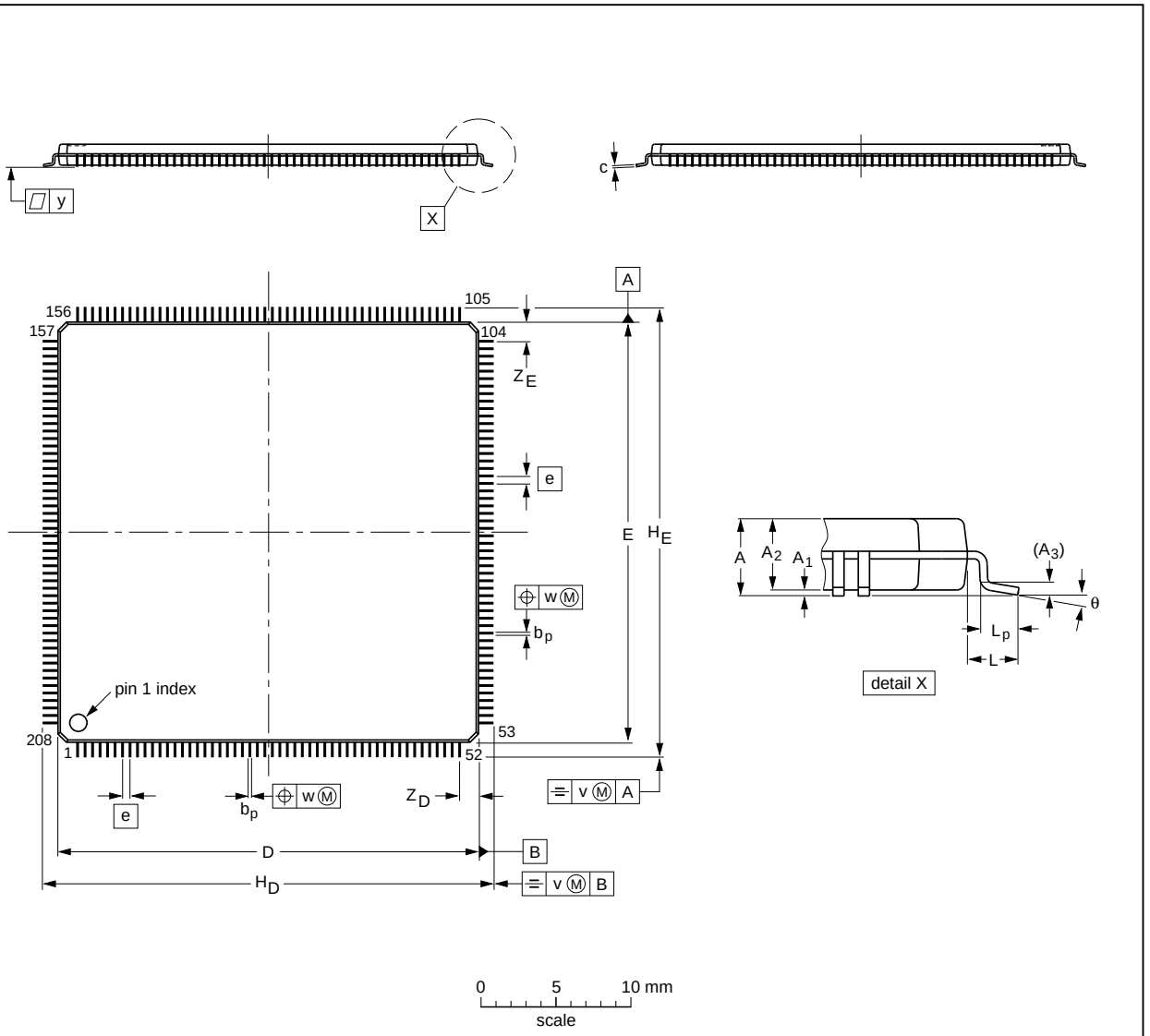
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
DT_{sen}	sensor temperature accuracy	T_{amb} = −40 °C to +105 °C	[1]	-		2.56	°C
E_L	linearity error	T_{amb} = −40 °C to +105 °C		-	-	2.56	°C
$t_{s(pu)}$	power-up settling time	to 99% of temperature sensor output value	[2]	-	10.0	15.0	µs

[1] Absolute temperature accuracy.

[2] Based on simulation.

14. Package outline

LQFP208; plastic low profile quad flat package; 208 leads; body 28 x 28 x 1.4 mm **SOT459-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	Z_D	Z_E	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	28.1 27.9	28.1 27.9	0.5	30.15 29.85	30.15 29.85	1	0.75 0.45	0.12	0.08	0.08	1.43 1.08	1.43 1.08	7^o 0^o

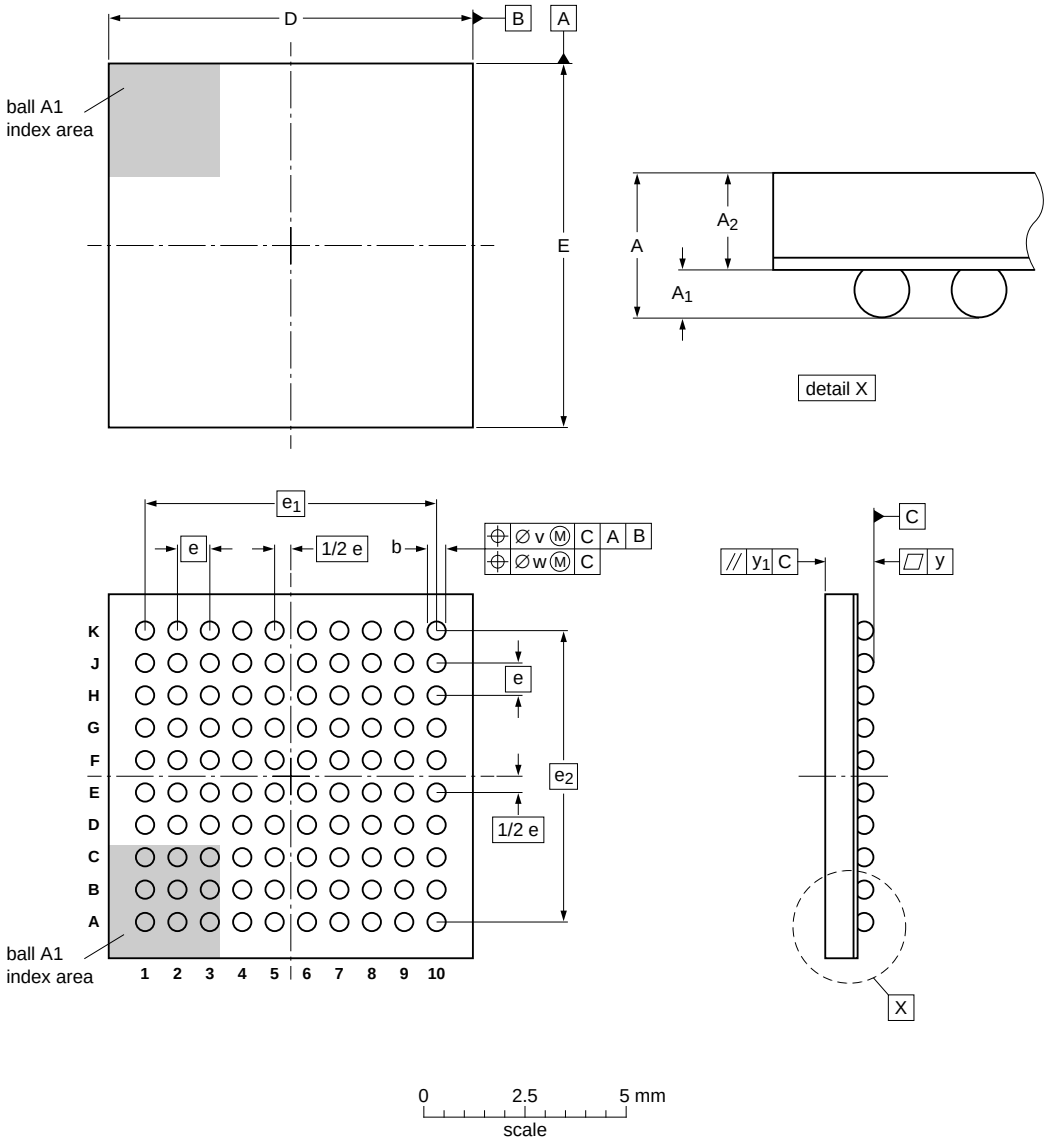
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT459-1	136E30	MS-026				~~00-02-06~~ 03-02-20

Fig 51. LQFP208 package

TFBGA100: plastic thin fine-pitch ball grid array package; 100 balls; body 9 x 9 x 0.7 mm **SOT926-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.2	0.4 0.3	0.8 0.65	0.5 0.4	9.1 8.9	9.1 8.9	0.8	7.2	7.2	0.15	0.05	0.08	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT926-1	- - -	- - -	- - -			~~05-12-09~~ 05-12-22

Fig 54. TFBGA100 package