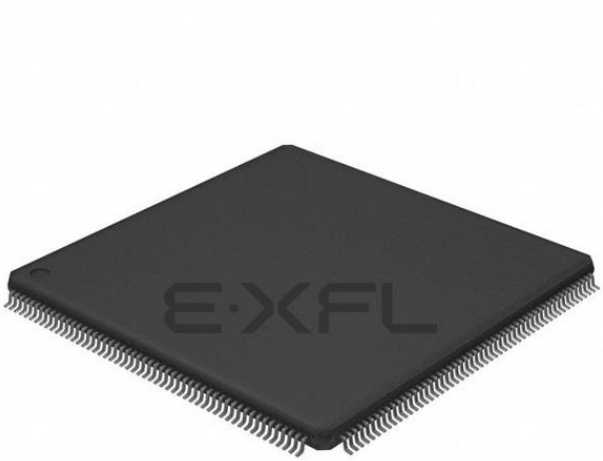

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SmartCard, SPI, SPIFI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	171
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	360K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP
Supplier Device Package	208-LQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc54018jbd208e

4. Marking

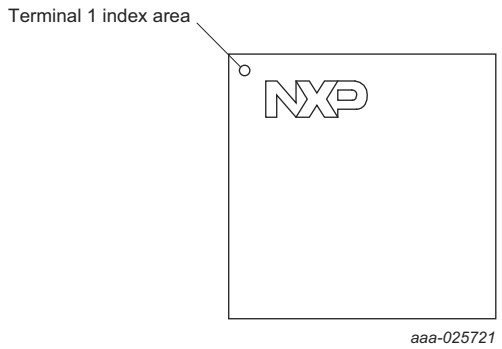

Fig 1. TFBGA180 and TFBGA 100 package markings

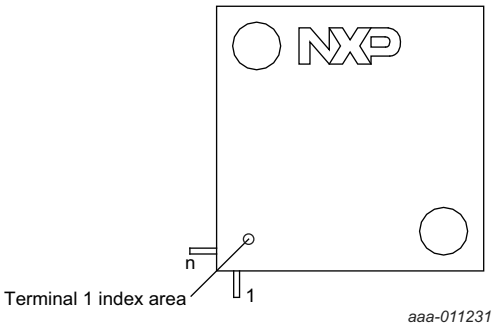

Fig 2. LQFP208 package marking

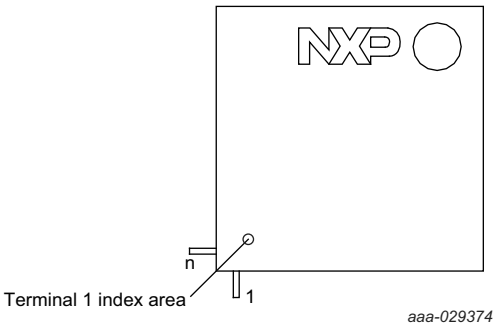

Fig 3. LQFP100 package marking

The LPC540xx TFBGA180 and TFBGA100 packages have the following top-side marking:

- First line: LPC540xxJ
- Second line: ET180 or ET100
- Third line: xxxxxxxxxxxx
- Fourth line: xxxyywwx[R]x
  - yyww: Date code with yy = year and ww = week.
  - xR = boot code version and device revision.

The LPC540xx LQFP208 and LQFP100 packages have the following top-side marking:

- First line: LPC540xxJ
- Second line: BD208 or BD100
- Third line: xxxxxxxxxxxx
- Fourth line: xxxyywwx[R]x
  - yyww: Date code with yy = year and ww = week.
  - xR = Boot code version and device revision.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state[1] [9]	Type	Description
PIO0_12/ ADC0_2	J2	M3	52	25	[4]	PU; Z	I/O; AI	**PIO0_12/ADC0_2 —** General-purpose digital input/output pin. ADC input channel 2 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
							I/O	**FC3_TXD_SCL_MISO —** Flexcomm 3: USART transmitter, I2C clock, SPI master-in/slave-out data.
								R — Reserved.
							I	**FREQME_GPIO_CLK_B —** Frequency Measure pin clock input B.
							I	**SCT0_GPI7 —** Pin input 7 to SCTimer/PWM.
								R — Reserved.
							I/O	**SWDIO —** Serial Wire Debug I/O. This is the default function after booting.
PIO0_13	C10	F11	141	67	[3]	Z	I/O	**PIO0_13 —** General-purpose digital input/output pin. **Remark:** In ISP mode, this pin is set to the Flexcomm 1 I2C SDA function.
							I/O	**FC1_CTS_SDA_SSEL0 —** Flexcomm 1: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							I	**UTICK_CAP0 —** Micro-tick timer capture input 0.
							I	**CT0_CAP0 —** Capture input 0 to Timer 0.
							I	**SCT0_GPI0 —** Pin input 0 to SCTimer/PWM.
								R — Reserved.
								R — Reserved.
							I	**ENET_RXD0 —** Ethernet receive data 0.
PIO0_14	D9	E13	144	69	[3]	Z	I/O	**PIO0_14 —** General-purpose digital input/output pin. **Remark:** In ISP mode, this pin is set to the Flexcomm 1 I2C SCL function.
							I/O	**FC1_RTS_SCL_SSEL1 —** Flexcomm 1: USART request-to-send, I2C clock, SPI slave select 1.
							I	**UTICK_CAP1 —** Micro-tick timer capture input 1.
							I	**CT0_CAP1 —** Capture input 1 to Timer 0.
							I	**SCT0_GPI1 —** Pin input 1 to SCTimer/PWM.
								R — Reserved.
								R — Reserved.
							I	**ENET_RXD1 —** Ethernet receive data 1.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state[1] [9]	Type	Description
PIO1_8	H5	P8	72	36	[2]	PU; Z	I/O	**PIO1_8 —** General-purpose digital input/output pin.
							I/O	**FC0_CTS_SDA_SSEL0 —** Flexcomm 0: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							O	**SD_CLK —** SD/MMC clock.
								R — Reserved.
							O	**SCT0_OUT1 —** SCTimer/PWM output 1.
							I/O	**FC4_SSEL2 —** Flexcomm 4: SPI slave select 2.
							O	**EMC_A[7] —** External memory interface address 7.
PIO1_9	K7	K6	78	39	[2]	PU; Z	I/O	**PIO1_9 —** General-purpose digital input/output pin.
							O	**ENET_TXD0 —** Ethernet transmit data 0.
							I/O	**FC1_SCK —** Flexcomm 1: USART or SPI clock.
							I	**CT1_CAP0 —** Capture 0 input to Timer 1.
							O	**SCT0_OUT2 —** SCTimer/PWM output 2.
							I/O	**FC4_CTS_SDA_SSEL0 —** Flexcomm 4: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							O	**EMC_CASN —** External memory interface column access strobe (active low).
PIO1_10	H6	N9	84	41	[2]	PU; Z	I/O	**PIO1_10 —** General-purpose digital input/output pin.
							O	**ENET_TXD1 —** Ethernet transmit data 1.
							I/O	**FC1_RXD_SDA_MOSI —** Flexcomm 1: USART receiver, I2C data I/O, SPI master-out/slave-in data.
							O	**CT1_MAT0 —** Match output 0 from Timer 1.
							O	**SCT0_OUT3 —** SCTimer/PWM output 3.
								R — Reserved.
							O	**EMC_RASN —** External memory interface row address strobe (active low).
PIO1_11	B4	B4	198	94	[2][8]	PU; Z	I/O	**PIO1_11 —** General-purpose digital input/output pin.
							O	**ENET_TX_EN —** Ethernet transmit enable (RMII/MII interface).
							I/O	**FC1_TXD_SCL_MISO —** Flexcomm 1: USART transmitter, I2C clock, SPI master-in/slave-out data.
							I	**CT1_CAP1 —** Capture 1 input to Timer 1.
							I	**USB0_VBUS —** Monitors the presence of USB0 bus power.
								R — Reserved.
							O	**EMC_CLK[0] —** External memory interface clock 0.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state[1] [9]	Type	Description
PIO1_28	A10	E12	151	73	[2]	PU; Z	I/O	**PIO1_28 —** General-purpose digital input/output pin.
							I/O	**FC7_SCK —** Flexcomm 7: USART, SPI, or I2S clock.
							I/O	**SD_D[5] —** SD/MMC data 5.
							I	**CT0_CAP2 —** Capture 2 input to Timer 0.
								R — Reserved.
								R — Reserved.
							I/O	**EMC_D[12] —** External Memory interface data [12].
PIO1_29	A8	C11	165	81	[2][8]	PU; Z	I/O	**PIO1_29 —** General-purpose digital input/output pin.
							I/O	**FC7_RXD_SDA_MOSI_DATA —** Flexcomm 7: USART receiver, I2C data I/O, SPI master-out/slave-in data, I2S data I/O.
							I/O	**SD_D[6] —** SD/MMC data 6.
							I	**SCT0_GPI6 —** Pin input 6 to SCTimer/PWM.
							O	**USB1_PORTPWRN —** USB1 VBUS drive indicator (Indicates VBUS must be driven).
							O	**USB1_FRAME —** USB1 frame toggle signal.
							I/O	**EMC_D[13] —** External Memory interface data [13].
PIO1_30	C6	A8	182	86	[2]	PU; Z	I/O	**PIO1_30 —** General-purpose digital input/output pin.
							I/O	**FC7_TXD_SCL_MISO_WS —** Flexcomm 7: USART transmitter, I2C clock, SPI master-in/slave-out data I/O, I2S word-select/frame.
							I/O	**SD_D[7] —** SD/MMC data 7.
							I	**SCT0_GPI7 —** Pin input 7 to SCTimer/PWM.
							I	**USB1_OVERCURRENTN —** USB1 bus overcurrent indicator (active low).
							O	**USB1_LEDN —** USB1-configured LED indicator (active low).
							I/O	**EMC_D[14] —** External Memory interface data [14].
PIO1_31	A3	C5	195	92	[2]	PU; Z	I/O	**PIO1_31 —** General-purpose digital input/output pin.
							I/O	**MCLK —** MCLK input or output for I2S and/or digital microphone.
								R — Reserved.
							O	**CT0_MAT2 —** Match output 2 from Timer 0.
							O	**SCT0_OUT6 —** SCTimer/PWM output 6.
							I/O	**FC8_CTS_SDA_SSEL0 —** Flexcomm 8: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							I/O	**EMC_D[15] —** External Memory interface data [15].

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state[1] [9]	Type	Description
PIO3_13	-	H4	75	-	[2]	PU; Z	I/O	**PIO3_13 —** General-purpose digital input/output pin.
							O	**SCT0_OUT9 —** SCTimer/PWM output 9.
							I/O	**FC9_CTS_SDA_SSEL0 —** Flexcomm 9: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							I	**CT3_CAP1 —** Capture input 1 to Timer 3.
								R — Reserved.
								R — Reserved.
							I	**EMC_FBCK —** External memory interface feedback clock.
							O	**TRACEDATA[1] —** Trace data bit 1.
PIO3_14	-	E3	13	-	[2]	PU; Z	I/O	**PIO3_14 —** General-purpose digital input/output pin.
							O	**SCT0_OUT4 —** SCTimer/PWM output 4.
							I/O	**FC9_RTS_SCL_SSEL1 —** Flexcomm 9: USART request-to-send, I2C clock, SPI slave select 1.
							O	**CT3_MAT1 —** Match output 1 from Timer 3.
								R — Reserved.
								R — Reserved.
								R — Reserved.
							O	**TRACEDATA[2] —** Trace data bit 2.
PIO3_15	-	D2	11	-	[2]	PU; Z	I/O	**PIO3_15 —** General-purpose digital input/output pin.
							I/O	**FC8_SCK —** Flexcomm 8: USART or SPI clock.
							I	**SD_WR_PRT —** SD/MMC write protect.
PIO3_16	-	E1	19	-	[2]	PU; Z	I/O	**PIO3_16 —** General-purpose digital input/output pin.
							I/O	**FC8_RXD_SDA_MOSI —** Flexcomm 8: USART receiver, I2C data I/O, SPI master-out/slave-in data.
							I/O	**SD_D[4] —** SD/MMC data 4.
PIO3_17	-	K1	31	-	[2]	PU; Z	I/O	**PIO3_17 —** General-purpose digital input/output pin.
							I/O	**FC8_TXD_SCL_MISO —** Flexcomm 8: USART transmitter, I2C clock, SPI master-in/slave-out data.
							I/O	**SD_D[5] —** SD/MMC data 5.
PIO3_18	-	M6	68	-	[2]	PU; Z	I/O	**PIO3_18 —** General-purpose digital input/output pin.
							I/O	**FC8_CTS_SDA_SSEL0 —** Flexcomm 8: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							I/O	**SD_D[6] —** SD/MMC data 6.
							O	**CT4_MAT0 —** Match output 0 from Timer 4.
							O	**CAN0_TD —** Transmitter output for CAN 0.
							O	**SCT0_OUT5 —** SCTimer/PWM output 5.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state[1] [9]	Type	Description
PIO3_19	-	J3	44	-	[2]	PU; Z	I/O	**PIO3_19 —** General-purpose digital input/output pin.
							I/O	**FC8_RTS_SCL_SSEL1 —** Flexcomm 8: USART request-to-send, I2C clock, SPI slave select 1.
							I/O	**SD_D[7] —** SD/MMC data 7.
							O	**CT4_MAT1 —** Match output 1 from Timer 4.
							I	**CAN0_RD —** Receiver input for CAN 0.
							O	**SCT0_OUT6 —** SCTimer/PWM output 6.
PIO3_20	-	N2	46	-	[2]	PU; Z	I/O	**PIO3_20 —** General-purpose digital input/output pin.
							I/O	**FC9_SCK —** Flexcomm 9: USART or SPI clock.
							I	**SD_CARD_INT_N —**
							O	**CLKOUT —** Output of the CLKOUT function.
								R — Reserved.
							O	**SCT0_OUT7 —** SCTimer/PWM output 7.
PIO3_21/ ADC0_9	-	P5	61	-	[4]	PU; Z	I/O; AI	**PIO3_21/ADC0_9 —** General-purpose digital input/output pin. ADC input channel 9 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
							I/O	**FC9_RXD_SDA_MOSI —** Flexcomm 9: USART receiver, I2C data I/O, SPI master-out/slave-in data.
							O	**SD_BACKEND_PWR —** SD/MMC back-end power supply for embedded device.
							O	**CT4_MAT3 —** Match output 3 from Timer 4.
							I	**UTICK_CAP2 —** Micro-tick timer capture input 2.
PIO3_22/ ADC0_10	-	N5	62	-	[4]	PU; Z	I/O; AI	**PIO3_22/ADC0_10 —** General-purpose digital input/output pin. ADC input channel 10 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
							I/O	**FC9_TXD_SCL_MISO —** Flexcomm 9: USART transmitter, I2C clock, SPI master-in/slave-out data.
PIO3_23	-	C2	8	-	[3]	Z	I/O	**PIO3_23 —** General-purpose digital input/output pin.
							I/O	**FC2_CTS_SDA_SSEL0 —** Flexcomm 2: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
								R — Reserved.
							I	**UTICK_CAP3 —** Micro-tick timer capture input 3.
PIO3_24	-	E2	16	-	[3]	Z	I/O	**PIO3_24 —** General-purpose digital input/output pin.
							I/O	**FC2_RTS_SCL_SSEL1 —** Flexcomm 2: USART request-to-send, I2C clock, SPI slave select 1.
							I	**CT4_CAP0 —** Capture input 4 to Timer 0.
							I	**USB0_VBUS —** Monitors the presence of USB0 bus power.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state[1] [9]	Type	Description
PIO4_5	-	E10	154	-	[2]	PU; Z	I/O	**PIO4_5 —** General-purpose digital input/output pin.
								R — Reserved.
							I/O	**FC9_CTS_SDA_SSEL0 —** Flexcomm 9: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							I/O	**FC0_CTS_SDA_SSEL0 —** Flexcomm 0: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							O	**CT4_MAT3 —** Match output 3 from Timer 4.
							I	**SCT0_GPI6 —** Pin input 6 to SCTimer/PWM.
							O	**EMC_CKE[2] —** External memory interface SDRAM clock enable 2.
PIO4_6	-	D10	161	-	[2]	PU; Z	I/O	**PIO4_6 —** General-purpose digital input/output pin.
								R — Reserved.
							I/O	**FC9_RTS_SCL_SSEL1 —** Flexcomm 9: USART request-to-send, I2C clock, SPI slave select 1.
								R — Reserved.
								R — Reserved.
							I	**SCT0_GPI7 —** Pin input 7 to SCTimer/PWM.
							O	**EMC_CKE[3] —** External memory interface SDRAM clock enable 3.
PIO4_7	-	A14	166	-	[2][8]	PU; Z	I/O	**PIO4_7 —** General-purpose digital input/output pin.
								R — Reserved.
							I	**CT4_CAP3 —** Capture input 3 to Timer 4.
							O	**USB0_PORTPWRN —** USB0 VBUS drive indicator (Indicates VBUS must be driven).
							O	**USB0_FRAME —** USB0 frame toggle signal.
							I	**SCT0_GPI0 —** Pin input 0 to SCTimer/PWM.
PIO4_8	-	B14	170	-	[2]	PU; Z	I/O	**PIO4_8 —** General-purpose digital input/output pin.
							O	**ENET_TXD0 —** Ethernet transmit data 0.
							I/O	**FC2_SCK —** Flexcomm 2: USART or SPI clock.
							I	**USB0_OVERCURRENTN —** USB0 bus overcurrent indicator (active low).
							O	**USB0_LEDN —** USB0-configured LED indicator (active low).
							I	**SCT0_GPI1 —** Pin input 1 to SCTimer/PWM.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state[1] [9]	Type	Description
PIO5_3	-	-	129	-	[2]	PU; Z	I/O	**PIO5_3 —** General-purpose digital input/output pin.
							O	**ENET_MDC —** Ethernet management data clock.
							O	**SD_VOLT[2] —** SD/MMC card regulator voltage control [2].
							I	**CT3_CAP1 —** Capture input 1 to Timer 3.
							I/O	**FC4_RTS_SCL_SSEL1 —** Flexcomm 4: USART request-to-send, I2C clock, SPI slave select 1.
								R — Reserved.
							I/O	**EMC_D[30] —** External Memory interface data [30].
PIO5_4	-	-	135	-	[2]	PU; Z	I/O	**PIO5_4 —** General-purpose digital input/output pin.
							I/O	**ENET_MDIO —** Ethernet management data I/O.
							O	**SD_BACKEND_PWR —** SD/MMC back-end power supply for embedded device.
							I	**CT3_CAP2 —** Capture input 2 to Timer 3.
							I/O	**FC4_SSEL2 —** Flexcomm 4: SPI slave select 2.
								R — Reserved.
							I/O	**EMC_D[31] —** External Memory interface data [31].
PIO5_5	-	-	145	-	[2]	PU; Z	I/O	**PIO5_5 —** General-purpose digital input/output pin.
							I	**SCT0_GPI0 —** Pin input 0 to SCTimer/PWM.
							O	**PDM1_CLK —** Clock for PDM interface 1, for digital microphone.
							I	**CT3_CAP3 —** Capture input 3 to Timer 3.
							I/O	**FC4_SSEL3 —** Flexcomm 4: SPI slave select 3.
							O	**TRACECLK —** Trace clock.
							O	**EMC_A[21] —** External memory interface address 21.
PIO5_6	-	-	152	-	[2]	PU; Z	I/O	**PIO5_6 —** General-purpose digital input/output pin.
							I	**SCT0_GPI1 —** Pin input 1 to SCTimer/PWM.
							I	**PDM1_DATA —** Data for PDM interface 1 (digital microphone).
							I/O	**FC5_SCK —** Flexcomm 5: USART or SPI clock.
							O	**SCT0_OUT5 —** SCTimer/PWM output 5.
							O	**TRACEDATA[0] —** Trace data bit 0.
							O	**EMC_A[22] —** External memory interface address 22.

Table 7. Memory usage and details *…continued*

Address range	General Use	Address range details and description	
0x8000 0000 to 0xDFFF FFFF	Off-chip Memory via the External Memory Controller	Four static memory chip selects:	
		0x8000 0000 - 0x83FF FFFF	Static memory chip select 0 (up to 64 MB)[1]
		0x8800 0000 - 0x8BFF FFFF	Static memory chip select 1 (up to 64 MB)[2]
		0x9000 0000 – 0x93FF FFFF	Static memory chip select 2 (up to 64 MB).
		0x9800 0000 - 0x9BFF FFFF	Static memory chip select 3 (up to 64 MB).
		Four dynamic memory chip selects:	
		0xA000 0000 - 0xA7FF FFFF	Dynamic memory chip select 0 (up to 256 MB).
		0xA800 0000 - 0xAFFF FFFF	Dynamic memory chip select 1 (up to 256 MB).
		0xB000 0000 - 0xB7FF FFFF	Dynamic memory chip select 2 (up to 256 MB).
		0xB800 0000 - 0xBFFF FFFF	Dynamic memory chip select 3 (up to 256 MB).
0xE000 0000 to 0xE00F FFFF	Cortex-M4 Private Peripheral Bus	0xE000 0000 - 0xE00F FFFF	Cortex-M4 related functions, includes the NVIC and System Tick Timer.

[1] Can be up to 256 MB, upper address 0x8FFF FFFF, if the address shift mode is enabled. See the EMCSYSCTRL register bit 0 in the *LPC540xx user manual*.

[2] Can be up to 128 MB, upper address 0x97FF FFFF, if the address shift mode is enabled. See the EMCSYSCTRL register bit 0 in the *LPC540xx user manual*.

Figure 9 shows the overall map of the entire address space from the user program viewpoint following reset.

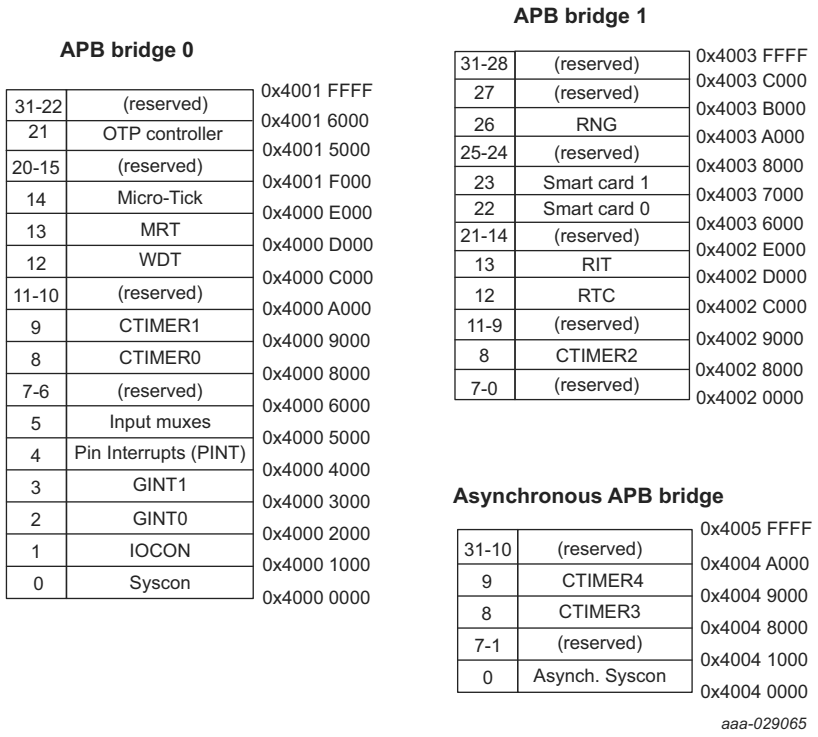

Fig 10. LPC540xx APB Memory map

7.10 System control

7.10.1 Clock sources

The LPC540xx supports one external and two internal clock sources:

- Free Running Oscillator (FRO).
- Watchdog oscillator (WDOSC).
- Crystal oscillator.

7.10.1.1 Free Running Oscillator (FRO)

The FRO 12 MHz oscillator provides the default clock at reset and provides a clean system clock shortly after the supply pins reach operating voltage.

- 12 MHz internal FRO oscillator, factory trimmed for accuracy, that can optionally be used as a system clock as well as other purposes.
- Selectable 48 MHz or 96 MHz FRO oscillator, factory trimmed for accuracy, that can optionally be used as a system clock as well as other purposes.

7.10.1.2 Watchdog oscillator (WDOSC)

The watchdog oscillator is a low-power internal oscillator. The WDOSC can be used to provide a clock to the WWDT and to the entire chip. The low-power watchdog oscillator provides a selectable frequency in the range of 6 kHz to 1.5 MHz. The accuracy of this clock is limited to ± 40% over temperature, voltage, and silicon processing variations.

7.14.8.2 SPI serial I/O controller

Features

- Maximum data rates of 48 Mbit/s in master mode and 14 Mbit/s in slave mode for SPI functions. (Flexcomm Interface 0-9).
- Maximum data rates of 50 Mbit/s in master mode and 50 Mbit/s in slave mode for SPI functions (Flexcomm Interface10).
- Data frames of 1 to 16 bits supported directly. Larger frames supported by software or DMA set-up.
- Master and slave operation.
- Data can be transmitted to a slave without the need to read incoming data. This can be useful while setting up an SPI memory.
- Control information can optionally be written along with data. This allows very versatile operation, including “any length” frames.
- Four Slave Select input/outputs with selectable polarity and flexible usage.
- Activity on the SPI in slave mode allows wake-up from deep-sleep mode on any enabled interrupt.

Remark: Texas Instruments SSI and National Microwire modes are not supported.

7.14.8.3 I^2C-bus interface

The I^2C-bus is bidirectional for inter-IC control using only two wires: a serial clock line (SCL) and a serial data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (for example, an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^2C is a multi-master bus and can be controlled by more than one bus master connected to it.

Features

- All I2Cs support standard, Fast-mode, and Fast-mode Plus with data rates of up to 1 Mbit/s.
- All I2Cs support high-speed slave mode with data rates of up to 3.4 Mbit/s.
- Independent Master, Slave, and Monitor functions.
- Supports both Multi-master and Multi-master with Slave functions.
- Multiple I^2C slave addresses supported in hardware.
- One slave address can be selectively qualified with a bit mask or an address range in order to respond to multiple I^2C-bus addresses.
- 10-bit addressing supported with software assist.
- Supports SMBus.
- Activity on the I2C in slave mode allows wake-up from deep-sleep mode on any enabled interrupt.

7.15.4 DMA controller

The DMA controller allows peripheral-to memory, memory-to-peripheral, and memory-to-memory transactions. Each DMA stream provides unidirectional DMA transfers for a single source and destination.

7.15.4.1 Features

- One channel per on-chip peripheral direction: typically one for input and one for output for most peripherals.
- DMA operations can optionally be triggered by on- or off-chip events.
- Priority is user selectable for each channel.
- Continuous priority arbitration.
- Address cache.
- Efficient use of data bus.
- Supports single transfers up to 1,024 words.
- Address increment options allow packing and/or unpacking data.

7.16 Counter/timers

7.16.1 General-purpose 32-bit timers/external event counter

The LPC540xx includes five general-purpose 32-bit timer/counters.

The timer/counter is designed to count cycles of the system derived clock or an externally-supplied clock. It can optionally generate interrupts, generate timed DMA requests, or perform other actions at specified timer values, based on four match registers. Each timer/counter also includes two capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.

7.16.1.1 Features

- A 32-bit timer/counter with a programmable 32-bit prescaler.
- Counter or timer operation.
- Up to four 32-bit captures can take a snapshot of the timer value when an input signal transitions. A capture event may also optionally generate an interrupt. The number of capture inputs for each timer that are actually available on device pins may vary by device.
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
  - Shadow registers are added for glitch-free PWM output.
- For each timer, up to four external outputs corresponding to match registers with the following capabilities (the number of match outputs for each timer that are actually available on device pins may vary by device):
  - Set LOW on match.
  - Set HIGH on match.

Table 10. Limiting values *…continued*
In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
$P_{tot(pack)}$	total power dissipation (per package)	LQFP208, based on package heat transfer, not device power consumption	[11]	-	1.2	W
		LQFP208, based on package heat transfer, not device power consumption	[12]	-	0.95	W
		LQFP100, based on package heat transfer, not device power consumption	[11]	-	0.82	W
		LQFP100, based on package heat transfer, not device power consumption	[12]	-	0.60	W
		TFBGA180, based on package heat transfer, not device power consumption	[11]	-	0.95	W
		TFBGA180, based on package heat transfer, not device power consumption	[13]	-	1.2	W
		TFBGA100, based on package heat transfer, not device power consumption	[11]	-	0.57	W
		TFBGA100, based on package heat transfer, not device power consumption	[13]	-	0.65	W
V_{ESD}	electrostatic discharge voltage	human body model; all pins	[4]	-	2000	V

[1] The following applies to the limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

c) The limiting values are stress ratings only and operating the part at these values is not recommended and proper operation is not guaranteed. The conditions for functional operation are specified in Table 20.

[2] Maximum/minimum voltage above the maximum operating voltage (see Table 20) and below ground that can be applied for a short time (< 10 ms) to a device without leading to irrecoverable failure. Failure includes the loss of reliability and shorter lifetime of the device.

[3] The peak current is limited to 25 times the corresponding maximum current.

[4] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

[5] V_{DD} present or not present. Compliant with the I^2C-bus standard. 5.5 V can be applied to this pin when V_{DD} is powered down.

[6] Applies to all 5 V tolerant I/O pins except true open-drain pins.

[7] Including the voltage on outputs in 3-state mode.

[8] An ADC input voltage above 3.6 V can be applied for a short time without leading to immediate, unrecoverable failure. Accumulated exposure to elevated voltages at 4.6 V must be less than 10^6 s total over the lifetime of the device. Applying an elevated voltage to the ADC inputs for a long time affects the reliability of the device and reduces its lifetime.

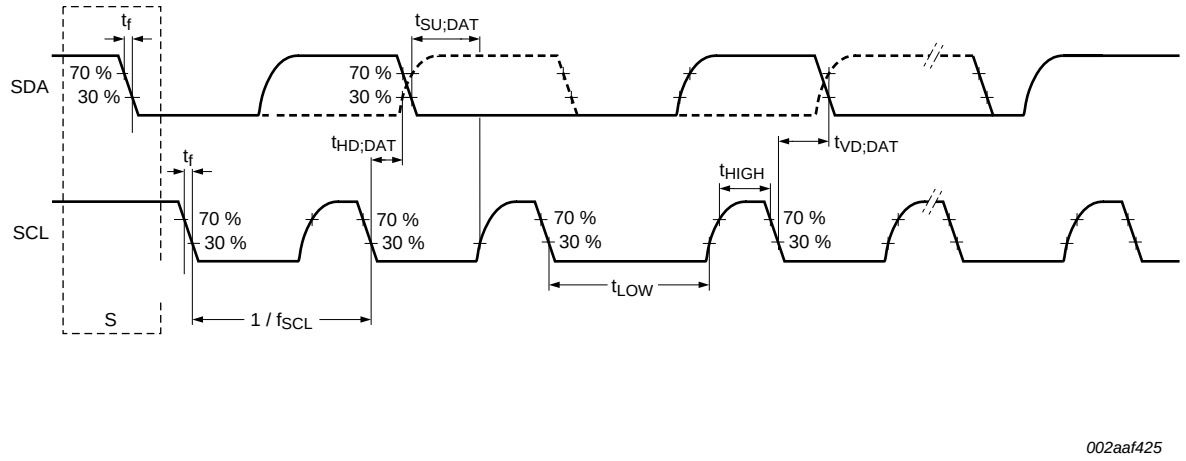

Fig 27. I^2C-bus pins clock timing

11.13 SPI interfaces (Flexcomm Interface 0-9)

The actual SPI bit rate depends on the delays introduced by the external trace, the external device, system clock (CCLK), and capacitive loading. Excluding delays introduced by external device and PCB, the maximum supported bit rate for SPI master mode is 48 Mbit/s, and the maximum supported bit rate for SPI slave mode is 14 Mbit/s.

Table 40. SPI dynamic characteristics[1]

T_{amb} = −40 °C to 105 °C; 1.71 V ≤ V_{DD} ≤ 3.6 V; C_L = 30 pF balanced loading on all pins; Input slew = 1 ns, SLEW setting = standard mode for all pins;. Parameters sampled at the 50 % level of the rising or falling edge.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
SPI master 1.71 V ≤ V_{DD} ≤ 2.7 V							
t_{DS}	data set-up time	CCLK ≤ 100 MHz		2.2	-	-	ns
		CCLK > 100 MHz		1.9	-	-	ns
t_{DH}	data hold time	CCLK ≤ 100 MHz		6.3	-	-	ns
		CCLK > 100 MHz		6.7	-	-	ns
$t_{v(Q)}$	data output valid time	CCLK ≤ 100 MHz		2.6	-	5.0	ns
		CCLK > 100 MHz		0.3	-	4.7	ns
SPI slave 1.71 V ≤ V_{DD} ≤ 2.7 V							
t_{DS}	data set-up time	CCLK ≤ 100 MHz		1.1	-	-	ns
		CCLK > 100 MHz		0.9	-	-	ns
t_{DH}	data hold time	CCLK ≤ 100 MHz		2.1	-	-	ns
		CCLK > 100 MHz		2.2	-	-	ns
$t_{v(Q)}$	data output valid time	CCLK ≤ 100 MHz		18.8	-	37.0	ns
		CCLK > 100 MHz		18.0	-	36.0	ns
SPI master 2.7 V ≤ V_{DD} ≤ 3.6 V							
t_{DS}	data set-up time	CCLK ≤ 100 MHz		2.4	-	-	ns
		CCLK > 100 MHz		2.2	-	-	ns
t_{DH}	data hold time	CCLK ≤ 100 MHz		4.2	-	-	ns
		CCLK > 100 MHz		4.5	-	-	ns
$t_{v(Q)}$	data output valid time	CCLK ≤ 100 MHz		1.8	-	4.6	ns
		CCLK > 100 MHz		1.7	-	4.0	ns
SPI slave 2.7 V ≤ V_{DD} ≤ 3.6 V							
t_{DS}	data set-up time	CCLK ≤ 100 MHz		1.2	-	-	ns
		CCLK > 100 MHz		1.0	-	-	ns
t_{DH}	data hold time	CCLK ≤ 100 MHz		0	-	-	ns
		CCLK > 100 MHz		0	-	-	ns
$t_{v(Q)}$	data output valid time	CCLK ≤ 100 MHz		14	-	23.9	ns
		CCLK > 100 MHz		13.3	-	22.2	ns

[1] Based on characterization; not tested in production.

12.2 12-bit ADC characteristics

Table 52. 12-bit ADC static characteristics

T_{amb} = −40 °C to +105 °C; 1.71 V ≤ V_{DD} ≤ 3.6 V; V_{SSA} = VREFN = GND. ADC calibrated at T_{amb} = 25 °C.

Symbol	Parameter	Conditions		Min	Typ[2]	Max	Unit
V_{IA}	analog input voltage		[3]	0	-	V_{DDA}	V
C_{ia}	analog input capacitance		[4]	-	5.0	-	pF
$f_{clk(ADC)}$	ADC clock frequency				-	80	MHz
f_s	sampling frequency			-	5.0	5.3	Msamples/s
E_D	differential linearity error	2.0 V < V_{DDA} ≤ 3.6 V 2.0 V < VREFP ≤ 3.6 V $f_{clk(ADC)}$ = 80 MHz	[1][5]	-	< ±3.0	-	LSB
		1.71 V ≤ V_{DDA} ≤ 2.0 V 1.71 V ≤ VREFP ≤ 2.0 V $f_{clk(ADC)}$ = 80 MHz	[1][5]	-	< ±4.5	-	LSB
			[1][5]	-		-	LSB
$E_{L(adj)}$	integral non-linearity	2.0 V < V_{DDA} ≤ 3.6 V 2.0 V < VREFP ≤ 3.6 V $f_{clk(ADC)}$ = 80 MHz	[1][6]	-	< ±4.0	-	LSB
		1.71 V ≤ V_{DDA} ≤ 2.0 V 1.71 V ≤ VREFP ≤ 2.0 V $f_{clk(ADC)}$ = 80 MHz	[1][6]	-	< ±7.5	-	LSB
			[1][6]	-		-	LSB
E_O	offset error	calibration enabled	[1][7]	-	< ±2.2	-	mV
$V_{err(FS)}$	full-scale error voltage	2.0 V < V_{DDA} ≤ 3.6 V 2.0 V < VREFP ≤ 3.6 V $f_{clk(ADC)}$ = 80 MHz	[1][8]	-	< ±3.0	-	LSB
		1.71 V ≤ V_{DDA} ≤ 2.0 V 1.71 V ≤ VREFP ≤ 2.0 V $f_{clk(ADC)}$ = 80 MHz		-	< ±2.5	-	LSB
Z_i	input impedance	f_s = 5.0 Msamples/s	[9][10]	17.0	-	-	kΩ

[1] Based on characterization; not tested in production.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[3] The input resistance of ADC channels 6 to 11 is higher than ADC channels 0 to 5.

[4] C_{ia} represents the external capacitance on the analog input channel for sampling speeds of 5.0 Msamples/s. No parasitic capacitances included.

[5] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 41.

[6] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 41.

[7] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 41.

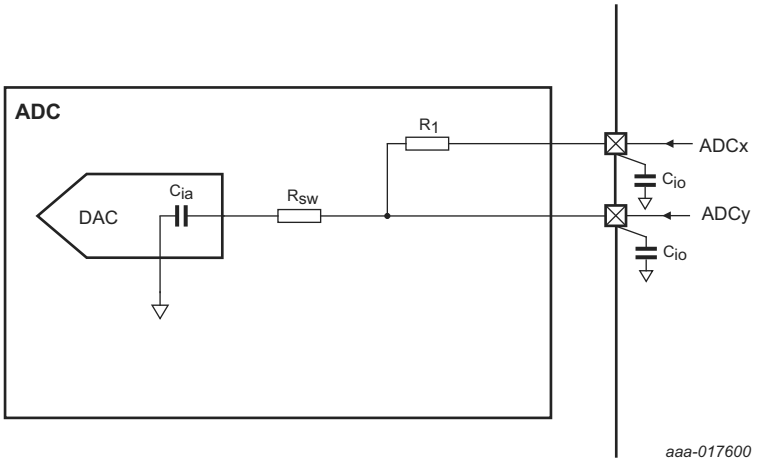

Fig 42. ADC input impedance

12.3 Temperature sensor

Table 54. Temperature sensor static and dynamic characteristics
$V_{DD} = V_{DDA} = 1.71$ V to 3.6 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
DT_{sen}	sensor temperature accuracy	T_{amb} = −40 °C to +105 °C	[1]	-		2.56	°C
E_L	linearity error	T_{amb} = −40 °C to +105 °C		-	-	2.56	°C
$t_{s(pu)}$	power-up settling time	to 99% of temperature sensor output value	[2]	-	10.0	15.0	µs

[1] Absolute temperature accuracy.

[2] Based on simulation.

16. Abbreviations

Table 57. Abbreviations

Acronym	Description
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
API	Application Programming Interface
DMA	Direct Memory Access
FRO oscillator	Internal Free-Running Oscillator, tuned to the factory specified frequency
GPIO	General Purpose Input/Output
FRO	Free Running Oscillator
LSB	Least Significant Bit
MCU	MicroController Unit
PDM	Pulse Density Modulation
PLL	Phase-Locked Loop
SPI	Serial Peripheral Interface
TCP/IP	Transmission Control Protocol/Internet Protocol
TTL	Transistor-Transistor Logic
USART	Universal Asynchronous Receiver/Transmitter

17. References

[1] LPC540xx. User manual UM11060.

[2] LPC540xx. Errata sheet.

[3] Technical note ADC design guidelines: http://www.nxp.com/documents/technical_note/TN00009.pdf

19. Legal information

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Document status[1][2]	Product status[3]	Definition
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Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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