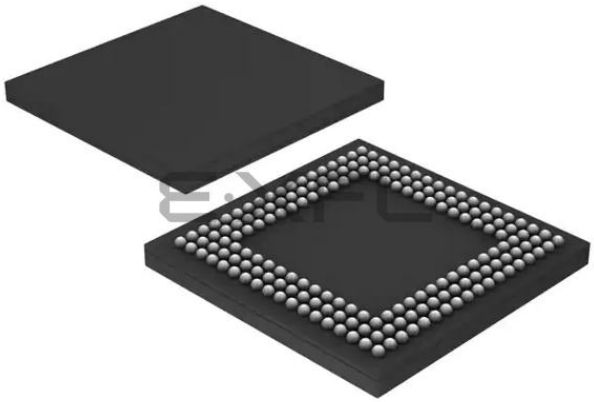

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SmartCard, SPI, SPIFI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	145
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	360K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	180-TFBGA
Supplier Device Package	180-TFBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc54018jet180e

3.1 Ordering options

Table 2. Ordering options

Type number	Package Name	SRAM/kB	FS USB	HS USB	Ethernet AVB	Classic CAN	CAN FD	LCD	EMC data bus width (bit)	Flexcomm Interface	GPIO	SHA
LPC54018 devices (HS/FS USB, Ethernet, CAN 2.0+CAN FD, LCD, SHA)												
LPC54018JET180	TFBGA180	360	yes	yes	yes	yes	yes	yes	8/16	11	145	yes
LPC54018JBD208	LQFP208	360	yes	yes	yes	yes	yes	yes	8/16/32	11	171	yes
LPC54016 devices (HS/FS USB, Ethernet, CAN 2.0+CAN FD, SHA)												
LPC54016JET180	TFBGA180	360	yes	yes	yes	yes	yes	-	8/16	11	145	yes
LPC54016JBD208	LQFP208	360	yes	yes	yes	yes	yes	-	8/16/32	11	171	yes
LPC54016JBD100	LQFP100	360	yes	yes	yes	yes	yes	-	8/16	10	64	yes
LPC54016JET100	TFBGA100	360	yes	yes	yes	yes	yes	-	8/16	10	64	yes
LPC54005 devices (HS/FS USB, SHA)												
LPC54005JET100	TFBGA100	360	yes	yes	-	-	-	-	8/16	10	64	yes
LPC54005JBD100	LQFP100	360	yes	yes	-	-	-	-	8/16	10	64	yes

6.2 Pin description

On the LPC540xx, digital pins are grouped into several ports. Each digital pin can support several different digital functions (including General Purpose I/O (GPIO)) and an additional analog function.

Table 4. Pin description

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state[1] [9]	Type	Description
PIO0_0	C4	D6	196	93	[2]	PU; Z	I/O	**PIO0_0 —** General-purpose digital input/output pin. **Remark:** In ISP mode, this pin is set to the Flexcomm 3 SPI SCK function.
							I	**CAN1_RD —** Receiver input for CAN 1.
							I/O	**FC3_SCK —** Flexcomm 3: USART or SPI clock.
							O	**CTimer_MAT0 —** Match output 0 from Timer 0.
							I	**SCT0_GPI0 —** Pin input 0 to SCTimer/PWM.
							O	**PDM0_CLK —** Clock for PDM interface 0, for digital microphone.
PIO0_1	A1	A1	207	100	[2]	PU; ZPU; Z	I/O	**PIO0_1 —** General-purpose digital input/output pin. **Remark:** In ISP mode, this pin is set to the Flexcomm 3 SPI SSEL0 function.
							O	**CAN1_TD —** Transmitter output for CAN 1.
							I/O	**FC3_CTS_SDA_SSEL0 —** Flexcomm 3: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							I	**CT0_CAP0 —** Capture input 0 to Timer 0.
							I	**SCT0_GPI1 —** Pin input 1 to SCTimer/PWM.
							I	**PDM0_DATA —** Data for PDM interface 0 (digital microphone).
PIO0_2/ TRST	A7	E9	174	83	[2]	PU; Z	I/O	**PIO0_2 —** General-purpose digital input/output pin. In boundary scan mode: TRST (Test Reset). **Remark:** In ISP mode, this pin is set to the Flexcomm 3 SPI MISO function.
							I/O	**FC3_TXD_SCL_MISO —** Flexcomm 3: USART transmitter, I2C clock, SPI master-in/slave-out data.
							I	**CT0_CAP1 —** Capture input 1 to Timer 0.
							O	**SCT0_OUT0 —** SCTimer/PWM output 0.
							I	**SCT0_GPI[2] —** Pin input 2 to SCTimer/PWM.
							I/O	**EMC_D[0] —** External Memory interface data [0].

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state[1] [9]	Type	Description
PIO0_3/ TCK	A6	A10	178	85	[2]	PU; Z	I/O	**PIO0_3 —** General-purpose digital input/output pin. In boundary scan mode: TCK (Test Clock In). **Remark:** In ISP mode, this pin is set to the Flexcomm 3 SPI MOSI function.
							I/O	**FC3_RXD_SDA_MOSI —** Flexcomm 3: USART receiver, I2C data I/O, SPI master-out/slave-in data.
							O	**CT0_MAT1 —** Match output 1 from Timer 0.
							O	**SCT0_OUT1 —** SCTimer/PWM output 1.
							I	**SCT0_GPI3 —** Pin input 3 to SCTimer/PWM.
								R — Reserved.
							I/O	**EMC_D[1] —** External Memory interface data [1].
PIO0_4/ TMS	B6	C8	185	87	[2]	PU; Z	I/O	**PIO0_4 —** General-purpose digital input/output pin. In boundary scan mode: TMS (Test Mode Select). **Remark:** The state of this pin at Reset in conjunction with PIO0_5 and PIO0_6 will determine the boot source for the part or if ISP handler is invoked. See the Boot Process chapter in UM11060 for more details.
							I	**CAN0_RD —** Receiver input for CAN 0.
							I/O	**FC4_SCK —** Flexcomm 4: USART or SPI clock.
							I	**CT3_CAP0 —** Capture input 0 to Timer 3.
							I	**SCT0_GPI4 —** Pin input 4 to SCTimer/PWM.
								R — Reserved.
							I/O	**EMC_D[2] —** External Memory interface data [2].
							O	**ENET_MDC —** Ethernet management data clock.
PIO0_5/ TDI	A5	E7	189	89	[2]	PU; Z	I/O	**PIO0_5 —** General-purpose digital input/output pin. In boundary scan mode: TDI (Test Data In). **Remark:** The state of this pin at Reset in conjunction with PIO0_4 and PIO0_6 will determine the boot source for the part or if ISP handler is invoked. See the Boot Process chapter in UM11060 for more details.
							O	**CAN0_TD —** Transmitter output for CAN 0.
							I/O	**FC4_RXD_SDA_MOSI —** Flexcomm 4: USART receiver, I2C data I/O, SPI master-out/slave-in data.
							O	**CT3_MAT0 —** Match output 0 from Timer 3.
							I	**SCT0_GPI5 —** Pin input 5 to SCTimer/PWM.
								R — Reserved.
							I/O	**EMC_D[3] —** External Memory interface data [3].
							I/O	**ENET_MDIO —** Ethernet management data I/O.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state[1] [9]	Type	Description
PIO0_12/ ADC0_2	J2	M3	52	25	[4]	PU; Z	I/O; AI	**PIO0_12/ADC0_2 —** General-purpose digital input/output pin. ADC input channel 2 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
							I/O	**FC3_TXD_SCL_MISO —** Flexcomm 3: USART transmitter, I2C clock, SPI master-in/slave-out data.
								R — Reserved.
							I	**FREQME_GPIO_CLK_B —** Frequency Measure pin clock input B.
							I	**SCT0_GPI7 —** Pin input 7 to SCTimer/PWM.
								R — Reserved.
							I/O	**SWDIO —** Serial Wire Debug I/O. This is the default function after booting.
PIO0_13	C10	F11	141	67	[3]	Z	I/O	**PIO0_13 —** General-purpose digital input/output pin. **Remark:** In ISP mode, this pin is set to the Flexcomm 1 I2C SDA function.
							I/O	**FC1_CTS_SDA_SSEL0 —** Flexcomm 1: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							I	**UTICK_CAP0 —** Micro-tick timer capture input 0.
							I	**CT0_CAP0 —** Capture input 0 to Timer 0.
							I	**SCT0_GPI0 —** Pin input 0 to SCTimer/PWM.
								R — Reserved.
								R — Reserved.
							I	**ENET_RXD0 —** Ethernet receive data 0.
PIO0_14	D9	E13	144	69	[3]	Z	I/O	**PIO0_14 —** General-purpose digital input/output pin. **Remark:** In ISP mode, this pin is set to the Flexcomm 1 I2C SCL function.
							I/O	**FC1_RTS_SCL_SSEL1 —** Flexcomm 1: USART request-to-send, I2C clock, SPI slave select 1.
							I	**UTICK_CAP1 —** Micro-tick timer capture input 1.
							I	**CT0_CAP1 —** Capture input 1 to Timer 0.
							I	**SCT0_GPI1 —** Pin input 1 to SCTimer/PWM.
								R — Reserved.
								R — Reserved.
							I	**ENET_RXD1 —** Ethernet receive data 1.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state[1] [9]	Type	Description
PIO0_18	C9	C14	150	72	[2]	PU; Z	I/O	**PIO0_18 —** General-purpose digital input/output pin.
							I/O	**FC4_CTS_SDA_SSEL0 —** Flexcomm 4: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							I	**SD_WR_PRT —** SD/MMC write protect.
							O	**CT1_MAT0 —** Match output 0 from Timer 1.
							O	**SCT0_OUT1 —** SCTimer/PWM output 1.
							O	**SCI1_SCLK —** SmartCard Interface 1 clock.
							O	**EMC_A[0] —** External memory interface address 0.
PIO0_19	C5	C6	193	91	[2]	PU; Z	I/O	**PIO0_19 —** General-purpose digital input/output pin.
							I/O	**FC4_RTS_SCL_SSEL1 —** Flexcomm 4: USART request-to-send, I2C clock, SPI slave select 1.
							I	**UTICK_CAP0 —** Micro-tick timer capture input 0.
							O	**CT0_MAT2 —** Match output 2 from Timer 0.
							O	**SCT0_OUT2 —** SCTimer/PWM output 2.
								R — Reserved.
							O	**EMC_A[1] —** External memory interface address 1.
							I/O	**FC7_TXD_SCL_MISO_WS —** Flexcomm 7: USART transmitter, I2C clock, SPI master-in/slave-out data I/O, I2S word-select/frame.
PIO0_20	C8	D13	153	74	[2]	PU; Z	I/O	**PIO0_20 —** General-purpose digital input/output pin.
							I/O	**FC3_CTS_SDA_SSEL0 —** Flexcomm 3: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							O	**CT1_MAT1 —** Match output 1 from Timer 1.
							I	**CT3_CAP3 —** Capture input 3 to Timer 3.
							I	**SCT0_GPI2 —** Pin input 2 to SCTimer/PWM.
							I/O	**SCI0_IO —** SmartCard Interface 0 data I/O.
							O	**EMC_A[2] —** External memory interface address 2.
							I/O	**FC7_RXD_SDA_MOSI_DATA —** Flexcomm 7: USART receiver, I2C data I/O, SPI master-out/slave-in data, I2S data I/O.
PIO0_21	B9	C13	158	77	[2]	PU; Z	I/O	**PIO0_21 —** General-purpose digital input/output pin.
							I/O	**FC3_RTS_SCL_SSEL1 —** Flexcomm 3: USART request-to-send, I2C clock, SPI slave select 1.
							I	**UTICK_CAP3 —** Micro-tick timer capture input 3.
							O	**CT3_MAT3 —** Match output 3 from Timer 3.
							I	**SCT0_GPI3 —** Pin input 3 to SCTimer/PWM.
							O	**SCI0_SCLK —** SmartCard Interface 0 clock.
							O	**EMC_A[3] —** External memory interface address 3.
							I/O	**FC7_SCK —** Flexcomm 7: USART, SPI, or I2S clock.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state[1] [9]	Type	Description
PIO0_29	B7	B13	167	82	[2]	PU; Z	I/O	**PIO0_29 —** General-purpose digital input/output pin. **Remark:** In ISP mode, this pin is set to the Flexcomm 0 USART RXD function.
							I/O	**FC0_RXD_SDA_MOSI —** Flexcomm 0: USART receiver, I2C data I/O, SPI master-out/slave-in data.
								R — Reserved.
							O	**CT2_MAT3 —** Match output 3 from Timer 2.
							O	**SCT0_OUT8 —** SCTimer/PWM output 8.
							O	**TRACEDATA[2] —** Trace data bit 2.
PIO0_30	A2	A2	200	95	[2]	PU; Z	I/O	**PIO0_30 —** General-purpose digital input/output pin. **Remark:** In ISP mode, this pin is set to the Flexcomm 0 USART TXD function.
							I/O	**FC0_TXD_SCL_MISO —** Flexcomm 0: USART transmitter, I2C clock, SPI master-in/slave-out data.
								R — Reserved.
							O	**CT0_MAT0 —** Match output 0 from Timer 0.
							O	**SCT0_OUT9 —** SCTimer/PWM output 9.
							O	**TRACEDATA[1] —** Trace data bit 1.
PIO0_31/ ADC0_5	K3	M5	55	28	[4]	PU; Z	I/O; AI	**PIO0_31/ADC0_5 —** General-purpose digital input/output pin. ADC input channel 5 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
							I/O	**FC0_CTS_SDA_SSEL0 —** Flexcomm 0: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							I/O	**SD_D[2] —** SD/MMC data 2.
							O	**CT0_MAT1 —** Match output 1 from Timer 0.
							O	**SCT0_OUT3 —** SCTimer/PWM output 3.
							O	**TRACEDATA[0] —** Trace data bit 0.
PIO1_0/ ADC0_6	J3	N3	56	29	[4]	PU; Z	I/O; AI	**PIO1_0/ADC0_6 —** General-purpose digital input/output pin. ADC input channel 6 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
							I/O	**FC0_RTS_SCL_SSEL1 —** Flexcomm 0: USART request-to-send, I2C clock, SPI slave select 1.
							I/O	**SD_D[3] —** SD/MMC data 3.
							I	**CT0_CAP2 —** Capture 2 input to Timer 0.
							I	**SCT0_GPI4 —** Pin input 4 to SCTimer/PWM.
							O	**TRACECLK —** Trace clock.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state[1] [9]	Type	Description
PIO1_8	H5	P8	72	36	[2]	PU; Z	I/O	**PIO1_8 —** General-purpose digital input/output pin.
							I/O	**FC0_CTS_SDA_SSEL0 —** Flexcomm 0: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							O	**SD_CLK —** SD/MMC clock.
								R — Reserved.
							O	**SCT0_OUT1 —** SCTimer/PWM output 1.
							I/O	**FC4_SSEL2 —** Flexcomm 4: SPI slave select 2.
							O	**EMC_A[7] —** External memory interface address 7.
PIO1_9	K7	K6	78	39	[2]	PU; Z	I/O	**PIO1_9 —** General-purpose digital input/output pin.
							O	**ENET_TXD0 —** Ethernet transmit data 0.
							I/O	**FC1_SCK —** Flexcomm 1: USART or SPI clock.
							I	**CT1_CAP0 —** Capture 0 input to Timer 1.
							O	**SCT0_OUT2 —** SCTimer/PWM output 2.
							I/O	**FC4_CTS_SDA_SSEL0 —** Flexcomm 4: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							O	**EMC_CASN —** External memory interface column access strobe (active low).
PIO1_10	H6	N9	84	41	[2]	PU; Z	I/O	**PIO1_10 —** General-purpose digital input/output pin.
							O	**ENET_TXD1 —** Ethernet transmit data 1.
							I/O	**FC1_RXD_SDA_MOSI —** Flexcomm 1: USART receiver, I2C data I/O, SPI master-out/slave-in data.
							O	**CT1_MAT0 —** Match output 0 from Timer 1.
							O	**SCT0_OUT3 —** SCTimer/PWM output 3.
								R — Reserved.
							O	**EMC_RASN —** External memory interface row address strobe (active low).
PIO1_11	B4	B4	198	94	[2][8]	PU; Z	I/O	**PIO1_11 —** General-purpose digital input/output pin.
							O	**ENET_TX_EN —** Ethernet transmit enable (RMII/MII interface).
							I/O	**FC1_TXD_SCL_MISO —** Flexcomm 1: USART transmitter, I2C clock, SPI master-in/slave-out data.
							I	**CT1_CAP1 —** Capture 1 input to Timer 1.
							I	**USB0_VBUS —** Monitors the presence of USB0 bus power.
								R — Reserved.
							O	**EMC_CLK[0] —** External memory interface clock 0.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state[1] [9]	Type	Description
PIO3_13	-	H4	75	-	[2]	PU; Z	I/O	**PIO3_13 —** General-purpose digital input/output pin.
							O	**SCT0_OUT9 —** SCTimer/PWM output 9.
							I/O	**FC9_CTS_SDA_SSEL0 —** Flexcomm 9: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							I	**CT3_CAP1 —** Capture input 1 to Timer 3.
								R — Reserved.
								R — Reserved.
							I	**EMC_FBCK —** External memory interface feedback clock.
							O	**TRACEDATA[1] —** Trace data bit 1.
PIO3_14	-	E3	13	-	[2]	PU; Z	I/O	**PIO3_14 —** General-purpose digital input/output pin.
							O	**SCT0_OUT4 —** SCTimer/PWM output 4.
							I/O	**FC9_RTS_SCL_SSEL1 —** Flexcomm 9: USART request-to-send, I2C clock, SPI slave select 1.
							O	**CT3_MAT1 —** Match output 1 from Timer 3.
								R — Reserved.
								R — Reserved.
								R — Reserved.
							O	**TRACEDATA[2] —** Trace data bit 2.
PIO3_15	-	D2	11	-	[2]	PU; Z	I/O	**PIO3_15 —** General-purpose digital input/output pin.
							I/O	**FC8_SCK —** Flexcomm 8: USART or SPI clock.
							I	**SD_WR_PRT —** SD/MMC write protect.
PIO3_16	-	E1	19	-	[2]	PU; Z	I/O	**PIO3_16 —** General-purpose digital input/output pin.
							I/O	**FC8_RXD_SDA_MOSI —** Flexcomm 8: USART receiver, I2C data I/O, SPI master-out/slave-in data.
							I/O	**SD_D[4] —** SD/MMC data 4.
PIO3_17	-	K1	31	-	[2]	PU; Z	I/O	**PIO3_17 —** General-purpose digital input/output pin.
							I/O	**FC8_TXD_SCL_MISO —** Flexcomm 8: USART transmitter, I2C clock, SPI master-in/slave-out data.
							I/O	**SD_D[5] —** SD/MMC data 5.
PIO3_18	-	M6	68	-	[2]	PU; Z	I/O	**PIO3_18 —** General-purpose digital input/output pin.
							I/O	**FC8_CTS_SDA_SSEL0 —** Flexcomm 8: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							I/O	**SD_D[6] —** SD/MMC data 6.
							O	**CT4_MAT0 —** Match output 0 from Timer 4.
							O	**CAN0_TD —** Transmitter output for CAN 0.
							O	**SCT0_OUT5 —** SCTimer/PWM output 5.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state[1] [9]	Type	Description
PIO4_1	-	G14	132	-	[2]	PU; Z	I/O	**PIO4_1 —** General-purpose digital input/output pin.
								R — Reserved.
							I/O	**FC6_SCK —** Flexcomm 6: USART, SPI, or I2S clock.
								R — Reserved.
								R — Reserved.
							I	**SCT0_GPI2 —** Pin input 2 to SCTimer/PWM.
							O	**EMC_CSN[2] —** External memory interface static chip select 2 (active low).
PIO4_2	-	F14	138	-	[2]	PU; Z	I/O	**PIO4_2 —** General-purpose digital input/output pin.
								R — Reserved.
							I/O	**FC6_RXD_SDA_MOSI_DATA —** Flexcomm 6: USART receiver, I2C data I/O, SPI master-out/slave-in data, I2S data I/O.
								R — Reserved.
								R — Reserved.
							I	**SCT0_GPI3 —** Pin input 3 to SCTimer/PWM.
							O	**EMC_CSN[3] —** External memory interface static chip select 3 (active low).
PIO4_3	-	F13	140	-	[2]	PU; Z	I/O	**PIO4_3 —** General-purpose digital input/output pin.
								R — Reserved.
							I/O	**FC6_TXD_SCL_MISO_WS —** Flexcomm 6: USART transmitter, I2C clock, SPI master-in/slave-out data I/O, I2S word-select/frame.
							I	**CT0_CAP3 —** Capture 3 input to Timer 0.
								R — Reserved.
							I	**SCT0_GPI4 —** Pin input 4 to SCTimer/PWM.
							O	**EMC_DYCSN[2] —** External Memory interface SDRAM chip select 2 (active low).
PIO4_4	-	D9	147	-	[2]	PU; Z	I/O	**PIO4_4 —** General-purpose digital input/output pin.
								R — Reserved.
							I/O	**FC4_SSEL3 —** Flexcomm 4: SPI slave select 3.
							I/O	**FC0_RTS_SCL_SSEL1 —** Flexcomm 0: USART request-to-send, I2C clock, SPI slave select 1.
								R — Reserved.
							I	**SCT0_GPI5 —** Pin input 5 to SCTimer/PWM.
							O	**EMC_DYCSN[3] —** External Memory interface SDRAM chip select 3 (active low).

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP	Reset state[1] [9]	Type	Description
PIO4_9	-	A12	173	-	[2][8]	PU; Z	I/O	**PIO4_9 —** General-purpose digital input/output pin.
							O	**ENET_TXD1 —** Ethernet transmit data 1.
							I/O	**FC2_RXD_SDA_MOSI —** Flexcomm 2: USART receiver, I2C data I/O, SPI master-out/slave-in data.
							O	**USB1_PORTPWRN —** USB1 VBUS drive indicator (Indicates VBUS must be driven).
							O	**USB1_FRAME —** USB1 frame toggle signal.
							I	**SCT0_GPI2 —** Pin input 2 to SCTimer/PWM.
PIO4_10	-	B9	181	-	[2]	PU; Z	I/O	**PIO4_10 —** General-purpose digital input/output pin.
							I	**ENET_RX_DV —** Ethernet receive data valid.
							I/O	**FC2_TXD_SCL_MISO —** Flexcomm 2: USART transmitter, I2C clock, SPI master-in/slave-out data.
							I	**USB1_OVERCURRENTN —** USB1 bus overcurrent indicator (active low).
							O	**USB1_LEDN —** USB1-configured LED indicator (active low).
								SCT0_GPI3 — Pin input 3 to SCTimer/PWM.
PIO4_11	-	A9	183	-	[2]	PU; Z	I/O	**PIO4_11 —** General-purpose digital input/output pin.
							I	**ENET_RXD0 —** Ethernet receive data 0.
							I/O	**FC2_CTS_SDA_SSEL0 —** Flexcomm 2: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							I	**USB0_IDVALUE —** Indicates to the transceiver whether connected as an A-device (USB0_ID LOW) or B-device (USB0_ID HIGH).
								R — Reserved.
							I	**SCT0_GPI4 —** Pin input 4 to SCTimer/PWM.
PIO4_12	-	A6	188	-	[2]	PU; Z	I/O	**PIO4_12 —** General-purpose digital input/output pin.
							I	**ENET_RXD1 —** Ethernet receive data 1.
							I/O	**FC2_RTS_SCL_SSEL1 —** Flexcomm 2: USART request-to-send, I2C clock, SPI slave select 1.
								R — Reserved.
							I	**SCT0_GPI5 —** Pin input 5 to SCTimer/PWM.
PIO4_13	-	B6	190	-	[2]	PU; Z	I/O	**PIO4_13 —** General-purpose digital input/output pin.
							O	**ENET_TX_EN —** Ethernet transmit enable (RMII/MII interface).
							O	**CT4_MAT0 —** Match output 0 from Timer 4.
								R — Reserved.
							I	**SCT0_GPI6 —** Pin input 6 to SCTimer/PWM.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state[1] [9]	Type	Description
PIO4_23	-	-	42	-	[2]	PU; Z	I/O	**PIO4_23 —** General-purpose digital input/output pin.
							I	**ENET_RXD0 —** Ethernet receive data 0.
							I	**SD_WR_PRT —** SD/MMC write protect.
							I/O	**FC2_CTS_SDA_SSEL0 —** Flexcomm 2: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
								R — Reserved.
							O	**CT1_MAT0 —** Match output 0 from Timer 1.
							I/O	**EMC_D[18] —** External Memory interface data [18].
PIO4_24	-	-	67	-	[2]	PU; Z	I/O	**PIO4_24 —** General-purpose digital input/output pin.
							I	**ENET_RXD1 —** Ethernet receive data 1.
							I	**SD_CARD_INT_N —** Card interrupt line.
							I/O	**FC7_RTS_SCL_SSEL1 —** Flexcomm 7: USART request-to-send, I2C clock, SPI slave select 1.
								R — Reserved.
							O	**CT1_MAT1 —** Match output 1 from Timer 1.
							I/O	**EMC_D[19] —** External Memory interface data [19].
PIO4_25	-	-	69	-	[2]	PU; Z	I/O	**PIO4_25 —** General-purpose digital input/output pin.
							I	**ENET_RXD2 —** Ethernet Receive Data 2 (MII interface).
							I/O	**SD_D[0] —** SD/MMC data 0.
							I/O	**FC7_CTS_SDA_SSEL0 —** Flexcomm 7: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
								R — Reserved.
							O	**CT1_MAT2 —** Match output 2 from Timer 1.
							I/O	**EMC_D[20] —** External Memory interface data [20].
PIO4_26	-	-	73	-	[2]	PU; Z	I/O	**PIO4_26 —** General-purpose digital input/output pin.
							I	**ENET_RXD3 —** Ethernet Receive Data 3 (MII interface).
							I/O	**SD_D[1] —** SD/MMC data 1.
								R — Reserved.
							I	**UTICK_CAP2 —** Micro-tick timer capture input 2.
							O	**CT1_MAT3 —** Match output 3 from Timer 1.
							I/O	**EMC_D[21] —** External Memory interface data [21].

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state[1] [9]	Type	Description
PIO4_27	-	-	85	-	[2]	PU; Z	I/O	**PIO4_27 —** General-purpose digital input/output pin.
							O	**ENET_TX_EN —** Ethernet transmit enable (RMII/MII interface).
							I/O	**SD_D[2] —** SD/MMC data 2.
								R — Reserved.
							I/O	**FC1_SCK —** Flexcomm 1: USART or SPI clock.
							I	**CT1_CAP0 —** Capture input 0 to Timer 1.
							I/O	**EMC_D[22] —** External Memory interface data [22].
PIO4_28	-	-	92	-	[2]	PU; Z	I/O	**PIO4_28 —** General-purpose digital input/output pin.
							O	**ENET_TX_ER —** Ethernet Transmit Error (MII interface).
							I/O	**SD_D[3] —** SD/MMC data 3.
								R — Reserved.
							I/O	**FC1_RXD_SDA_MOSI —** Flexcomm 1: USART receiver, I2C data I/O, SPI master-out/slave-in data.
							I	**CT1_CAP1 —** Capture 1 input to Timer 1.
							I/O	**EMC_D[23] —** External Memory interface data [23].
PIO4_29	-	-	102	-	[2]	PU; Z	I/O	**PIO4_29 —** General-purpose digital input/output pin.
							I	**ENET_RX_ER —** Ethernet receive error (RMII/MII interface).
							I/O	**SD_D[4] —** SD/MMC data 4.
								R — Reserved.
							I/O	**FC1_TXD_SCL_MISO —** Flexcomm 1: USART transmitter, I2C clock, SPI master-in/slave-out data.
							I	**CT1_CAP2 —** Capture 2 input to Timer 1.
							I/O	**EMC_D[24] —** External Memory interface data [24].
PIO4_30	-	-	80	-	[2]	PU; Z	I/O	**PIO4_30 —** General-purpose digital input/output pin.
							I	**ENET_TX_CLK —** Ethernet Transmit Clock (MII interface).
							I/O	**SD_D[5] —** SD/MMC data 5.
							O	**CT3_MAT0 —** Match output 0 from Timer 3.
							I/O	**FC1_RTS_SCL_SSEL1 —** Flexcomm 1: USART request-to-send, I2C clock, SPI slave select 1.
							I	**CT1_CAP3 —** Capture 3 input to Timer 1.
							I/O	**EMC_D[25] —** External Memory interface data [25].

[1] PU = input mode, pull-up enabled (pull-up resistor pulls up pin to V_{DD}). Z = high impedance; pull-up or pull-down disabled, AI = analog input, I = input, O = output, F = floating. Reset state reflects the pin state at reset without boot code operation. For pin states in the different power modes, see Section 6.2.2 “Pin states in different power modes”. For termination on unused pins, see Section 6.2.1 “Termination of unused pins”.

[2] 5 V tolerant pad with programmable glitch filter (5 V tolerant if V_{DD} present; if V_{DD} not present, do not exceed 3.6 V); provides digital I/O functions with TTL levels and hysteresis; normal drive strength. See Figure 45. Pulse width of spikes or glitches suppressed by input filter is from 3 ns to 16 ns (simulated value).

[3] True open-drain pin. I2C-bus pins compliant with the I2C-bus specification for I2C standard mode, I2C Fast-mode, and I2C Fast-mode Plus. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I2C lines. Open-drain configuration applies to all functions on this pin.

[4] 5 V tolerant pin providing standard digital I/O functions with configurable modes, configurable hysteresis, and analog input. When configured as an analog input, the digital section of the pin is disabled, and the pin is not 5 V tolerant.

[5] Reset pad.5 V tolerant pad with glitch filter with hysteresis. Pulse width of spikes or glitches suppressed by input filter is from 3 ns to 20 ns (simulated value)

[6] 5 V tolerant transparent analog pad.

[7] The oscillator input pin (XTALIN) cannot be driven by an external clock. Must connect a crystal between XTALIN and XTALOUT.

[8] VBUS must be connected to supply voltage when using the USB peripheral.

[9] For initial device revision 0A (Boot ROM version 21.0), PU = input mode, pull-up enabled (pull-up resistor pulls up pin to VDD). For future device revision 1B (Boot ROM version 21.1), Z = high impedance; pull-up or pull-down disabled. See the Errata sheet LPC540xx (IOCON.1) for more details. For future device revision 1B (Boot ROM version 21.1), GPIO pins PIO0_12, PIO0_11, PIO0_2, PIO0_3, PIO0_4, PIO0_5, and PIO0_6 have the input buffer enabled (DIGIMODE, bit 8 is enabled in IOCON register) and will be floating by default. If unused, it is recommended to externally terminate this pins to prevent leakage.

6.2.1 Termination of unused pins

Table 5 shows how to terminate pins that are **not** used in the application. In many cases, unused pins should be connected externally or configured correctly by software to minimize the overall power consumption of the part.

Unused pins with GPIO function should be configured as outputs set to LOW with their internal pull-up disabled. To configure a GPIO pin as output and drive it LOW, select the GPIO function in the IOCON register, select output in the GPIO DIR register, and write a 0 to the GPIO PORT register for that pin. Disable the pull-up in the pin’s IOCON register.

In addition, it is recommended to configure all GPIO pins that are not bonded out on smaller packages as outputs driven LOW with their internal pull-up disabled.

Table 5. Termination of unused pins

Pin	Default state[1][2]	Recommended termination of unused pins
$\overline{\text{RESET}}$	I; PU	The $\overline{\text{RESET}}$ pin can be left unconnected if the application does not use it.
all PIOn_m (not open-drain)	I; PU; Z	Can be left unconnected if driven LOW and configured as GPIO output with pull-up disabled by software.
PIOn_m (I2C open-drain)	IA	Can be left unconnected if driven LOW and configured as GPIO output by software.
RTCXIN	-	Connect to ground. When grounded, the RTC oscillator is disabled.
RTCXOUT	-	Can be left unconnected.
XTALIN	-	Connect to ground. When grounded, the RTC oscillator is disabled.
XTALOUT	-	Can be left unconnected.
VREFP	-	Tie to VDD.
VREFN	-	Tie to VSS.
VDDA	-	Tie to VDD.
VSSA	-	Tie to VSS.

7.14.8.4 USART

Features

- Maximum bit rates of 6.25 Mbit/s in asynchronous mode.
- The maximum supported bit rate for USART master synchronous mode is 24 Mbit/s, and the maximum supported bit rate for USART slave synchronous mode is 12.5 Mbit/s.
- 7, 8, or 9 data bits and 1 or 2 stop bits.
- Synchronous mode with master or slave operation. Includes data phase selection and continuous clock option.
- Multiprocessor/multidrop (9-bit) mode with software address compare.
- RS-485 transceiver output enable.
- Autobaud mode for automatic baud rate detection
- Parity generation and checking: odd, even, or none.
- Software selectable oversampling from 5 to 16 clocks in asynchronous mode.
- One transmit and one receive data buffer.
- RTS/CTS for hardware signaling for automatic flow control. Software flow control can be performed using Delta CTS detect, Transmit Disable control, and any GPIO as an RTS output.
- Received data and status can optionally be read from a single register
- Break generation and detection.
- Receive data is 2 of 3 sample "voting". Status flag set when one sample differs.
- Built-in Baud Rate Generator with auto-baud function.
- A fractional rate divider is shared among all USARTs.
- Interrupts available for Receiver Ready, Transmitter Ready, Receiver Idle, change in receiver break detect, Framing error, Parity error, Overrun, Underrun, Delta CTS detect, and receiver sample noise detected.
- Loopback mode for testing of data and flow control.
- In synchronous slave mode, wakes up the part from deep-sleep mode.
- Special operating mode allows operation at up to 9600 baud using the 32.768 kHz RTC oscillator as the UART clock. This mode can be used while the device is in deep-sleep mode and can wake-up the device when a character is received.
- USART transmit and receive functions work with the system DMA controller.

7.14.8.5 I^2S-bus interface

The I^2S bus provides a standard communication interface for streaming data transfer applications such as digital audio or data collection. The I^2S bus specification defines a 3-wire serial bus, having one data, one clock, and one word select/frame trigger signal, providing single or dual (mono or stereo) audio data transfer as well as other configurations. In the LPC540xx, the I^2S function is included in Flexcomm Interface 6 and Flexcomm Interface 7. Each of the Flexcomm Interface implements four I^2S channel pairs.

The I^2S interface within one Flexcomm Interface provides at least one channel pair that can be configured as a master or a slave. Other channel pairs, if present, always operate as slaves. All of the channel pairs within one Flexcomm Interface share one set of I^2S

Table 20. Static characteristics: pin characteristics *…continued*

T_{amb} = −40 °C to +105 °C, unless otherwise specified. 1.71 V ≤ V_{DD} ≤ 3.6 V unless otherwise specified. Values tested in production unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
USB0_DM and USB0_DP pins							
V_I	input voltage			0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage			2.0	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.8	V
V_{hys}	hysteresis voltage			0.4	-	-	V
Z_{out}	output impedance		[11]	33.0	-	44	Ω
V_{OH}	HIGH-level output voltage		[12]	2.8	-	-	V
V_{OL}	LOW-level output voltage		[13]	-	-	0.3	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD} - 0.3$ V	[9][10]	38	-	74	mA
		$V_{OH} = V_{DD} - 0.3$ V	[10][11]	6.0		9.0	mA
I_{OL}	LOW-level output current	$V_{OL} = 0.3$ V	[9][10]	38	-	74	mA
		$V_{OL} = 0.3$ V	[10][11]	6.0		9.0	mA
I_{OLS}	LOW-level short-circuit output current	drive LOW; pad connected to ground	[10]	-	-	100	mA
I_{OHS}	HIGH-level short-circuit output current	drive HIGH; pad connected to ground	[10]	-	-	100	mA
Pin capacitance							
C_{io}	input/output capacitance	I^2C-bus pins	[8]	-	-	6.0	pF
		pins with digital functions only	[6]	-	-	2.0	pF
		Pins with digital and analog functions	[6]	-	-	7.0	pF

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltage.

[2] Based on characterization. Not tested in production.

[3] With respect to ground.

[4] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[5] To V_{SS}.

[6] The values specified are simulated and absolute values, including package/bondwire capacitance.

[7] The weak pull-up resistor is connected to the V_{DD} rail and pulls up the I/O pin to the V_{DD} level.

[8] The value specified is a simulated value, excluding package/bondwire capacitance.

[9] Without 33 Ω ± 2 % series external resistor.

[10] The parameter values specified are simulated and absolute values.

[11] With 33 Ω ± 2 % series external resistor.

[12] With 15 KΩ ± 5 % resistor to V_{SS}.

[13] With 1.5 KΩ ± 5% resistor to 3.6 V external pull-up.

[14] Guaranteed by design, not tested in production.

Table 24. Dynamic characteristics: Static external memory interface *…continued*

C_L = 20 pF balanced loading on all pins, T_{amb} = −40 °C to 105 °C, V_{DD} = 2.7 V to 3.6 V. Max EMC clock = 100 MHz. Input slew = 1 ns; SLEW set to fast-mode. Parameters sampled at the 90 % and 10 % level of the rising or falling edge. Excluding delays introduced by external device and PCB; Values based on simulation.

Symbol	Parameter[1]	Conditions[1]		Min	Typ	Max	Unit
$t_{h(D)}$	data input hold time	RD_6	[2][4]	−5.5	-	-	ns
$t_{CSHBLSH}$	$\overline{CS}$ HIGH to $\overline{BLS}$ HIGH time	PB = 1	[6]	0.7	-	1.5	ns
t_{CSHOEH}	$\overline{CS}$ HIGH to $\overline{OE}$ HIGH time		[2]	0.5	-	0.9	ns
t_{OEHANV}	$\overline{OE}$ HIGH to address invalid time	RD_8	[2]	−0.4	-	0	ns
t_{deact}	deactivation time	RD_7	[2]	0.5	-	0.9	ns
Write cycle parameters[2]							
t_{CSLAV}	$\overline{CS}$ LOW to address valid time	WR_1		0.1	-	0.5	ns
t_{CSLDV}	$\overline{CS}$ LOW to data valid time	WR_2		1	-	2.2	ns
t_{CSLWEL}	$\overline{CS}$ LOW to $\overline{WE}$ LOW time	WR_3; PB =1	[2][6]	−0.5 + (WAITWEN + 1) × $T_{cy(clk)}$	-	(WAITWEN + 1) × $T_{cy(clk)}$	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW time	WR_4; PB = 1	[2][6]	−1.9	-	0	ns
t_{WELWEH}	$\overline{WE}$ LOW to $\overline{WE}$ HIGH time	WR_5; PB =1	[2][6]	−0.1 + (WAITWEN + 1) × $T_{cy(clk)}$	-	(WAITWEN + 1) × $T_{cy(clk)}$	ns
$t_{BLSLBLSH}$	$\overline{BLS}$ LOW to $\overline{BLS}$ HIGH time	PB = 1	[2][6]	3.1	-	6.7	ns
t_{WEHDNV}	$\overline{WE}$ HIGH to data invalid time	WR_6; PB =1	[2][6]	1.6 + $T_{cy(clk)}$	-	2.8 + $T_{cy(clk)}$	ns
t_{WEHEOW}	$\overline{WE}$ HIGH to end of write time	WR_7; PB = 1	[2][5][6]	0.5 +$T_{cy(clk)}$	-	0.8 + $T_{cy(clk)}$	ns
$t_{BLSHDNV}$	$\overline{BLS}$ HIGH to data invalid time	PB = 1	[6]	−0.8	-	0	ns
t_{WEHANV}	$\overline{WE}$ HIGH to address invalid time	PB = 1	[6]	0.5	-	0.8	ns
t_{deact}	deactivation time	WR_8; PB = 0; PB = 1	[2][6]	−0.8	-	0	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW	WR_9; PB = 0	[2][6]	−1.9 + (WAITWEN + 1) × $T_{cy(clk)}$	-	(WAITWEN + 1) × $T_{cy(clk)}$	ns
$t_{BLSLBLSH}$	$\overline{BLS}$ LOW to $\overline{BLS}$ HIGH time	WR_{10}; PB = 0	[2][6]	3.1+ (WAITWR − WAITWEN + 1) × $T_{cy(clk)}$	-	6.7+ (WAITWR − WAITWEN + 1) × $T_{cy(clk)}$	ns
$t_{BLSHEOW}$	$\overline{BLS}$ HIGH to end of write time	WR_{11}; PB = 0	[2][5][6]	−0.8 + $T_{cy(clk)}$	-	$T_{cy(clk)}$	ns
$t_{BLSHDNV}$	$\overline{BLS}$ HIGH to data invalid time	WR12; PB = 0	[2][6]	0.2 + $T_{cy(clk)}$	-	0.5 + $T_{cy(clk)}$	ns

[1] Parameters are shown as RD_n or WD_n in Figure 23 as indicated in the Conditions column.

11.15 SPIFI

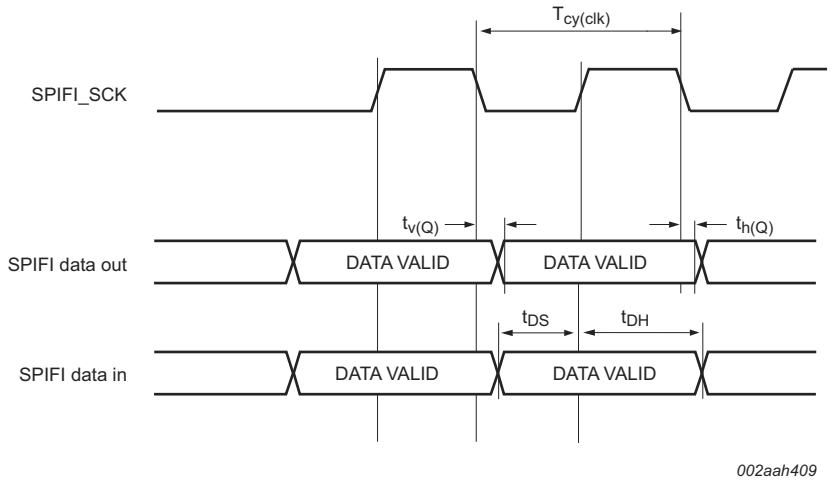
The actual SPIFI bit rate depends on the delays introduced by the external trace, the external device, system clock (CCLK), and capacitive loading. Excluding delays introduced by external device and PCB, the maximum supported bit rate for SPIFI mode is 100 Mbit/s.

Table 42. Dynamic characteristics: SPIFI[1]

T_{amb} = −40 °C to 105 °C; V_{DD} = 1.71 V to 3.6 V; C_L = 30 pF balanced loading on all pins; Input slew = 1 ns, SLEW set to standard mode for all pins; Parameters sampled at the 50 % level of the rising or falling edge.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SPIFI 1.71 V ≤ VDD ≤ 2.7 V						
t_{DS}	data set-up time	CCLK ≤ 100 MHz	4	-	-	ns
		CCLK > 100 MHz	4	-	-	ns
t_{DH}	data hold time	CCLK ≤ 100 MHz	6.4	-	-	ns
		CCLK > 100 MHz	6.6	-	-	ns
$t_{v(Q)}$	data output valid time	CCLK ≤ 100 MHz	5.7	-	13.7	ns
		CCLK > 100 MHz	5.7	-	13.7	ns
SPIFI 2.7 V ≤ VDD ≤ 3.6 V						
t_{DS}	data set-up time	CCLK ≤ 100 MHz	4	-	-	ns
		CCLK > 100 MHz	4	-	-	ns
t_{DH}	data hold time	CCLK ≤ 100 MHz	3.5	-	-	ns
		CCLK > 100 MHz	3.6	-	-	ns
$t_{v(Q)}$	data output valid time	CCLK ≤ 100 MHz	3.3	-	11.5	ns
		CCLK > 100 MHz	3.3	-	11.5	ns

[1] Based on simulation; not tested in production.



In mode 0, MODE3 bit (23) in SPIFI CTRL register is set to '0' (default). The SPIFI drives SCK low after the rising edge at which the last bit of each command is captured, and keeps it LOW while CS is HIGH.

Fig 34. SPIFI control register (Mode 0)

11.23 SD/MMC and SDIO

Table 49. Dynamic characteristics: SD/MMC and SDIO

T_{amb} = −40 °C to +105 °C, V_{DD} = 2.7 V to 3.6 V; C_L = 20 pF. SAMPLE_DELAY = 0, DRV_DELAY = 0 in the SDDELAY register, SDIOCLKCTRL = 0x84, sampled at 90 % and 10 % of the signal level, SLEW = 1 ns for SD_CLK pin, SLEW = 1 ns for SD_DATn and SD_CMD pins. Simulated values in high-speed mode.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{clk}	clock frequency	on pin SD_CLK; data transfer mode	-	-	50	MHz
$t_{su(D)}$	data input set-up time	on pins SD_DATn as inputs				
		CCLK ≤ 100 MHz	14.4	-	-	ns
		CCLK > 100 MHz	14.4	-	-	ns
		on pins SD_CMD as inputs				
		CCLK ≤ 100 MHz	14.4	-	-	ns
		CCLK > 100 MHz	14.4	-	-	ns
$t_{h(D)}$	data input hold time	on pins SD_DATn as inputs				
		CCLK ≤ 100 MHz	1.5	-	-	ns
		CCLK > 100 MHz	1.5	-	-	ns
		on pins SD_CMD as inputs				
		CCLK ≤ 100 MHz	1.5	-	-	ns
		CCLK > 100 MHz	1.5	-	-	ns
$t_{v(Q)}$	data output valid time	on pins SD_DATn as outputs				
		CCLK ≤ 100 MHz	1.9	-	3.5	ns
		CCLK > 100 MHz	1.9	-	3.5	ns
		on pins SD_CMD as outputs				
		CCLK ≤ 100 MHz	1.9	-	3.5	ns
		CCLK > 100 MHz	1.9	-	3.5	ns

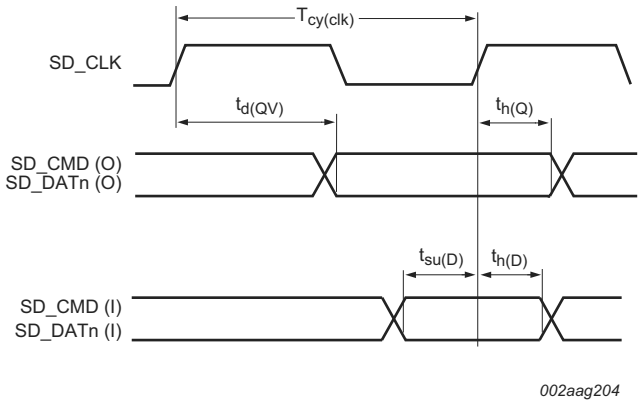


Fig 40. SD/MMC and SDIO timing

12. Analog characteristics

12.1 BOD

Table 51. BOD static characteristics

T_{amb} = 25 °C; based on characterization; not tested in production.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{th}	threshold voltage	interrupt level 0					
		assertion		1.5	-	1.63	V
		de-assertion		1.55	-	1.69	V
		reset level 0					
		assertion		1.5	-	1.62	V
		de-assertion		1.55	-	1.69	V
V_{th}	threshold voltage	interrupt level 1					
		assertion		1.54	-	1.68	V
		de-assertion		1.6	-	1.75	V
		reset level 1					
		assertion		1.55	-	1.68	V
		de-assertion		1.61	-	1.74	V
V_{th}	threshold voltage	interrupt level 2					
		assertion		1.79	-	1.95	V
		de-assertion		1.85	-	2.02	V
		reset level 2					
		assertion		2.04	-	2.21	V
		de-assertion		2.19	-	2.38	V
V_{th}	threshold voltage	interrupt level 3					
		assertion		2.62	-	2.86	V
		de-assertion		2.77	-	3.03	V
		reset level 3					
		assertion		2.62	-	2.85	V
		de-assertion		2.78	-	3.02	V

13.3 Connecting power, clocks, and debug functions

Figure 46 shows the basic board connections used to power the LPC540xx devices, connect the external crystal and the 32 kHz oscillator for the RTC, and provide debug capabilities via the serial wire port.