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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ACE1001
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	6
Program Memory Size	1KB (1K x 8)
Program Memory Type	EEPROM
EEPROM Size	64 x 8
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	8-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	8-TSSOP
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=ace1001mt8x

ACE1001(L) DC Electrical Characteristics

V_{CC} = 1.8/2.2 to 5.5V

All measurements valid for ambient operating temperature unless otherwise stated.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Units
I_{CC}[3]	Supply Current – no data EEPROM write in progress	1.8V 2.2V 2.7V 3.3V 5.5V		0.2 0.4 0.7 1.2 3.7	0.5 1.0 1.2 2.0 5.5	mA mA mA mA mA
I_{CCH}	HALT Mode current	3.3V @ +25°C 3.3V @ -40°C to +85°C		 10	100 1000	nA nA
		5.5V @ +25°C 5.5V @+125°C		 250	1000 3000	nA nA
I_{CCL}[4]	IDLE Mode Current	3.3V 5.5V		120 140	200 300	µA µA
V_{CCW}	EEPROM Write Voltage	Code EEPROM in Programming Mode	4.5	5.0	5.5	V
		Data EEPROM in Operating Mode	2.4		5.5	V
S_{VCC}	Power Supply Slope		1µs/V		10ms/V	
V_{IL}	Input Low with Schmitt Trigger Buffer	V_{CC} = 1.8V V_{CC} = 2.2 -5.5V			$0.15V_{CC}$ $0.20V_{CC}$	V V
V_{IH}	Input High with Schmitt Trigger Buffer	$V_{CC} \leq 2.2V$ $V_{CC} > 2.2V$	$0.9V_{CC}$ $0.8V_{CC}$			V V
I_{IP}	Input Pull-up Current	V_{CC} =5.5V, V_{IN} =0V	30	65	350	µA
I_{TL}	TRI-STATE Leakage	V_{CC} =5.5V		2	200	nA
V_{OL}	Output Low Voltage	V_{CC} = 1.8 - 2.2V				
	G0, G1, G2, G4	0.8 mA sink			$0.2V_{CC}$	V
	G5	1.0 mA sink			$0.2V_{CC}$	V
	Output Low Voltage	V_{CC} = 2.2V – 3.3V				
	G0, G1, G2, G4	3.0 mA sink			$0.2V_{CC}$	V
	G5	5.0 mA sink			$0.2V_{CC}$	V
	Output Low Voltage	V_{CC} = 3.3V – 5.5V				
	G0, G1, G2, G4	5.0 mA sink			$0.2V_{CC}$	V
	G5	10.0 mA sink			$0.2V_{CC}$	V
V_{OH}	Output High Voltage	V_{CC} = 1.8 - 2.2V				
	G0, G1, G2, G4	0.1 mA source	$0.8V_{CC}$			V
	G5	0.2 mA source	$0.8V_{CC}$			V
	Output High Voltage	V_{CC} = 3.3V – 5.5V				
	G0, G1, G2, G4	0.4 mA source	$0.8V_{CC}$			V
	G5	0.8 mA source	$0.8V_{CC}$			V
	Output High Voltage	V_{CC} = 3.3V – 5.5V				
	G0, G1, G2, G4	0.4 mA source	$0.8V_{CC}$			V
	G5	1.0 mA source	$0.8V_{CC}$			V

[3] I_{CC} active current is dependent on the program code.

[4] Based on a continuous IDLE looping program.

ACE1001(L) AC Electrical Characteristics

V_{CC} = 1.8/2.2 to 5.5V

All measurements valid for ambient operating temperature unless otherwise stated.

Parameter	Conditions	MIN	TYP	MAX	Units
Instruction cycle time from internal clock - setpoint	5.0V at +25°C	0.96	1.0	1.04	µs
Internal clock frequency variation	2.4V to 5.5V at constant temperature	-5		+5	%
	2.4V to 5.5V at full temperature range	-10		+10	%
Crystal oscillator frequency	(Note 5)			4	MHz
External clock frequency	(Note 5)			4	MHz
EEPROM write time			3	10	ms
Internal clock start up time	(Note 6)			2	ms
Oscillator start up time	(Note 6)			2400	cycles

[5] The maximum permissible frequency is guaranteed by design but not 100% tested.

[6] The parameter is guaranteed by design but not 100% tested.

ACE1001(L) Electrical Characteristics for programming

All data following is valid between 4.5V and 5.5V at ambient temperature. The following characteristics are guaranteed by design but are not 100% tested. See "EEPROM write time" in the AC Electrical Characteristics for definition of the programming ready time.

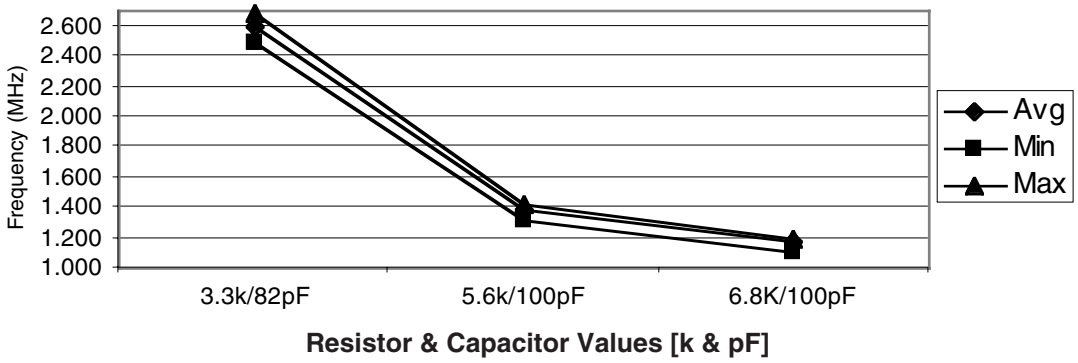
Parameter	Description	MIN	MAX	Units
t_{HI}	CLOCK high time	500	DC	ns
t_{LO}	CLOCK low time	500	DC	ns
t_{DIS}	SHIFT_IN setup time	100		ns
t_{DIH}	SHIFT_IN hold time	100		ns
t_{DOS}	SHIFT_OUT setup time	100		ns
t_{DOH}	SHIFT_OUT hold time	900		ns
t_{SV1}, t_{SV2}	LOAD supervoltage timing	50		µs
t_{LOAD1}, t_{LOAD2}, t_{LOAD3}, t_{LOAD4}	LOAD timing	5		µs
$V_{SUPERVOLTAGE}$	Supervoltage level	11.5	12.5	V

3.0 AC & DC Electrical Characteristic Graphs

The graphs in this section are for design guidance and are based on preliminary test data.

Figure 4: RC Oscillator Frequency vs. Temperature

(a) V_{CC} = 5.0V



(b)V_{CC}=2.5V

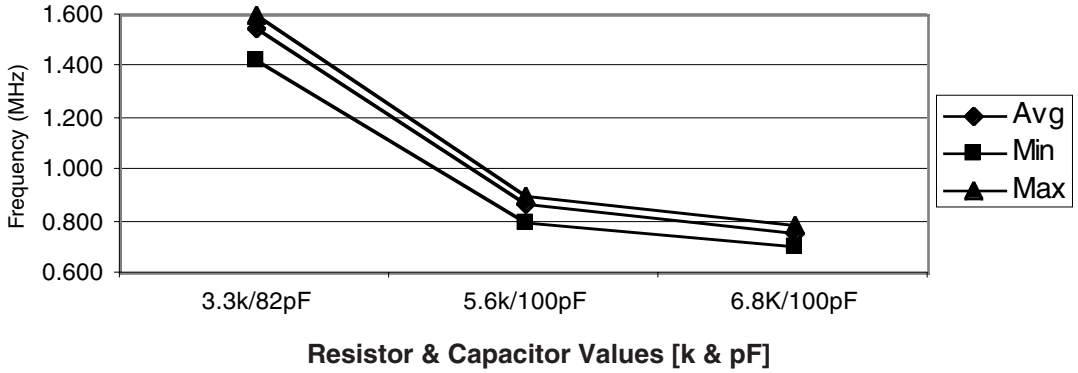


Figure 5: Internal Oscillator Frequency

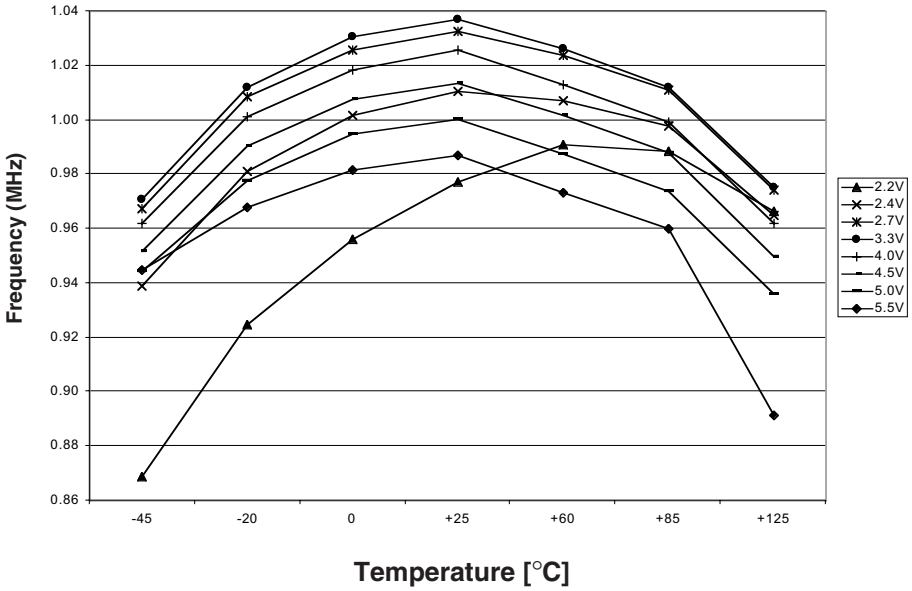
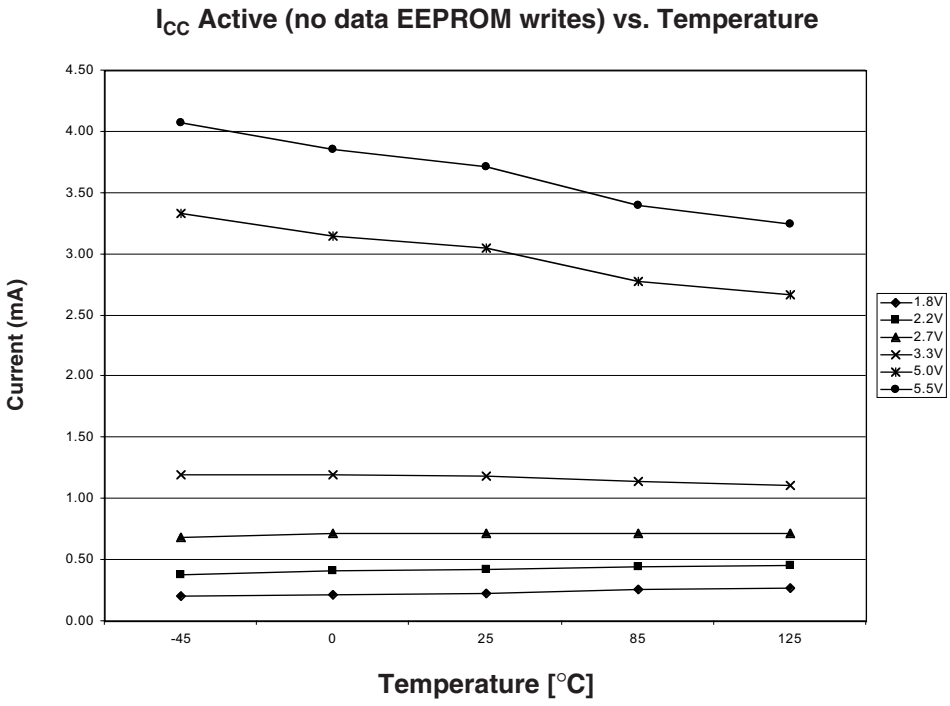


Figure 7: I_{CC} Active Current



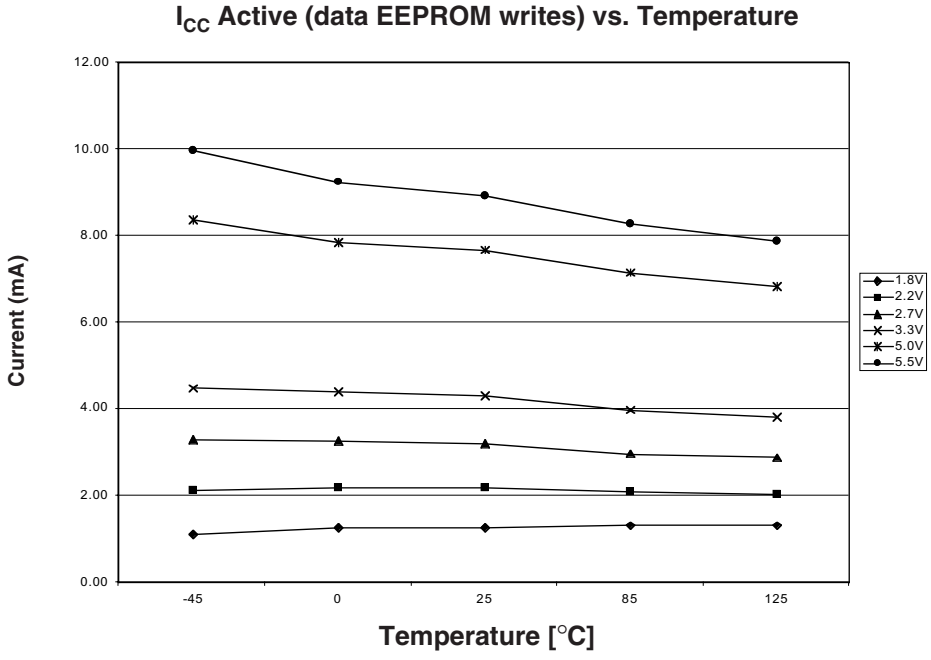


Figure 8: HALT Mode Currents

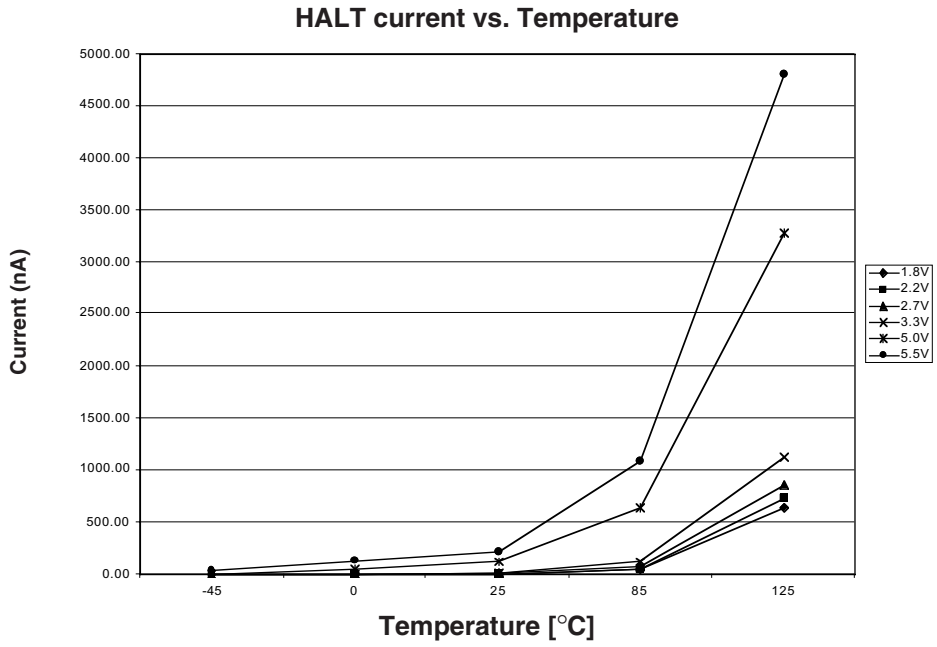


Figure 9: IDLE Mode Current

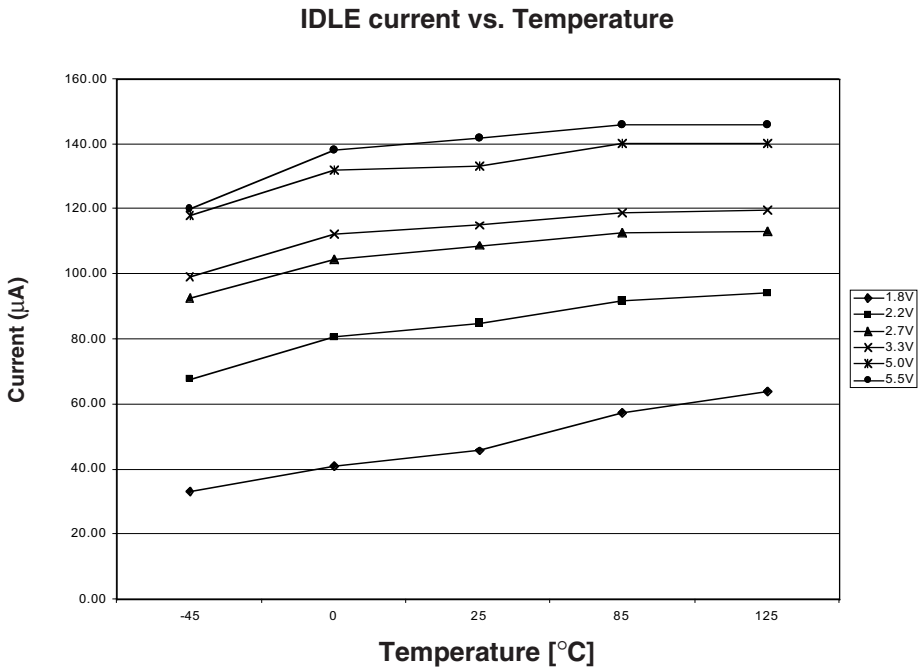
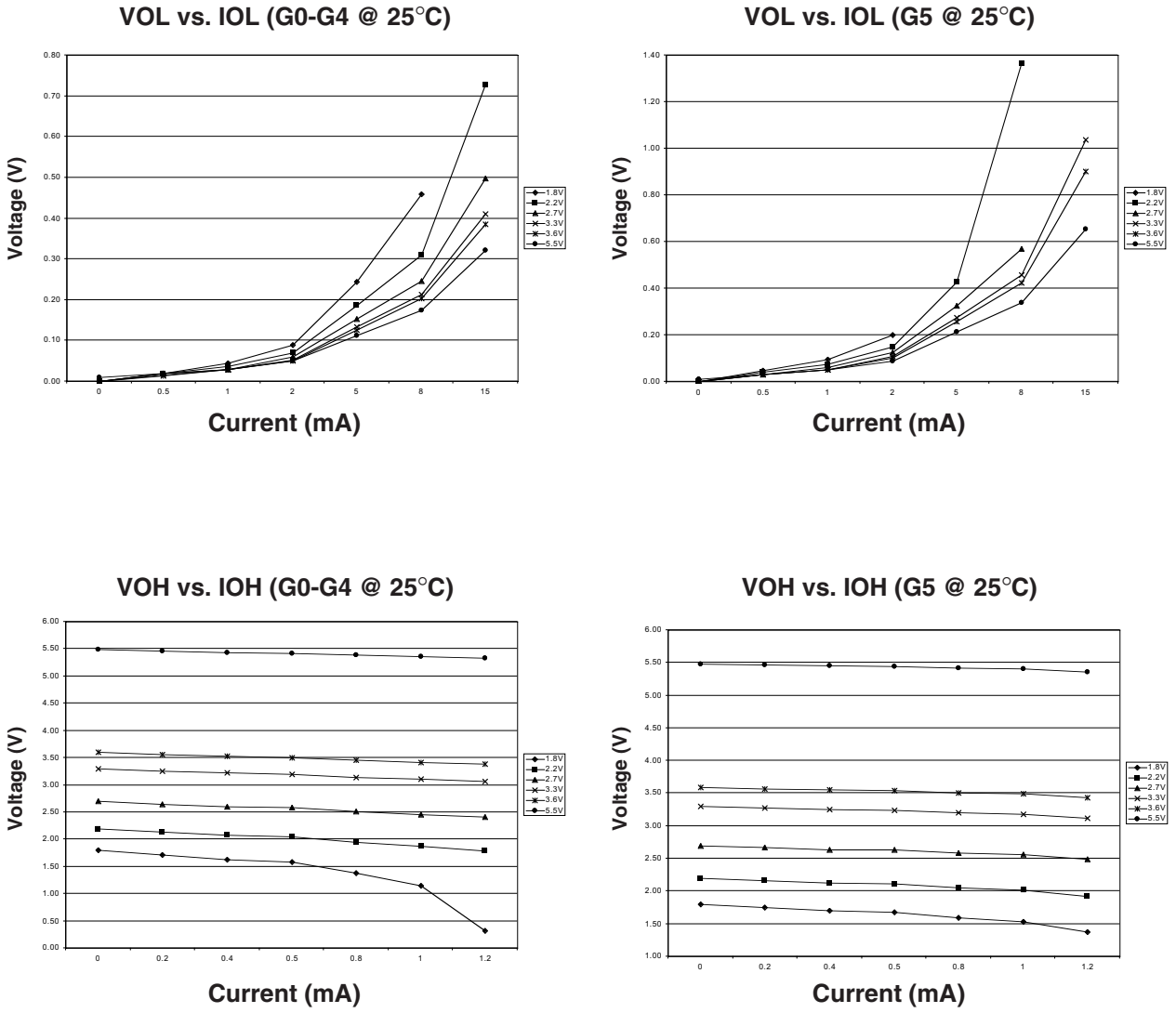


Figure 10: VOL/VOH



4.1.1 Accumulator (A)

The Accumulator is a general-purpose 8-bit register that is used to hold data and results of arithmetic calculations or data manipulations.

4.1.2 X-Pointer (X)

The X-Pointer register allows for an 11-bit indexing value to be added to an 8-bit offset creating an effective address used for reading and writing between the entire memory space. (Software can only read from code EEPROM.) This provides software with the flexibility of storing lookup tables in the code EEPROM memory space for the core's accessibility during normal operation.

The X register is divided into two sections. The 10 least significant bits (LSB) of the register is the address of the program or data memory space. The most significant bit (MSB) of the register is write only and selects between the data (0x000 to 0x0FF) or program (0xC00 to 0xFFF) memory space.

Example: If Bit 10 = 0, then the LD A, [00,X] instruction will take a value from address range 0x000 to 0x0FF and load it into A. If Bit 10 = 1, then the LD A, [00,X] instruction will take a value from address range 0xC00 to 0xFFF and load it into A.

4.1.3 Program Counter (PC)

The 10-bit program counter register contains the address of the next instruction to be executed. After a reset, if in normal mode the program counter is initialized to 0xC00.

4.1.4 Stack Pointer (SP)

The ACEx microcontroller has an automatic program stack with a 4-bit stack pointer. The stack can be initialized to any location between addresses 0x30-0x3F. After a reset, the stack pointer is defaulted to 0xF pointing to address 0x3F. Normally, the stack pointer is initialized by one of the first instructions in an application program.

The stack is configured as a data structure which decrements from high to low memory. Each time a new address is pushed onto the stack, the core decrements the stack pointer by two. Each time an address is pulled from the stack, the core increments the stack pointer by two. At any given time, the stack pointer points to the next free location in the stack.

When a subroutine is called by a jump to subroutine (JSR) instruction, the address of the instruction is automatically pushed onto the stack least significant byte first. When the subroutine is finished, a return from subroutine (RET) instruction is executed. The RET instruction pulls the previously stacked return address from the stack and loads it into the program counter. Execution then continues at the recovered return address.

4.1.5 Status Register (SR)

This 8-bit register contains four condition code indicators (C, H, Z, and N), an interrupt masking bit (G), and an EEPROM write flag (R). The condition code indicators are automatically updated by most instructions. (See Table 10)

Carry/Borrow (C)

The carry flag is set if the arithmetic logic unit (ALU) performs a carry or borrow during an arithmetic operation and by its dedicated instructions. The rotate instruction operates with and through the carry bit to facilitate multiple-word shift operations. The LDC and INVC instructions facilitate direct bit manipulation using the carry flag.

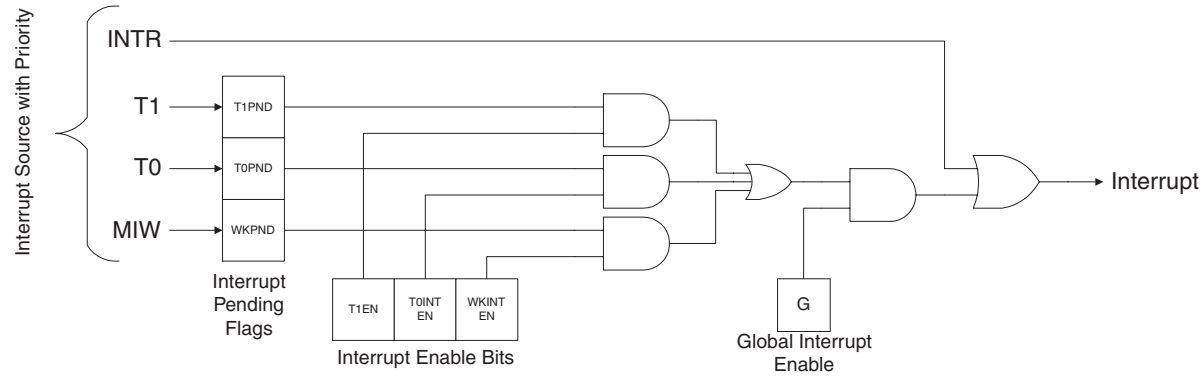
Half Carry (H)

The half carry flag indicates whether an overflow has taken place on the boundary between the two nibbles in the accumulator. It is primarily used for Binary Coded Decimal (BCD) arithmetic calculation.

Zero (Z)

The zero flag is set if the result of an arithmetic, logic, or data manipulation operation is zero. Otherwise, it is cleared.

Figure 12: Basic Interrupt Structure



Negative (N)

The negative flag is set if the MSB of the result from an arithmetic, logic, or data manipulation operation is set to one. Otherwise, the flag is cleared. A result is said to be negative if its MSB is a one.

Interrupt Mask (G)

The interrupt request mask (G) is a global mask that disables all maskable interrupt sources. If the G Bit is cleared, interrupts can become pending, but the operation of the core continues uninterrupted. However, if the G Bit is set an interrupt is recognized. After any reset, the G bit is cleared by default and can only be set by a software instruction. When an interrupt is recognized, the G bit is cleared after the PC is stacked and the interrupt vector is fetched. Once the interrupt is serviced, a return from interrupt instruction is normally executed to restore the PC to the value that was present before the interrupt occurred. The G bit is the reset to one after a return from interrupt is executed. Although the G bit can be set within an interrupt service routine, "nesting" interrupts in this way should only be done when there is a clear understanding of latency and of the arbitration mechanism.

4.2 Interrupt handling

When an interrupt is recognized, the current instruction completes its execution. The return address (the current value in the program counter) is pushed onto the stack and execution continues at the address specified by the unique interrupt vector (see Table 11). This process takes five instruction cycles. At the end of the interrupt service routine, a return from interrupt (RETI) instruction is executed. The RETI instruction causes the saved address to be pulled off the stack in reverse order. The G bit is set and instruction execution resumes at the return address.

The ACEx microcontroller is capable of supporting four interrupts. Three are maskable through the G bit of the SR and the fourth (software interrupt) is not inhibited by the G bit (see Figure 12). The software interrupt is generated by the execution of the INTR instruction. Once the INTR instruction is executed, the ACEx core will interrupt whether the G bit is set or not. The INTR interrupt is executed in the same manner as the other maskable interrupts where the program counter register is stacked and the G bit is cleared. This means, if the G bit was enabled prior to the software interrupt the RETI instruction must be used to return from interrupt in order to restore the G bit to its previous state. However, if the G bit was not enabled prior to the software interrupt the RET instruction must be used.

In case of multiple interrupts occurring at the same time, the ACEx microcontroller core has prioritized the interrupts. The interrupt priority sequence in shown in Table 8.

4.3 Addressing Modes

The ACEx microcontroller has six addressing modes indexed, direct, immediate, absolute jump, and relative jump.

Indexed

The instruction allows an 8-bit unsigned offset value to be added to the 10-LSBs of the X-pointer yielding a new effective address. This mode can be used to address any memory space (program or data).

Direct

The instruction contains an 8-bit address field that directly points to the data memory space as an operand.

Immediate

The instruction contains an 8-bit immediate field as an operand.

Inherent

This instruction has no operands associated with it.

Absolute

The instruction contains a 10-bit address that directly points to a location in the program memory space. There are two operands associated with this addressing mode. Each operand contains a byte of an address. This mode is used only for the long jump (JMP) and JSR instructions.

Relative

This mode is used for the short jump (JP) instructions where the operand is a value relative to the current PC address. With this instruction, software is limited to the number of bytes it can jump, -31 or +32.

Table 8: Interrupt Priority Sequence

Priority (4 highest, 1 lowest)	Interrupt
4	MIW (EDGEI)
3	Timer0 (TMRI0)
2	Timer1 (TMRI1)
1	Software (INTR)

Table 9: Instruction Addressing Modes

Instruction	Immediate			Direct	Indexed	Inherent		Relative	Absolute
ADC	A, #			A, M					
AND	A, #			A, M					
SUBC	A, #			A, M					
XOR	A, #			A, M					
CLR				M		A			
INC				M		A	X		
DEC				M		A	X		
IFEQ	A, #	M,#		A, M					
IFGT	A, #			A, M					
IFNE	A, #			A, M					
SC						no-op			
RC						no-op			
IFC						no-op			
IFNC						no-op			
INVC						no-op			
LDC				#, M					
STC				#, M					
RLC						A			
RRC						A			
LD	A, #	M, #	X, #	A, M	A, [00,X]				
ST				A, M	A, [00,X]				
LD				M, M					
NOP						no-op			
IFBIT				#, M					
SBIT				#, M					
RBIT				#, M					
JP								Rel	
JSR									M
JMP									M
RET						no-op			
RETI						no-op			
INTR						no-op			

Table 10: Instruction Cycles and Bytes

Mnemonic	Operand	Bytes	Cycles	Flags affected
ADC	A, #	2	2	C,H,Z,N
ADC	A, M	2	2	C,H,Z,N
AND	A, #	2	2	Z,N
AND	A, M	2	2	Z,N
CLR	A	1	1	Z,N,C,H
CLR	M	2	1	Z,N,C,H
DEC	A	1	1	Z,N
DEC	M	2	2	Z,N
DEC	X	1	1	Z
IFBIT	#, M	2	2	None
IFC		1	1	None
IFEQ	A, #	2	2	None
IFEQ	A, M	2	2	None
IFEQ	M, #	3	3	None
IFGT	A, #	2	2	None
IFGT	A, M	2	2	None
IFNE	A, #	2	2	None
IFNE	A, M	2	2	None
IFNC		1	1	None
INC	A	1	1	Z,N
INC	M	2	2	Z,N
INC	X	1	1	Z
INTR		1	5	None
INVC		1	1	C
JMP	M	3	4	None

Mnemonic	Operand	Bytes	Cycles	Flags affected
JP		1	1	None
JSR	M	3	5	None
LD	A, #	2	2	None
LD	A, [00,X]	2	3	None
LD	A, M	2	2	None
LD	M, #	3	3	None
LD	M, M	3	3	None
LD	X, #	3	3	None
LDC	#, M	2	2	C
NOP		1	1	None
RBIT	#, M	2	2	Z,N
RC		1	1	C,H
RET		1	5	None
RETI		1	5	None
RLC	A	1	1	C,Z,N
RRC	A	1	1	C,Z,N
SBIT	#, M	2	2	Z,N
SC		1	1	C,H
ST	A, [00,X]	2	3	None
ST	A, M	2	2	None
STC	#, M	2	2	Z,N
SUBC	A, #	2	2	C,H,Z,N
SUBC	A, M	2	2	C,H,Z,N
XOR	A, #	2	2	Z,N
XOR	A, M	2	2	Z,N

4.4 Memory Map

All I/O ports, peripheral registers and core registers (except the accumulator and the program counter) are mapped into memory space.

Table 11: Memory Map

Address	Memory Space	Block	Contents
0x00 - 0x3F	Data	SRAM	Data RAM
0x40 - 0x7F	Data	EEPROM	Data EEPROM
0xAA	Data	Timer1	T1RA register
0xAB, 0xAD			Reserved
0xAC	Data	Timer1	TMR1 register
0xAE	Data	Timer1	T1CNTRL register
0xAF	Data	MIW	WKEDG register
0xB0	Data	MIW	WKPND register
0xB1	Data	MIW	WKEN register
0xB2	Data	I/O	PORTGD register
0xB3	Data	I/O	PORTGC register
0xB4	Data	I/O	PORTGP register
0xB5	Data	Timer0	WDSVR register
0xB6	Data	Timer0	T0CNTRL register
0xB7	Data	Clock	HALT mode register
0xB8 - 0xBA			Reserved
0xBB	Data	Init. Reg.	Initialization register 1
0xBC	Data	Init. Reg.	Initialization register 2
0xBD	Data	LBD	LBD register
0xBE	Data	Core	XHI register
0xBF	Data	Core	XLO register
0xC0	Data	Clock	Power mode clear (PMC) register
0xCE	Data	Core	SP register
0xCF	Data	Core	Status register (SR)
0xC00 - 0xFF5	Program	EEPROM	Code EEPROM
0xFF6 - 0xFF7	Program	Core	Timer0 Interrupt vector
0xFF8 - 0xFF9	Program	Core	Timer1 Interrupt vector
0xFFA - 0xFFB	Program	Core	MIW Interrupt vector
0xFFC - 0xFFD	Program	Core	Soft Interrupt vector
0xFFE - 0xFFF			Reserved

5.0 Timer 1

Timer 1 is a versatile 8-bit timer. Its main function is to operate as a Pulse Width Modulation (PWM) generator that generates pulses of a specified width and duty cycles.

Timer 1 contains an 8-bit timer register (TMR1), an 8-bit auto-reload register (T1RA), and an 8-bit control register (T1CNTRL). All registers are memory-mapped for simple access through the core. For the PWM signal generation the timer contains an output (T1) that is multiplexed with the I/O pin G2.

The timer can be started or stopped through the T1CNTRL register bit T1C0. When running, the timer counts down (decrements) every clock cycle. The timer's clock has a pre-scalar and is selectable through two T1CNTRL register bits T1PSC[1:0]. Depending on the selected operating mode, occurrences of timer underflow (transitions from 0x00 to 0xFF or reload) can either generate an interrupt and/or toggle the T1 output pin.

Timer 1's interrupt (TMRI1) can be enabled by the interrupt enable (T1EN) bit in the T1CNTRL register. When the timer interrupt is enabled, the source of the interrupt is a timer underflow. By default, the timer register is reset to 0xFF and the auto-reload register is reset to 0x00.

5.1 Timer control bits

Reading and writing to the T1CNTRL register controls the timer's operation. By writing to the control bits, the user can enable or disable the timer interrupts, set the mode of operation, start or stop the timer, and select the clock. The T1CNTRL register bits are described in Table 12.

Table 12: TIMER1 Control Register Bits

T1CNTRL Register	Name	Function
Bit 7	----------	Reserved
Bit 6	----------	Reserved
Bit 5	T1C1	T1 toggle enable bit: 1 = T1 toggle enabled, 0 = T1 toggle disabled
Bit 4	T1C0	TMR1 run: 1 = Start timer, 0 = Stop timer
Bit 3	T1PND	Timer1 interrupt pending flag: 1 = Timer1 interrupt pending, 0 = Timer1 interrupt not pending
Bit 2	T1EN	Timer1 interrupt enable bit: 1 = Timer1 interrupt enabled, 0 = Timer1 interrupt disabled
Bit 1,0	T1PSC	Pre-scalar selection bits: Selects the 1MHz clock divider to be by 1 (00b), 2 (01b), 4 (10b), or 8 (11b)

9.0 I/O Port

The six I/O pins are bi-directional with the exception of G3 which is always an input with weak pull-up (see Figure 19). The bi-directional I/O pins can be individually configured by software to operate as high-impedance inputs, as inputs with weak pull-up, or as push-pull outputs. The operating state is determined by the contents of the corresponding bits in the data and configuration registers. Each bi-directional I/O pin can be used for general purpose I/O, or in some cases, for a specific alternate function determined by the on-chip hardware.

9.1 I/O registers

The I/O pins (G0-G5) have three memory-mapped port registers associated with the I/O circuitry: a port configuration register (PORTGC), a port data register (PORTGD), and a port input register (PORTGP). PORTGC is used to configure the pins as inputs or outputs. A pin may be configured as an input by writing a 0 or as an output by writing a 1 to its corresponding PORTGC bit. If a pin is configured as an output, its PORTGD bit represents the state of the pin (1 = logic high, 0 = logic low). If the pin is configured as an input, its PORTGD bit selects whether the pin is a weak pull-up or a high-impedence input. Table 13 provides details of the port configuration options. The port configuration and data registers are both read/writable. Reading PORTGP returns the value of the port pins regardless of how the pins are configured. Since this device supports multi-input wakeup/interrupt, the PORTG inputs have Schmitt triggers.

Figure 19: PORTGD Logic Diagram

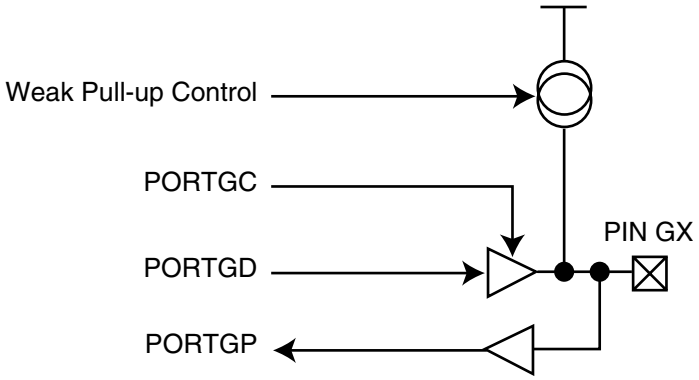


Figure 20: I/O Register bit assignments

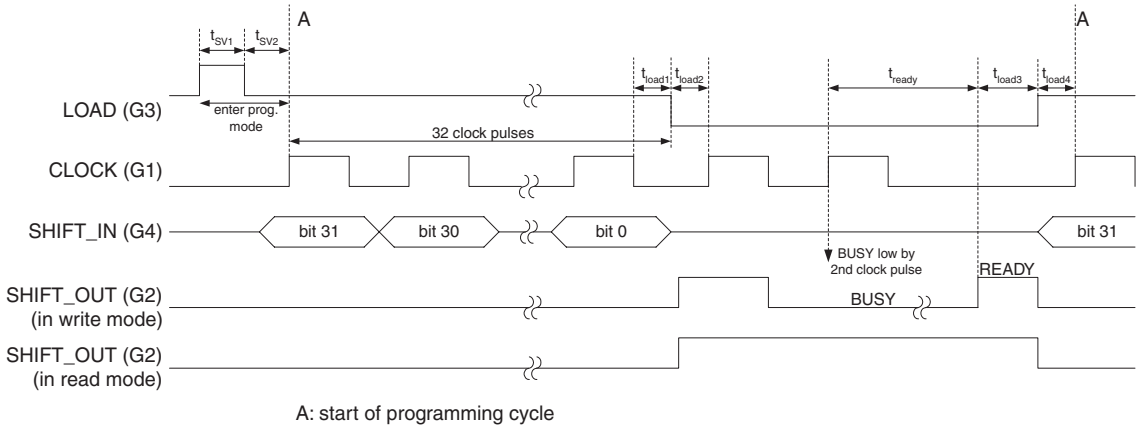
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
x	x	G5	G4	G3[9]	G2	G1	G0

Table 13: I/O configuration options

Configuration Bit	Data Bit	Port Pin Configuration
0	0	High-impedence input (TRI-STATE input)
0	1	Input with pull-up (weak one input)
1	0	Push-pull zero output
1	1	Push-pull one output

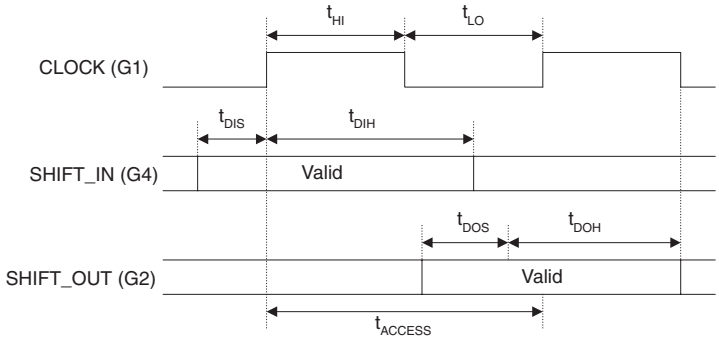
[9] G3 is only an input.

Figure 21: Programming Protocol[10]



A: start of programming cycle

Figure 22: Serial Data Timing



11.0 Brown-out/Low Battery Detect Circuit

The Brown-out Reset (BOR) and Low Battery Detect (LBD) circuits on the ACEx microcontroller have been designed to offer two types of voltage reference comparators. The sections below will describe the functionality of both circuits.

11.1 Brown Out Reset

The Brown-out Reset (BOR) function is used to hold the device in reset when V_{CC} drops below a fixed threshold. While in reset, the device is held in its initial condition until V_{CC} rises above the threshold value. Shortly after V_{CC} rises above the threshold value, an internal reset sequence is started. After the reset sequence, the core fetches the first instruction and starts normal operation.

On the devices, the BOR should be used in situations when V_{CC} rises and falls slowly and in situations when V_{CC} does not fall to zero before rising back to operating range. The BOR can be thought of as a supplement function to the Power-on Reset when V_{CC} does not fall below ~1.5V. The Power-on Reset circuit works best when V_{CC} starts from 0V and rises sharply. So in applications where V_{CC} is not constant, the BOR will give added device stability.

The BOR circuit must be enabled through the BOR enable bit (BOREN) in the initialization register. The BOREN bit can only be set while the device is in programming mode. Once set, the BOR will always be powered-up enabled. Software cannot disable the BOR. The BOR can only be disabled in programming mode by resetting the BOREN bit as long as the global write protect (WDIS) feature is not enabled.

11.2 Low Battery Detect

The Low Battery Detect (LBD) circuit allows software to monitor the V_{CC} level at the lower voltage ranges. LBD has eight software programmable voltage reference threshold levels ranging from 2.2V to 3.3V that can be changed on the fly. Once Vcc falls below the selected threshold, the LBD flag in the LBD control register is set. The LBD flag will hold its value until V_{CC} rises above the threshold. (See Figure 23)

The LBD bit is read only. If LBD is 0, it indicates that the V_{CC} level is higher than the selected threshold. If LBD is 1, it indicates that the V_{CC} level is below the selected threshold. The threshold level can be adjusted up to eight levels using the three trim bits (Bat_trim[2:0]) of the LBD control register. The LBD flag does not cause any hardware actions or an interruption of the processor. It is for software monitoring only.

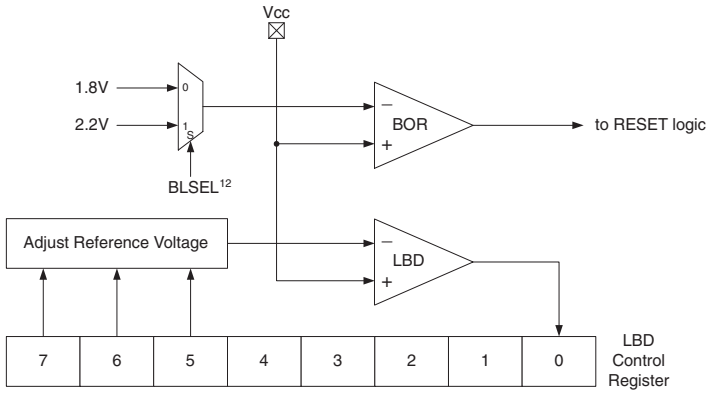
The LBD function is disabled during HALT/IDLE mode. After exiting HALT/IDLE, software must wait at lease 10µs before reading the LBD bit to ensure that the internal circuit has stabilized.

Figure 23: LBD Control Register Definition

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bat_trim[2:0]			0	X	X	X	LBD

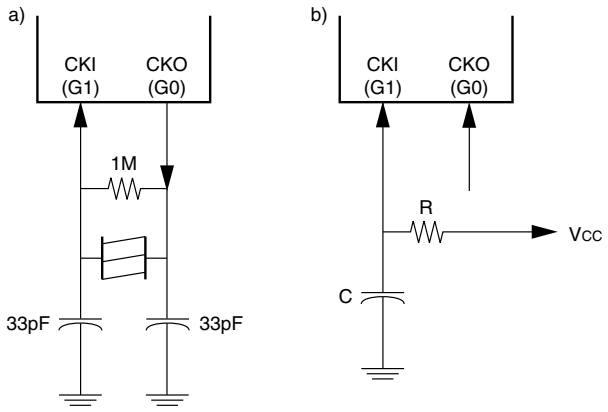
Bat_trim[2]	Bat_trim[1]	Bat_trim[0]	Voltage Threshold
0	0	0	3.3
0	0	1	3.1
0	1	0	2.9
0	1	1	2.7
1	0	0	2.5
1	0	1	2.4
1	1	0	2.3
1	1	1	2.2

Figure 24: BOR/LBD Block Diagram



[12] See Figure 13 for information on BLSEL.

Figure 26: Crystal 9 (a) and RC (b) Oscillator Diagrams



15.0 HALT Mode

The HALT mode is a power saving feature that almost completely shuts down the device for current conservation. The device is placed into HALT mode by setting the HALT enable bit (EHALT) of the HALT register through software using only the "LD M, #" instruction. EHALT is a write only bit and is automatically cleared upon exiting HALT. When entering HALT, the internal oscillator and all the on-chip systems including the LBD and the BOR circuits are shut down.

The device can exit HALT mode only by the MIW circuit. Therefore, prior to entering HALT mode, software must configure the MIW circuit accordingly. (See Section 8.0) After a wakeup from HALT, a 64 clock cycle start-up delay is initiated to allow the internal oscillator to stabilize before normal execution resumes. Immediately after exiting HALT, software must clear the Power Mode Clear (PMC) register by only using the "LD M, #" instruction. (See Figure 28)

16.0 IDLE Mode

In addition to the HALT mode power saving feature, the device also supports an IDLE mode operation. The device is placed into IDLE mode by setting the IDLE enable bit (EIDLE) of the HALT register through software using only the "LD M, #" instruction. EIDLE is a write only bit and is automatically cleared upon exiting IDLE. The IDLE mode operation is similar to HALT except the internal oscillator, the Watchdog, and the Timer 0 remain active while the other on-chip systems including the LBD and the BOR circuits are shut down.

The device can exit IDLE by a Timer 0 overflow every 8192 cycles or/and by the MIW circuit. If exiting IDLE mode with the MIW, prior to entering, software must configure the MIW circuit accordingly. (See Section 8.0) Once a wake from IDLE mode is triggered, the core will begin normal operation by the next clock cycle. Immediately after exiting IDLE mode, software must clear the Power Mode Clear (PMC) register by using only the "LD M, #" instruction. (See Figure 29)

Figure 27: HALT Register Definition

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
x	x	x	x	x	x	EIDLE	EHALT

Figure 28: Recommended HALT Flow

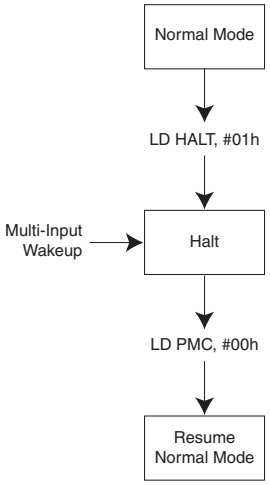
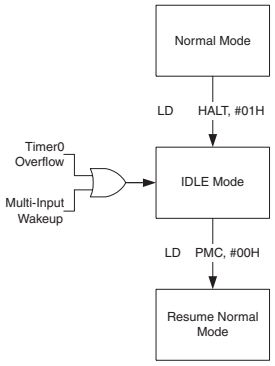


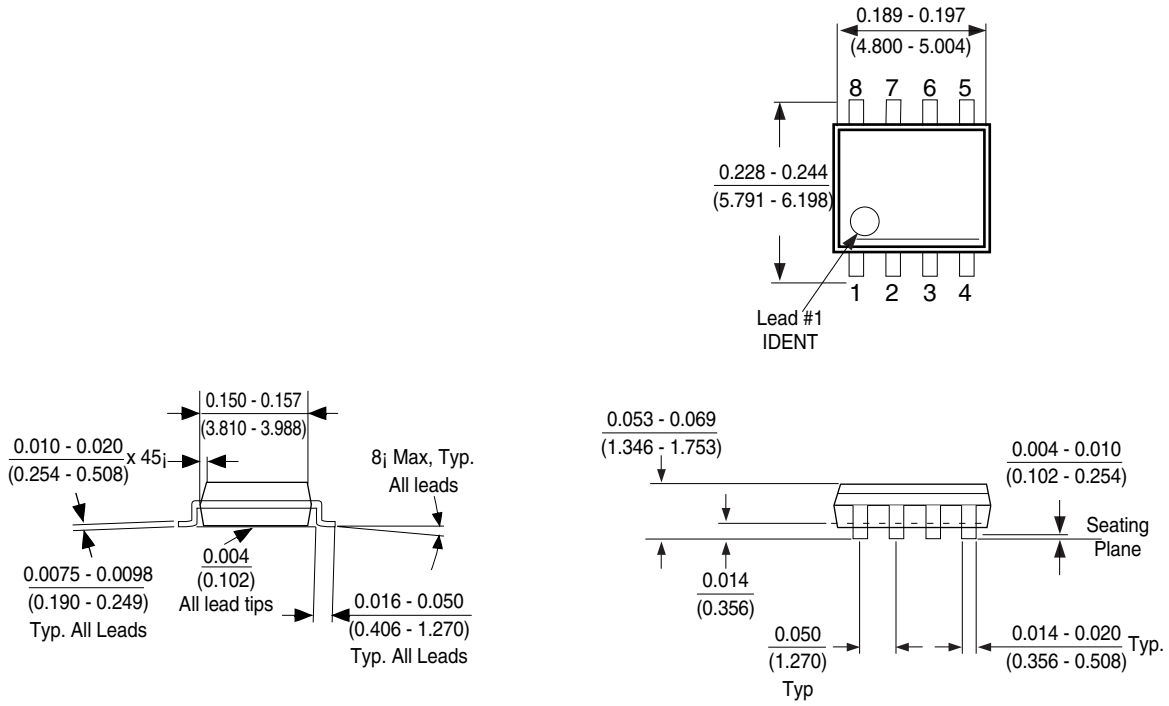
Figure 29: Recommended IDLE Flow



Ordering Information

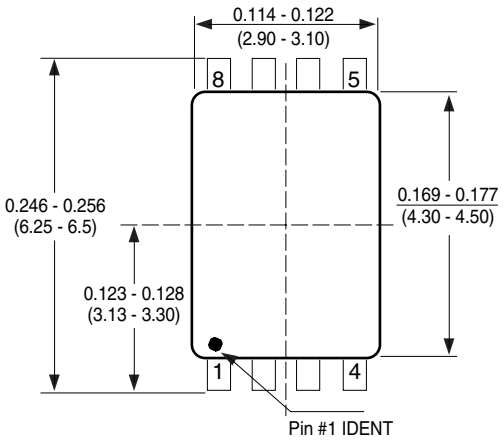
Part Number	Core Type			Max. # I/Os	Program Memory Size		Operating Voltage Range		Temperature Range			Package		Tape and Reel
	0	1	2	8	1K	2K	1.8 – 5.5V	2.2 –- 5.5V	0 to 70°C	-40 to +85C	-40 to +125°C	8-pin SOIC	8-pin TSSOP	
ACE1001M8		X		X	X			X	X			X		
ACE1001M8X		X		X	X			X	X			X		X
ACE1001MT8		X		X	X			X	X				X	
ACE1001MT8X		X		X	X			X	X				X	X
ACE1001EM8		X		X	X			X		X		X		
ACE1001EM8X		X		X	X			X		X		X		X
ACE1001EMT8		X		X	X			X		X			X	
ACE1001EMT8X		X		X	X			X		X			X	X
ACE1001LM8		X		X	X		X		X			X		
ACE1001LM8X		X		X	X		X		X			X		X
ACE1001LMT8		X		X	X		X		X				X	
ACE1001LMT8X		X		X	X		X		X				X	X

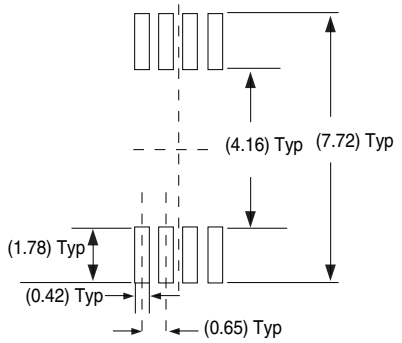
Physical Dimensions inches (millimeters) unless otherwise noted



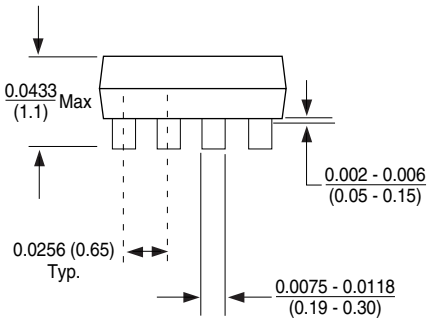
Molded Small Out-Line Package (M8)
Order Number ACE1001M8/ACE1001EM8/ACE1001LM8
Package Number M08A

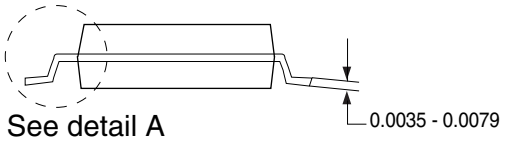
Physical Dimensions inches (millimeters) unless otherwise noted



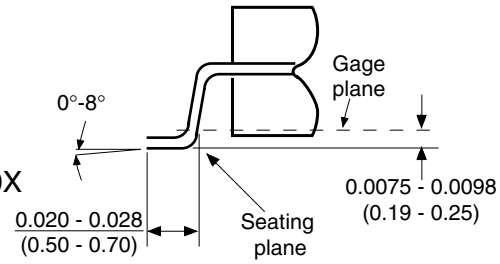


Land pattern recommendation





DETAIL A
Typ. Scale: 40X



Notes: Unless otherwise specified

1. Reference JEDEC registration MO153. Variation AA. Dated 7/93

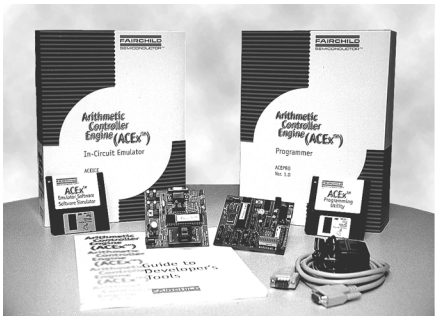
8-Pin Molded TSSOP (MT8)
Order Number ACE1001MT8/ACE1001EMT8/ACE1001LMT8
Package Number MTC08

ACEx Development Tools

General Information

Fairchild Semiconductor offers different possibilities to evaluate and emulate software written for ACEx.

Simulator: Is a Windows program able to load, assemble, and debug ACEx programs. It is possible to place as many breakpoints as needed, trace the program execution in symbolic format, and program a device with the proper options. The ACEx Simulator is available free-of-charge and can be downloaded from Fairchild's web site at www.fairchildsemi.com/products/micro



ACEx Emulator Kit: Fairchild also offers a low cost real-time in-circuit emulator kit that includes:

- Emulator board
- Emulator software
- Assembler and Manuals
- Power supply
- DIP14 target cable
- PC cable

The ACEx emulator allows for debugging the program code in a symbolic format. It is possible to place one breakpoint and watch various data locations. It also has built-in programming capability.

Prototype Board Kits: Fairchild offer two solutions for the simplification of the breadboard operation so that ACEx Applications can be quickly tested.

1) ACEDEMO is can be used for general purpose applications
2) ACETXRX for transmitting / receiving (RF, IR, RS232, RS485) applications.

ACEDEMO has 8 switches, 8 LEDs, RS232 voltage translator, buzzer, and a lamp with a small breadboard area.

Ordering P/Ns

Programming Adapters:

DIP8 - ACEADAPTN
DIP14 - ACEADAPTN14
TSSOP8 - ACEADAPTMT8
SO8 - ACEADAPTM8
SO14 - ACEADAPTM

Emulator Kit:

ACEICE (110Vac)
ACEICEEU (220Vac)

Prototype Boards:

ACEDEMO
ACETXRX (315MHz)
ACETXRXEU (433MHz)

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Fairchild's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of Fairchild Semiconductor Corporation. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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