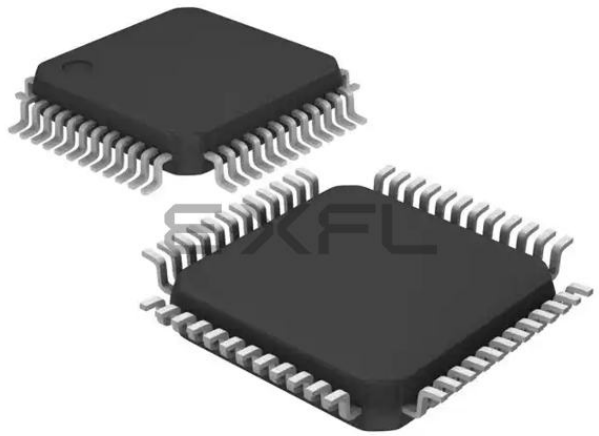

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	37
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f102c4t6a

List of tables

1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of STM32F102x4 and STM32F102x6 low-density USB access line microcontrollers. For more details on the whole STMicroelectronics STM32F102xx family. please refer to *Section 2.2: Full compatibility throughout the family*.

The medium-density STM32F102xx datasheet should be read in conjunction with the low-, medium- and high-density STM32F10xxx reference manual.

For information on programming, erasing and protection of the internal Flash memory please refer to the *STM32F10xxx Flash programming manual.*

The reference and Flash programming manuals are both available from the STMicroelectronics website *www.st.com*.

For information on the Cortex®-M3 core please refer to the Cortex®-M3 Technical Reference Manual, available from the ARM® website.

2 Description

The STM32F102xx medium-density USB access line incorporates the high-performance ARM® Cortex®-M3 32-bit RISC core operating at a 48 MHz frequency, high-speed embedded memories (Flash memory of 16 or 32 Kbytes and SRAM of 4 or 6 Kbytes), and an extensive range of enhanced peripherals and I/Os connected to two APB buses. All devices offer standard communication interfaces (one I^2C, one SPI, one USB and two USARTs), one 12-bit ADC and two general-purpose 16-bit timers.

The STM32F102xx family operates in the –40 to +85 °C temperature range, from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power applications.

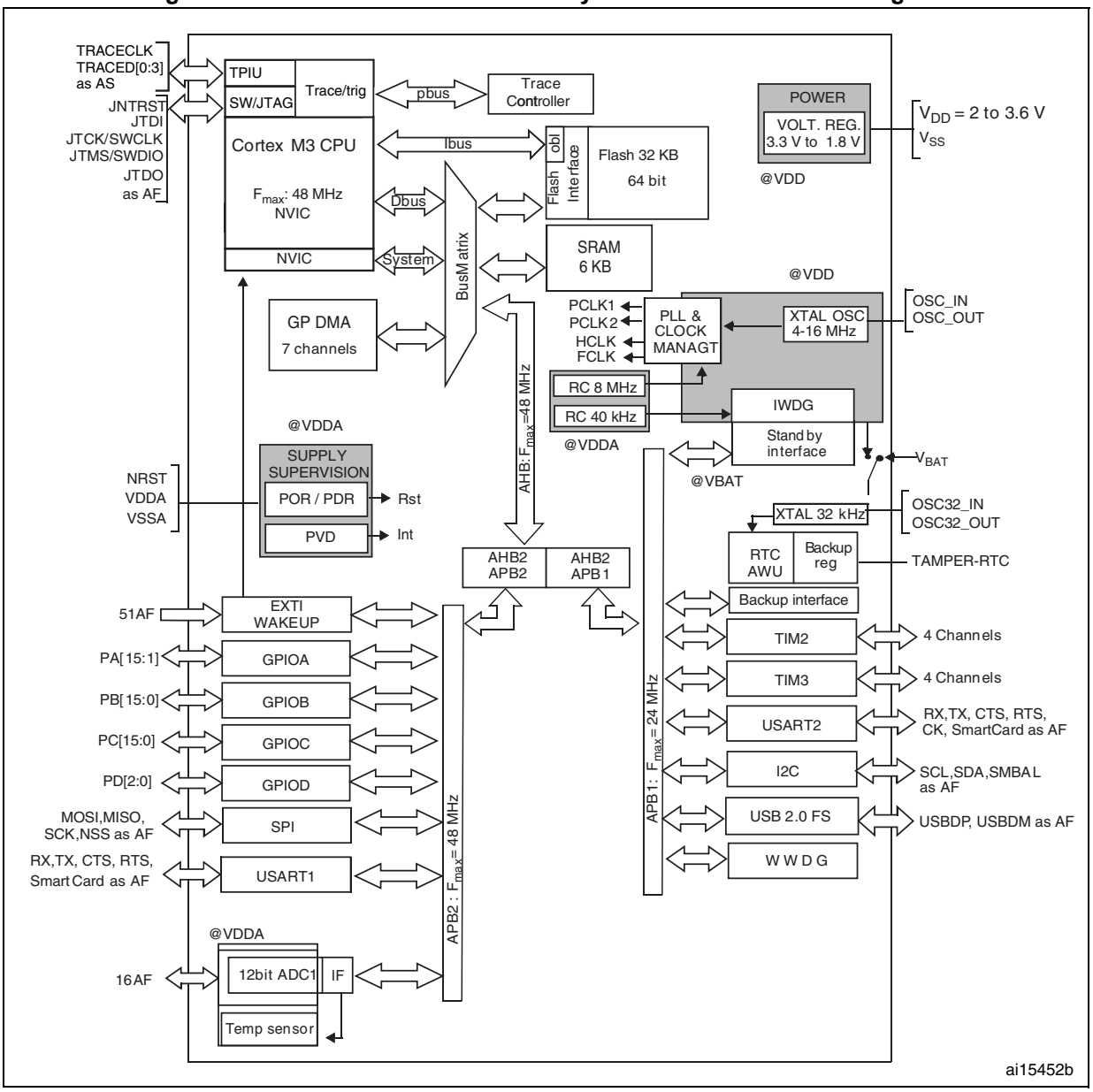
The STM32F102xx medium-density USB access line is delivered in the LQFP48 7 × 7 mm and LQFP64 10 × 10 mm packages.

The STM32F102xx medium-density USB access line microcontrollers are suitable for a wide range of applications.

- Application control and user interface
- Medical and handheld equipment
- PC peripherals, gaming and GPS platforms
- Industrial applications: PLC, inverters, printers, and scanners
- Alarm systems, Video intercom, and HVAC

Figure 1 shows the general block diagram of the device family.

Figure 1. STM32F102T8 medium-density USB access line block diagram



1. AF = alternate function on I/O port pin.
2. T_A = –40 °C to +85 °C (junction temperature up to 105 °C).

CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity, In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

Embedded SRAM

4 or 6 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states.

Nested vectored interrupt controller (NVIC)

The STM32F102xx medium-density USB access line embeds a nested vectored interrupt controller able to handle up to 36 maskable interrupt channels (not including the 16 interrupt lines of Cortex®-M3) and 16 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of *late arriving* higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 19 edge detectors lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect external line with pulse width lower than the Internal APB2 clock period. Up to 51 GPIOs are connected to the 16 external interrupt lines.

Clocks and startup

System clock selection is performed on startup. however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-16 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example on failure of an indirectly used external crystal, resonator or oscillator).

Several prescalers allow the configuration of the AHB frequency, the High Speed APB (APB2) and the low Speed APB (APB1) domains. The maximum frequency of the AHB and the APB domains is 48 MHz. See *Figure 2* for details on the clock tree.

Low-power modes

The STM32F102xx medium-density USB access line supports three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep** mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop** mode

  The Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low power mode.
  The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output or the RTC alarm.

- **Standby** mode

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and registers content are lost except for registers in the Backup domain and Standby circuitry.

  The device exits Standby mode when an external reset (NRST pin), a IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

DMA

The flexible 7-channel general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I^2C, USART, general purpose timers TIMx and ADC.

RTC (real-time clock) and backup registers

The RTC and the backup registers are supplied through a switch that takes power either on V_{DD} supply when present or through the V_{BAT} pin. The backup registers are ten 16-bit registers used to store 20 bytes of user application data when V_{DD} power is not present.

The real-time clock provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and a periodic interrupt. It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low power RC oscillator or the high-speed external clock divided by 128. The internal low power RC has a typical frequency of 40 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural crystal deviation. The RTC features a 32-bit programmable counter for long term measurement using the Compare

register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock. it can operate in Stop and Standby modes. It can be used as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

SysTick timer

This timer is dedicated for OS, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

General-purpose timers (TIMx)

There are 2 synchronizable general-purpose timers embedded in the STM32F102xx medium-density USB access line devices. These timers are based on a 16-bit auto-reload up/down counter, a 16-bit prescaler and feature 4 independent channels each for input capture, output compare, PWM or one-pulse mode output. This gives up to 12 input captures / output compares / PWMs on the LQFP48 and LQFP64 packages.
The general-purpose timers can work together via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode.

Any of the general-purpose timers can be used to generate PWM outputs. They both have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

I²C bus

One I²C bus interface can operate in multi-master and slave modes. It can support standard and fast modes. It supports dual slave addressing (7-bit only) and both 7/10-bit addressing in master mode. A hardware CRC generation/verification is embedded.

The I^2C interface can be served by DMA and they support SM Bus 2.0/PM Bus.

5.3 Operating conditions

5.3.1 General operating conditions

Table 8. General operating conditions

Symbol	Parameter	Conditions		Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-		0	48	MHz
f_{PCLK1}	Internal APB1 clock frequency	-		0	24	
f_{PCLK2}	Internal APB2 clock frequency	-		0	48	
V_{DD}	Standard operating voltage	-		2	3.6	V
V_{DDA}(1)	Analog operating voltage (ADC not used)	Must be the same potential as V_{DD}(2)		2	3.6	V
	Analog operating voltage (ADC used)			2.4	3.6	
V_{IN}	I/O input voltage	Standard IO		–0.3	V_{DD}+ 0.3	
		FTIO(3)	2 V < V_{DD} ≤ 3.6 V	–0.3	5.5	
			V_{DD} = 2 V	–0.3	5.2	
		BOOT0		0	5.5	
P_D	Power dissipation at T_A = 85 °C(4)	LQFP48		-	363	mW
		LQFP64		-	444	
T_A	Ambient temperature	Maximum power dissipation		–40	85	°C
		Low power dissipation(5)		–40	105	°C
T_J	Junction temperature range	-		–40	105	°C

1. When the ADC is used, refer to *Table 45: ADC characteristics*.
2. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and operation.
3. To sustain a voltage higher than V_{DD}+0.3 V, the internal pull-up/pull-down resistors must be disabled.
4. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed $T_J$max (see *Section 6.3: Thermal characteristics*).
5. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed $T_J$max (see *Section 6.3: Thermal characteristics*).

5.3.2 Operating conditions at power-up / power-down

Subject to general operating conditions for T_A.

Table 9. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	∞	µs/V
	V_{DD} fall time rate		20	∞	

5.3.3 Embedded reset and power control block characteristics

The parameters given in *Table 10* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

Table 10. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection	PLS[2:0]=000 (rising edge)	2.1	2.18	2.26	V
		PLS[2:0]=000 (falling edge)	2.0	2.08	2.16	V
		PLS[2:0]=001 (rising edge)	2.19	2.28	2.37	V
		PLS[2:0]=001 (falling edge)	2.09	2.18	2.27	V
		PLS[2:0]=010 (rising edge)	2.28	2.38	2.48	V
		PLS[2:0]=010 (falling edge)	2.18	2.28	2.38	V
		PLS[2:0]=011 (rising edge)	2.38	2.48	2.58	V
		PLS[2:0]=011 (falling edge)	2.28	2.38	2.48	V
		PLS[2:0]=100 (rising edge)	2.47	2.58	2.69	V
		PLS[2:0]=100 (falling edge)	2.37	2.48	2.59	V
		PLS[2:0]=101 (rising edge)	2.57	2.68	2.79	V
		PLS[2:0]=101 (falling edge)	2.47	2.58	2.69	V
		PLS[2:0]=110 (rising edge)	2.66	2.78	2.9	V
		PLS[2:0]=110 (falling edge)	2.56	2.68	2.8	V
		PLS[2:0]=111 (rising edge)	2.76	2.88	3	V
		PLS[2:0]=111 (falling edge)	2.66	2.78	2.9	V
$V_{PVDhyst}$(2)	PVD hysteresis	-	-	100	-	mV
$V_{POR/PDR}$	Power on/power down reset threshold	Falling edge	1.8(1)	1.88	1.96	V
		Rising edge	1.84	1.92	2.0	V
$V_{PDRhyst}$	PDR hysteresis	-	-	40	-	mV
$t_{RSTTEMPO}$(2)	Reset temporization	-	1.5	2.5	4.5	ms

1. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.
2. Guaranteed by design, not tested in production.

5.3.4 Embedded reference voltage

The parameters given in *Table 11* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

2. To have the Standby consumption with RTC ON, add I_{DD_VBAT} (Low-speed oscillator and RTC ON) to I_{DD} Standby (when V_{DD} is present the Backup Domain is powered by V_{DD} supply).
3. Based on characterization, not tested in production.

Figure 12. Typical current consumption on V_{BAT} with RTC on versus temperature at different V_{BAT} values

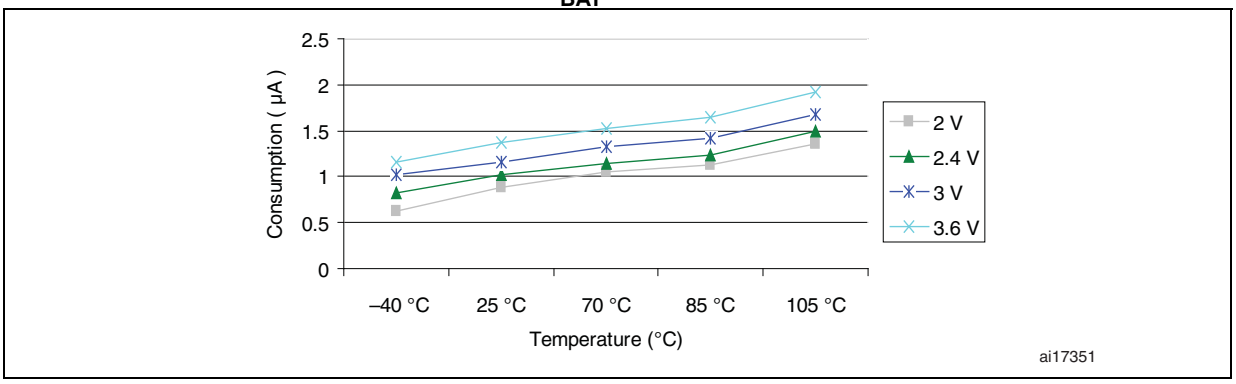
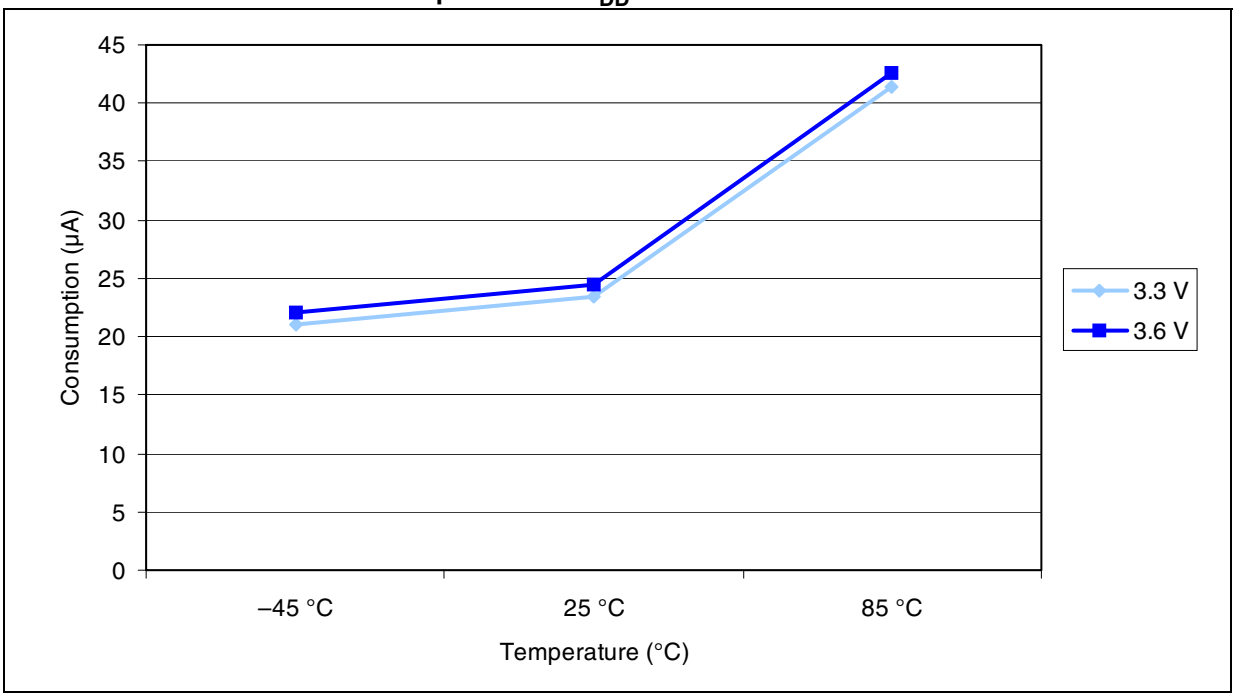


Figure 13. Typical current consumption in Stop mode with regulator in Run mode versus temperature at V_{DD} = 3.3 V and 3.6 V



Typical current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except if it is explicitly mentioned
- The Flash access time is adjusted to f_{HCLK} frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz)
- Prefetch is on (reminder: this bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled $f_{PCLK1} = f_{HCLK/4}$, $f_{PCLK2} = f_{HCLK/2}$, $f_{ADCCLK} = f_{PCLK2}/4$

The parameters given in *Table 16* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

Table 16. Typical current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Typ(1) All peripherals enabled(2)	Typ(1) All peripherals disabled	Unit
I_{DD}	Supply current in Run mode	External clock(3)	48 MHz	21.9	17.4	mA
			36 MHz	17.2	13.8	
			24 MHz	11.2	8.9	
			16 MHz	8.1	6.6	
			8 MHz	5	4.2	
			4 MHz	3	2.6	
			2 MHz	2	1.8	
			1 MHz	1.5	1.4	
			500 kHz	1.2	1.2	
			125 kHz	1.05	1	
		Running on high speed internal RC (HSI), AHB prescaler used to reduce the frequency	48 MHz	21.2	16.7	
			36 MHz	16.5	13.1	
			24 MHz	10.5	8.2	
			16 MHz	7.4	5.9	
			8 MHz	4.3	3.6	
			4 MHz	2.4	2	
			2 MHz	1.5	1.3	
			1 MHz	1.0	0.9	
			500 kHz	0.7	0.65	
			125 kHz	0.5	0.45	

1. Typical values are measures at $T_A = 25$ °C, $V_{DD} = 3.3$ V.
2. Add an additional power consumption of 0.8 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).

3. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Table 17. Typical current consumption in Sleep mode, code running from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Typ(1)	Typ(1)	Unit
				All peripherals enabled(2)	All peripherals disabled	
I_{DD}	Supply current in Sleep mode	External clock(3)	48 MHz	8.7	3.8	mA
			36 MHz	6.7	3.1	
			24 MHz	4.8	2.3	
			16 MHz	3.4	1.8	
			8 MHz	2	1.2	
			4 MHz	1.5	1.1	
			2 MHz	1.25	1	
			1 MHz	1.1	0.98	
			500 kHz	1.05	0.96	
			125 kHz	1	0.95	
		Running on High Speed Internal RC (HSI), AHB prescaler used to reduce the frequency	48 MHz	8.1	3.2	
			36 MHz	6.1	2.5	
			24 MHz	4.2	1.7	
			16 MHz	2.8	1.2	
			8 MHz	1.4	0.55	
			4 MHz	0.9	0.5	
			2 MHz	0.7	0.45	
			1 MHz	0.55	0.42	
			500 kHz	0.48	0.4	
			125 kHz	0.4	0.38	

1. Typical values are measures at T_A = 25 °C, V_{DD} = 3.3 V.
2. Add an additional power consumption of 0.8 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).
3. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

5.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (Electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports), the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 29*. They are based on the EMS levels and classes defined in application note AN1709.

Table 29. EMS characteristics

Symbol	Parameter	Conditions	Level/Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK}= 48 MHz conforms to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK} = 48 MHz conforms to IEC 61000-4-4	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and pre qualification tests in relation with the EMC level requested for his application.

Software recommendations: the software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers, etc.)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second. To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Figure 27. SPI timing diagram - slave mode and CPHA=0

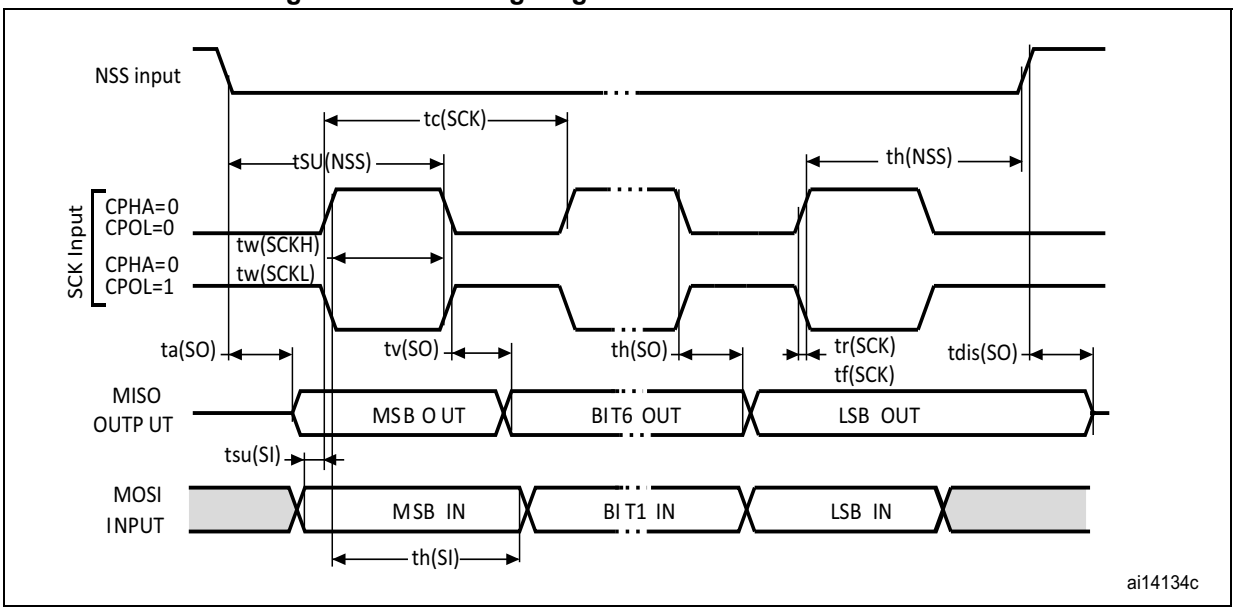
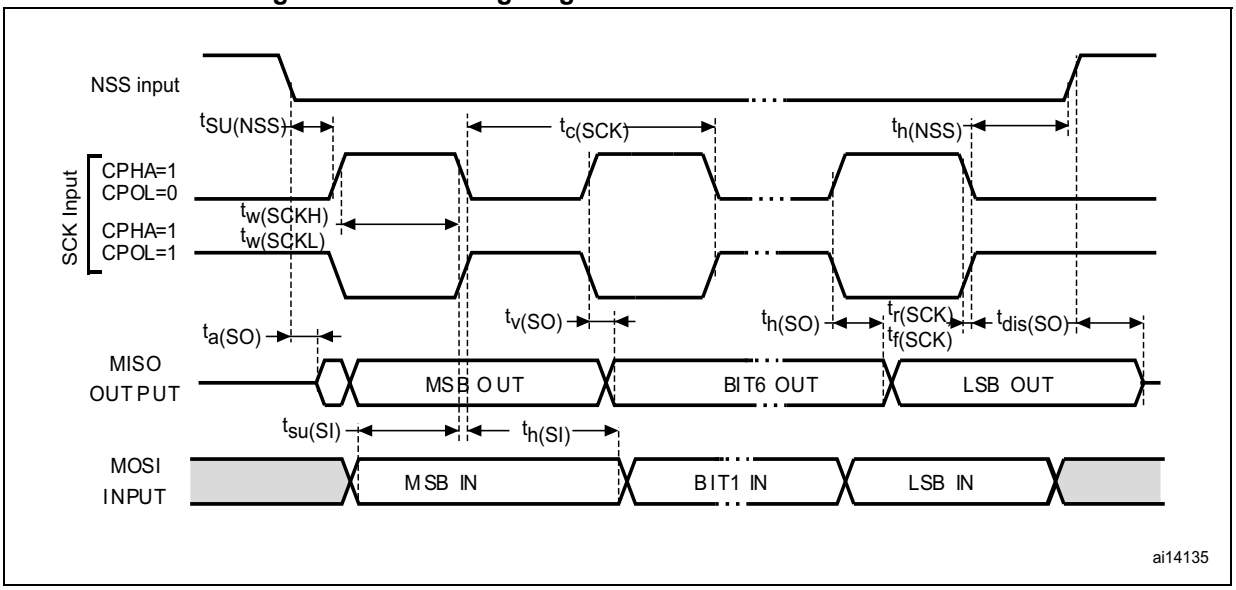


Figure 28. SPI timing diagram - slave mode and CPHA=1(1)

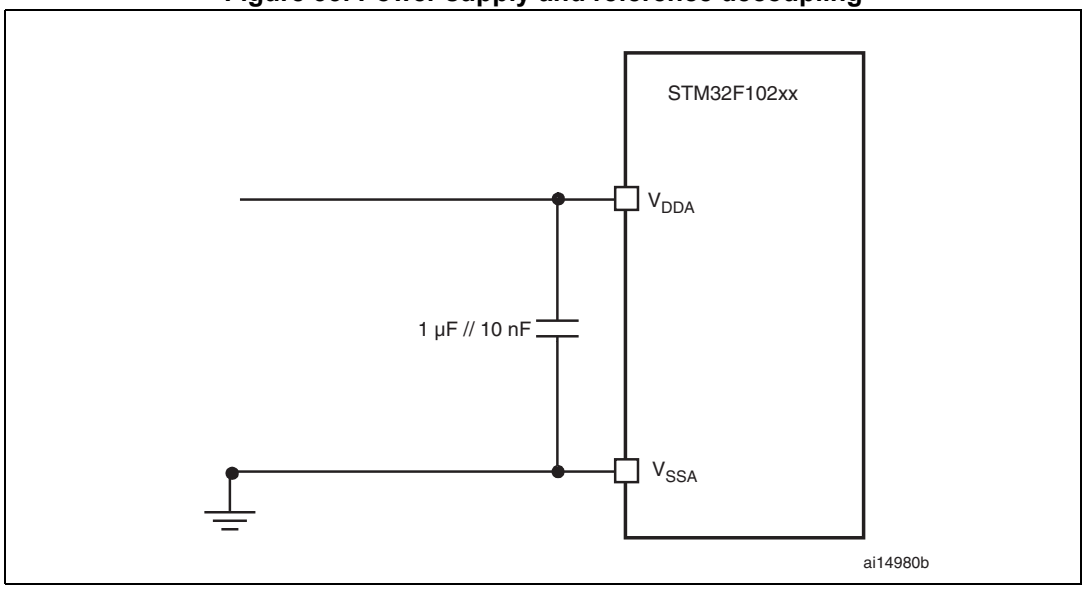


1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 33*. The 10 nF capacitors should be ceramic (good quality). They should be placed as close as possible to the chip.

Figure 33. Power supply and reference decoupling



5.3.18 Temperature sensor characteristics

Table 49. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	±1.5	-	°C
Avg_Slope(1)	Average slope	-	4.35	-	mV/°C
V_{25}(1)	Voltage at 25°C	-	1.42	-	V
t_{START}(2)	Startup time	4	-	10	µs
T_{S_temp}(3)(2)	ADC sampling time when reading the temperature	-	-	17.1	µs

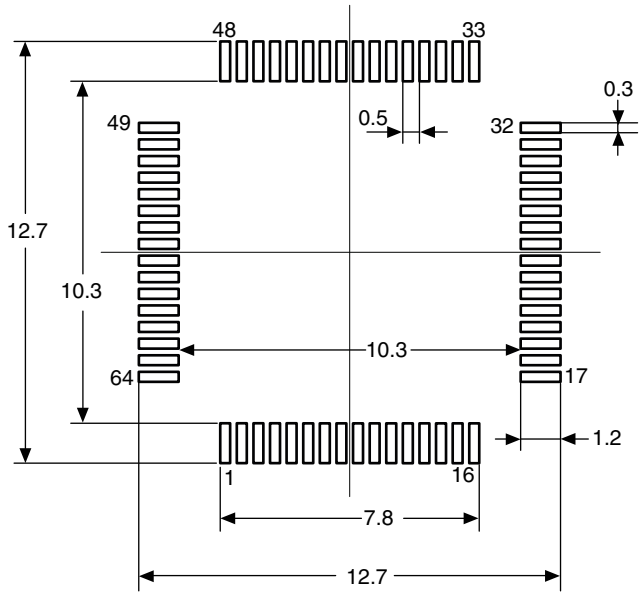
1. Guaranteed by characterization, not tested in production.
2. Data guaranteed by design, not tested in production.
3. Shortest sampling time can be determined in the application by multiple iterations.

Table 50. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 35. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

Table 51. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

6.4.1 Evaluating the maximum junction temperature for an application

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Table 53: Ordering information scheme*.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature. Here, only temperature range 6 is available (–40 to 85 °C).

The following example shows how to calculate the temperature range needed for a given application, making it possible to check whether the required temperature range is compatible with the STM32F102xx junction temperature range.

Example: High-performance application

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 82 °C (measured according to JESD51-2), I_{DDmax} = 50 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V and maximum 8 I/Os used at the same time in output mode at low level with I_{OL} = 20 mA, V_{OL}= 1.3 V

P_{INTmax} = 50 mA × 3.5 V= 175 mW

P_{IOmax} = 20 × 8 mA × 0.4 V + 8 × 20 mA × 1.3 V = 272 mW

This gives: P_{INTmax} = 175 mW and P_{IOmax} = 272 mW

P_{Dmax} = 175 + 272 = 447 mW

Thus: P_{Dmax} = 447 mW

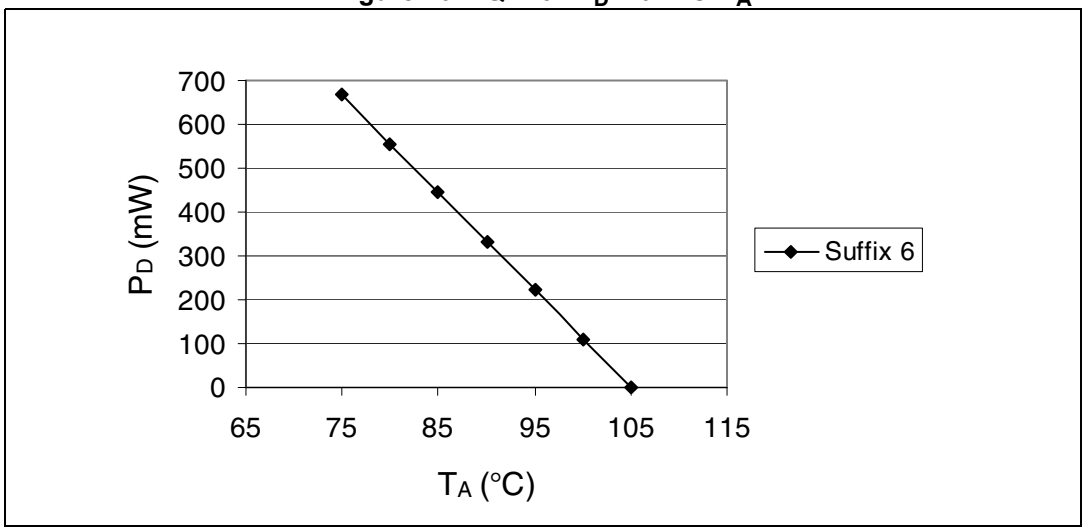
Using the values obtained in *Table 52* T_{Jmax} is calculated as follows:

– For LQFP64, 45 °C/W

T_{Jmax} = 82 °C + (45 °C/W × 447 mW) = 82 °C + 20.1 °C = 102.1 °C

This is within the junction temperature range of the STM32F102xx (–40 < T_J < 105 °C).

Figure 40. LQFP64 P_D max vs. T_A



7 Ordering information scheme

Table 53. Ordering information scheme

Example: STM32 F 102 C 6 T 6 A xxx

Device family

STM32 = ARM®-based 32-bit microcontroller

Product type

F = general-purpose

Device subfamily

102 = USB access line, USB 2.0 full-speed interface

Pin count

C = 48 pins

R = 64 pins

Flash memory size

4 = 16 Kbytes of Flash memory

6 = 32 Kbytes of Flash memory

Package

T = LQFP

Temperature range

6 = Industrial temperature range, –40 to 85 °C.

Internal code

“A” or blank(1)

Options

xxx = programmed parts

TR = tape and reel

1. For STM32F102x6 devices with a **blank** Internal code, please refer to the STM32F103x8/B datasheet available from the ST website: *www.st.com*.

Table 54. Document revision history (continued)

Date	Revision	Changes
02-Aug-2013	4	*Figure 2: Clock tree*: added FLITFCLK and *Note 3.*, and modified *Note 1.*. Removed sentence in “Unless otherwise specified the parameters ...” in *I2C interface characteristics* section. Added V_{IN} in *Table 8: General operating conditions*. Added note *5* in *Table 23: HSI oscillator characteristics* Added $DuCy_{(HSI)}$ in *Table 23: HSI oscillator characteristics* *Table 24: LSI oscillator characteristics*: removed note 2 related to oscillator selection, updated *Note 2.*, and $t_{SU(LSE)}$ specified for various ambient temperature values. Modified charge device model in *Table 33: I/O current injection susceptibility*. Updated ‘V_{IL}’ and ‘V_{IH}’ in *Table 34: I/O static characteristics*. Added notes to *Figure 20: Standard I/O input characteristics - CMOS port*, *Figure 21: Standard I/O input characteristics - TTL port*, *Figure 22: 5 V tolerant I/O input characteristics - CMOS port* and *Figure 23: 5 V tolerant I/O input characteristics - TTL port* *Table 37: Output voltage characteristics*: updated V_{OL} and V_{OH} conditions for TTL and CMOS outputs and added *Note 2.* Updated *Figure 24: I/O AC characteristics definition* Updated *Figure 25: Recommended NRST pin protection* Updated note *2.* and *3.* in *Table 39: I^2C characteristics* Updated *Figure 26: I2C bus AC waveforms and measurement circuit(1)* Updated title of *Table 40: SCL frequency (f_{PCLK1}= 36 MHz, V_{DD_I2C} = 3.3 V)* In *Table 43: SPI characteristics*, removed note 1 related to SPI1 remapped characteristics. Updated *Table 47: ADC characteristics* Updated *Section 6.1: Package mechanical data*
14-May-2015	5	Updated *Table 18: Peripheral current consumption* and *Table 39: I2C characteristics*. Updated *Section 6: Package characteristics*. Updated *Section 6.1: LQFP64 package information* with addition of *Device marking for LQFP64* and *Figure 36*. Updated *Section 6.2: LQFP48 package information* with addition of *Device marking for LQFP48* and *Figure 39*. Updated Disclaimer.