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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	37
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f102c4t6atr

List of tables

1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of STM32F102x4 and STM32F102x6 low-density USB access line microcontrollers. For more details on the whole STMicroelectronics STM32F102xx family. please refer to *Section 2.2: Full compatibility throughout the family*.

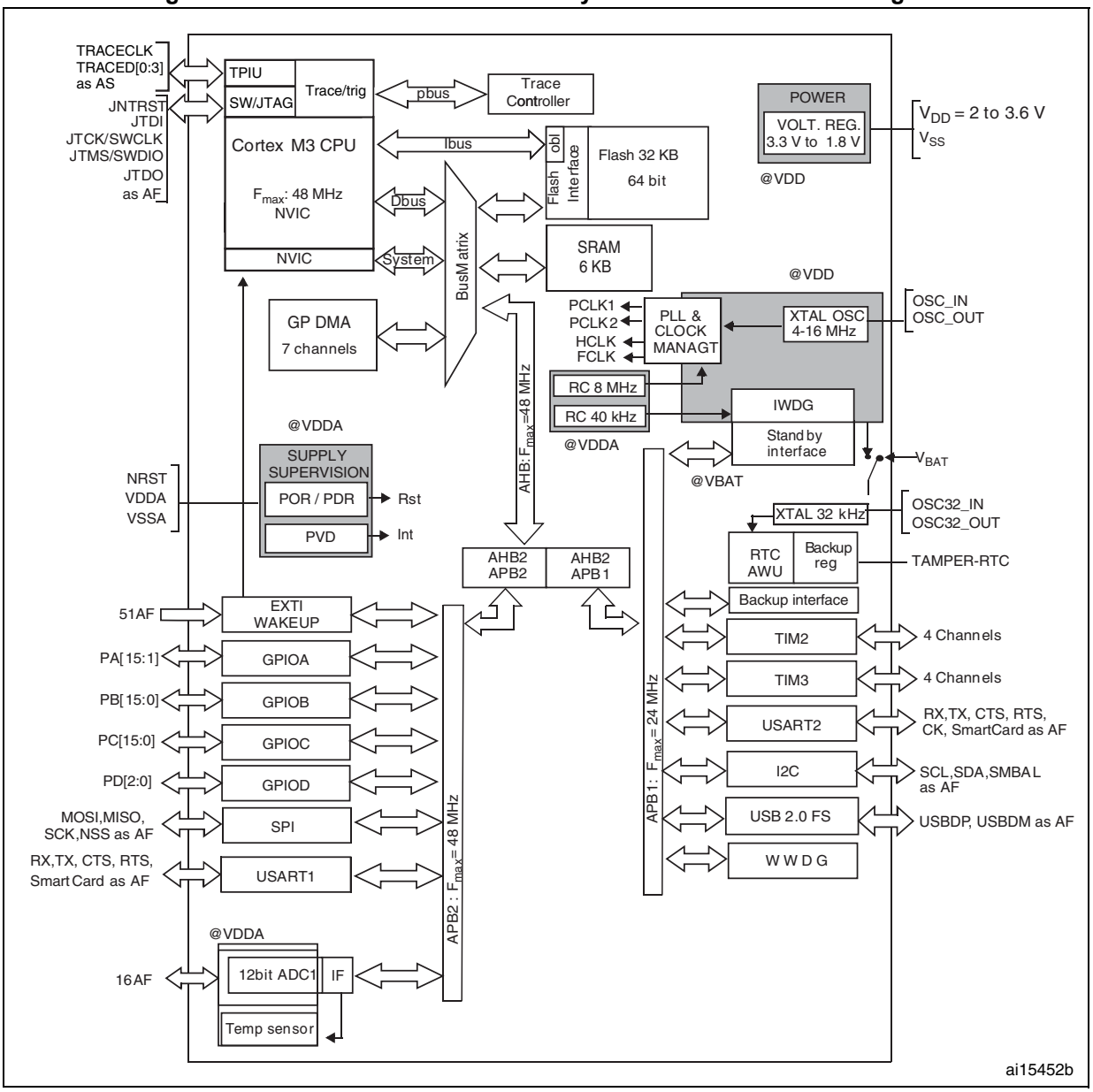
The medium-density STM32F102xx datasheet should be read in conjunction with the low-, medium- and high-density STM32F10xxx reference manual.

For information on programming, erasing and protection of the internal Flash memory please refer to the *STM32F10xxx Flash programming manual.*

The reference and Flash programming manuals are both available from the STMicroelectronics website *www.st.com*.

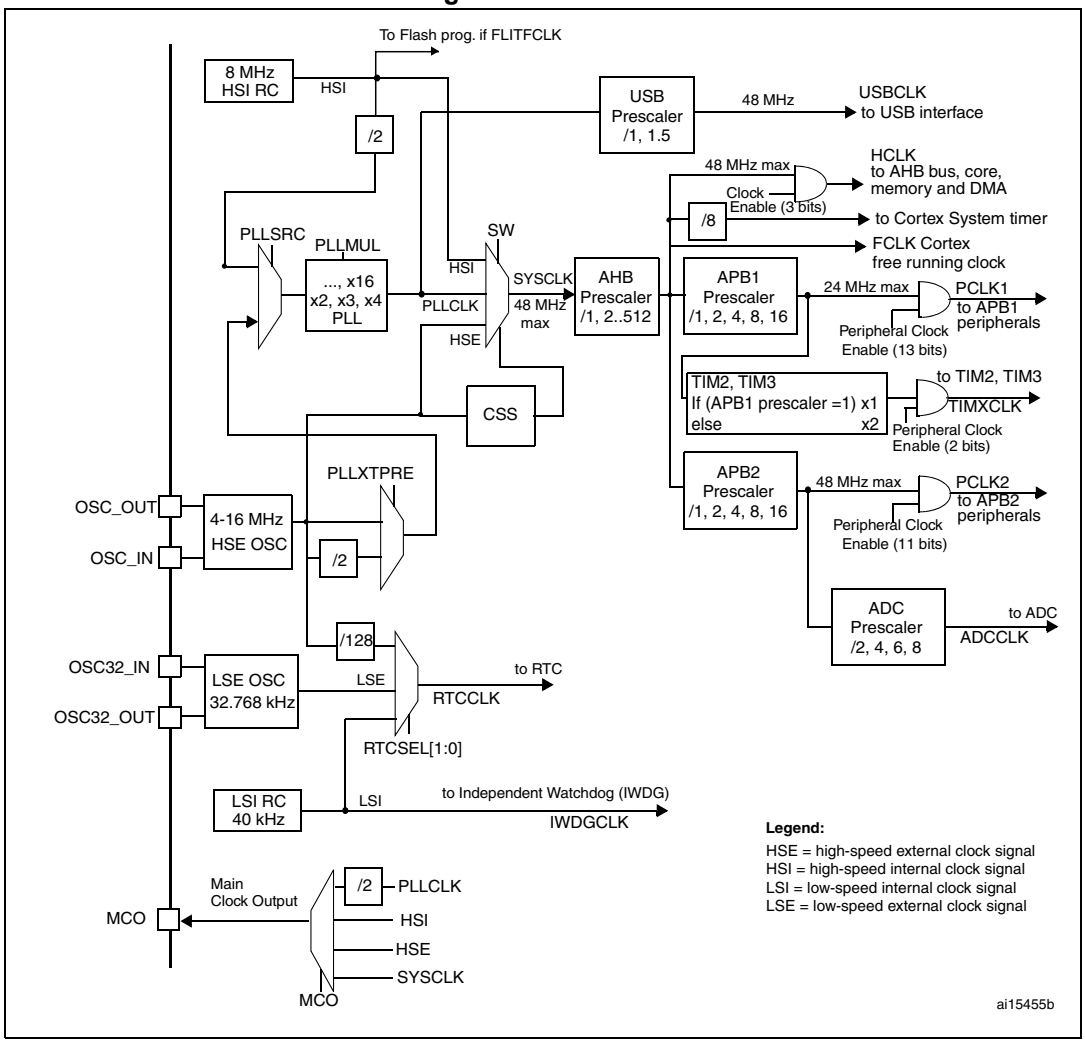
For information on the Cortex®-M3 core please refer to the Cortex®-M3 Technical Reference Manual, available from the ARM® website.

Figure 1. STM32F102T8 medium-density USB access line block diagram



1. AF = alternate function on I/O port pin.
2. T_A = –40 °C to +85 °C (junction temperature up to 105 °C).

Figure 2. Clock tree

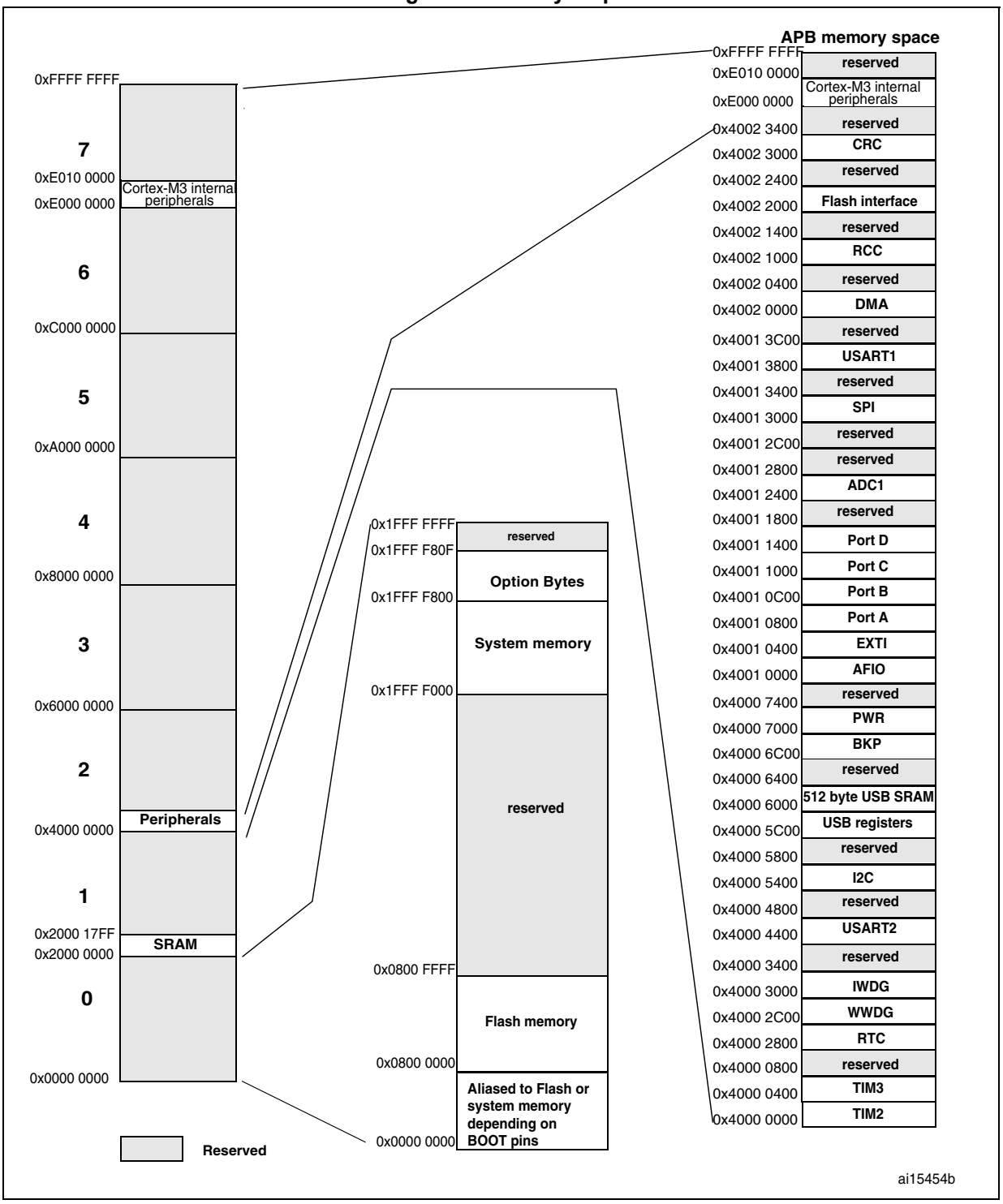


1. For the USB function to be available, both HSE and PLL must be enabled, with the USB clock output (USBCLK) at 48 MHz.
2. To have an ADC conversion time of 1.2 µs, APB2 must be at 12 MHz, 24 MHz or 48 MHz.
3. The Flash memory programming interface clock (FLITFCLK) is always the HSI clock.

4 Memory mapping

The memory map is shown in *Figure 5*.

Figure 5. Memory map



5.3 Operating conditions

5.3.1 General operating conditions

Table 8. General operating conditions

Symbol	Parameter	Conditions		Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-		0	48	MHz
f_{PCLK1}	Internal APB1 clock frequency	-		0	24	
f_{PCLK2}	Internal APB2 clock frequency	-		0	48	
V_{DD}	Standard operating voltage	-		2	3.6	V
V_{DDA}(1)	Analog operating voltage (ADC not used)	Must be the same potential as V_{DD}(2)		2	3.6	V
	Analog operating voltage (ADC used)			2.4	3.6	
V_{IN}	I/O input voltage	Standard IO		–0.3	V_{DD}+ 0.3	
		FTIO(3)	2 V < V_{DD} ≤ 3.6 V	–0.3	5.5	
			V_{DD} = 2 V	–0.3	5.2	
		BOOT0		0	5.5	
P_D	Power dissipation at T_A = 85 °C(4)	LQFP48		-	363	mW
		LQFP64		-	444	
T_A	Ambient temperature	Maximum power dissipation		–40	85	°C
		Low power dissipation(5)		–40	105	°C
T_J	Junction temperature range	-		–40	105	°C

1. When the ADC is used, refer to *Table 45: ADC characteristics*.
2. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and operation.
3. To sustain a voltage higher than V_{DD}+0.3 V, the internal pull-up/pull-down resistors must be disabled.
4. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed $T_J$max (see *Section 6.3: Thermal characteristics*).
5. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed $T_J$max (see *Section 6.3: Thermal characteristics*).

5.3.2 Operating conditions at power-up / power-down

Subject to general operating conditions for T_A.

Table 9. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	∞	µs/V
	V_{DD} fall time rate		20	∞	

Table 14. Maximum current consumption in Sleep mode, code running from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Max(1)	Unit
				T_A = 85 °C	
I_{DD}	Supply current in Sleep mode	External clock(2), all peripherals enabled	48 MHz	17	mA
			36 MHz	14	
			24 MHz	10	
			16 MHz	7	
			8 MHz	4	
		External clock(2), all peripherals disabled	48 MHz	6	
			36 MHz	5	
			24 MHz	4.5	
			16 MHz	4	
			8 MHz	3	

1. Based on characterization, tested in production at V_{DD} max and f_{HCLK} max with peripherals enabled.
2. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Table 15. Typical and maximum current consumptions in Stop and Standby modes

Symbol	Parameter	Conditions	Typ(1)			Max	Unit
			V_{DD}/ V_{BAT} = 2.4 V	V_{DD}/V_{BAT} = 3.3 V	V_{DD}/V_{BAT} = 2.0 V	T_A = 85 °C	
I_{DD}	Supply current in Stop mode	Regulator in Run mode. Low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	21.3	21.7	-	160	µA
		Regulator in Low Power mode. Low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	11.3	11.7	-	145	
	Supply current in Standby mode(2)	Low-speed internal RC oscillator and independent watchdog ON	2.75	3.4	-	-	
		Low-speed internal RC oscillator ON, independent watchdog OFF	2.55	3.2	-	-	
		Low-speed internal RC oscillator and independent watchdog OFF, low-speed oscillator and RTC OFF	1.55	1.9	-	3.2	
I_{DD_VBAT}	Backup domain supply current	Low-speed oscillator and RTC ON	1.1	1.4	0.9	1.9(3)	

1. Typical values are measured at T_A = 25 °C.

3. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Table 17. Typical current consumption in Sleep mode, code running from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Typ(1)	Typ(1)	Unit
				All peripherals enabled(2)	All peripherals disabled	
I_{DD}	Supply current in Sleep mode	External clock(3)	48 MHz	8.7	3.8	mA
			36 MHz	6.7	3.1	
			24 MHz	4.8	2.3	
			16 MHz	3.4	1.8	
			8 MHz	2	1.2	
			4 MHz	1.5	1.1	
			2 MHz	1.25	1	
			1 MHz	1.1	0.98	
			500 kHz	1.05	0.96	
			125 kHz	1	0.95	
		Running on High Speed Internal RC (HSI), AHB prescaler used to reduce the frequency	48 MHz	8.1	3.2	
			36 MHz	6.1	2.5	
			24 MHz	4.2	1.7	
			16 MHz	2.8	1.2	
			8 MHz	1.4	0.55	
			4 MHz	0.9	0.5	
			2 MHz	0.7	0.45	
			1 MHz	0.55	0.42	
			500 kHz	0.48	0.4	
			125 kHz	0.4	0.38	

1. Typical values are measures at T_A = 25 °C, V_{DD} = 3.3 V.
2. Add an additional power consumption of 0.8 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).
3. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 18*. The MCU is placed under the following conditions:

- all I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- ambient operating temperature and V_{DD} supply voltage conditions as summarized in *Table 5*.

Table 18. Peripheral current consumption(1)

Peripheral		µA/MHz
AHB (up to 48 MHz)	DMA1	15.97
	CRC	1.67
	BusMatrix(2)	8.33
APB1 (up to 24 MHz)	APB1-Bridge	7.22
	TIM2	33.33
	TIM3	33.61
	USART2	12.78
	I2C1	10.83
	USB	16.94
	WWDG	3.33
	PWR	1.94
	BKP	2.78
	IWDG	1.39
APB2 (up to 48 MHz)	APB2-Bridge	3.33
	GPIOA	7.50
	GPIOB	6.81
	GPIOC	7.22
	GPIOD	6.94
	SPI1	4.86
	USART1	12.78
	ADC1(3) (4)	15.54

1. f_{HCLK} = 48 MHz, $f_{APB1} = f_{HCLK}/2$, $f_{APB2} = f_{HCLK}$, default prescaler value for each peripheral.
2. The BusMatrix is automatically active when at least one master is ON.
3. Specific conditions for ADC: f_{HCLK} = 48 MHz, $f_{APB1} = f_{HCLK}/2$, $f_{APB2} = f_{HCLK}$, $f_{ADCCLK} = f_{APB2}/4$.
4. When ADON bit in the ADC_CR2 register is set to 1, there is an additional current consumption of 0, 68 mA. When we enable the ADC, there is an additional current consumption of 0, 06 mA.

5.3.6 External clock source characteristics

High-speed external user clock generated from an external source

The characteristics given in *Table 19* result from tests performed using an high-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 8*.

Table 19. High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency(1)	-	1	8	25	MHz
V_{HSEH}	OSC_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HSE)}$ $t_{w(HSE)}$	OSC_IN high or low time(1)		5	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time(1)		-	-	20	
$C_{in(HSE)}$	OSC_IN input capacitance(1)		-	5		pF
$DuCy_{(HSE)}$	Duty cycle		45	-	55	%
I_L	OSC_IN Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$		-	±1	µA

1. Guaranteed by design, not tested in production.

Low-speed external user clock generated from an external source

The characteristics given in *Table 21* result from tests performed using an low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 8*.

Table 20. Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency(1)	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSE)}$ $t_{w(LSE)}$	OSC32_IN high or low time(1)		450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time(1)		-	-	50	
$C_{in(LSE)}$	OSC32_IN input capacitance(1)		-	5	-	pF
$DuCy_{(LSE)}$	Duty cycle		30	-	70	%
I_L	OSC32_IN Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	±1	µA

1. Guaranteed by design, not tested in production.

High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 16 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 21*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

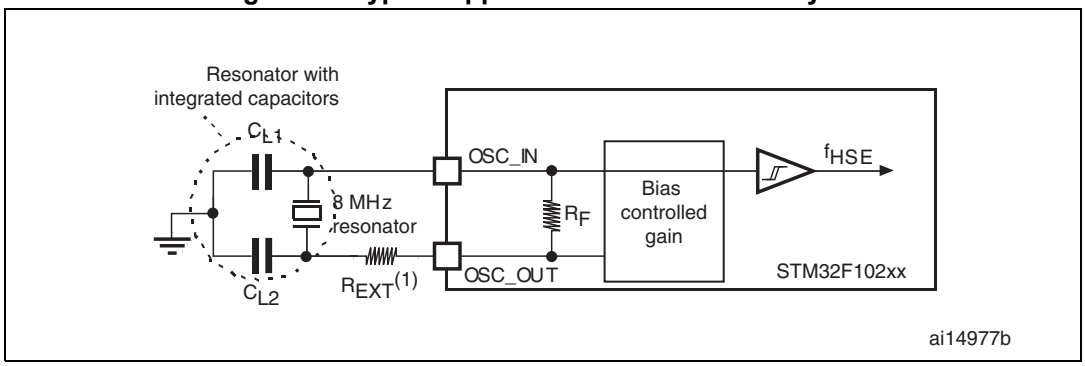
Table 21. HSE 4-16 MHz oscillator characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	16	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
C	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)(3)	R_S = 30 Ω	-	30	-	pF
i_2	HSE driving current	V_{DD} = 3.3 V V_{IN} = V_{SS} with 30 pF load	-	-	1	mA
g_m	Oscillator transconductance	Startup	25	-	-	mA/V
$t_{SU(HSE)}$(4)	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Based on characterization results, not tested in production.
3. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 18*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}. Refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website *www.st.com*.

Figure 18. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 22*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 22. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R_F	Feedback resistor	-		-	5	-	MΩ
$C^{(1)}$	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)	R_S = 30 kΩ		-	-	15	pF
I_2	LSE driving current	V_{DD} = 3.3 V V_{IN} = V_{SS}		-	-	1.4	µA
g_m	Oscillator transconductance	-		5	-	-	µA/V
$t_{SU(LSE)}^{(2)}$	Startup time	V_{DD} is stabilized	T_A = 50 °C	-	1.5	-	s
			T_A = 25 °C	-	2.5	-	
			T_A = 10 °C	-	4.0	-	
			T_A = 0 °C	-	6.0	-	
			T_A = -10 °C	-	10.0	-	
			T_A = -20 °C	-	17.0	-	
			T_A = -30 °C	-	32.0	-	
			T_A = -40 °C	-	60.0	-	

1. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
2. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled by software to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and can vary significantly with the crystal manufacturer, PCB layout and humidity.

2. Refer to application note AN2868 “STM32F10xxx internal RC oscillator (HSI) calibration” available from the ST website www.st.com.
3. Guaranteed by design, not tested in production.
4. Based on characterization, not tested in production.
5. The actual frequency of HSI oscillator may be impacted by a reflow, but does not drift out of the specified range.

Low-speed internal (LSI) RC oscillator

Table 24. LSI oscillator characteristics (1)

Symbol	Parameter	Min(2)	Typ	Max	Unit
f_{LSI}	Frequency	30	40	60	kHz
$t_{su(LSI)}$(3)	LSI oscillator startup time	-	-	85	µs
$I_{DD(LSI)}$(3)	LSI oscillator power consumption	-	0.65	1.2	µA

1. V_{DD} = 3 V, T_A = -40 to 85 °C unless otherwise specified.
2. Based on characterization, not tested in production.
3. Guaranteed by design, not tested in production.

Wakeup time from low-power mode

The wakeup times given in *Table 25* is measured on a wakeup phase with a 8-MHz HSI RC oscillator. The clock source used to wake up the device depends from the current operating mode:

- Stop or Standby mode: the clock source is the RC oscillator
- Sleep mode: the clock source is the clock that was set before entering Sleep mode.

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

Table 25. Low-power mode wakeup timings

Symbol	Parameter	Typ	Unit
$t_{WUSLEEP}$(1)	Wakeup from Sleep mode	1.8	µs
t_{WUSTOP}(1)	Wakeup from Stop mode (regulator in run mode)	3.6	µs
	Wakeup from Stop mode (regulator in low-power mode)	5.4	
$t_{WUSTDBY}$(1)	Wakeup from Standby mode	50	µs

1. The wakeup times are measured from the wakeup event to the point at which the user application code reads the first instruction.

5.3.8 PLL characteristics

The parameters given in *Table 26* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device is monitored while a simple application is executed (toggling 2 LEDs through the I/O ports), This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 30. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{HCLK}]	Unit
				8/48 MHz	
S_{EMI}	Peak level	V_{DD} = 3.3 V, T_A = 25 °C.	0.1 MHz to 30 MHz	7	dBµV
			30 MHz to 130 MHz	8	
			130 MHz to 1GHz	13	
			SAE EMI Level	3.5	-

5.3.11 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 31. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to JESD22-A114	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to ANSI/ESD STM5.3.1	II	500	

1. Based on characterization results, not tested in production.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78 IC latch-up standard.

Table 32. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II level A

Table 34. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low level input voltage	Standard IO input low level voltage	-	-	$0.28*(V_{DD}-2\ V)+0.8\ V$(1)	V
		IO FT(3) input low level voltage	-	-	$0.32*(V_{DD}-2V)+0.75\ V$(1)	
		All I/Os except BOOT0	-	-	$0.35V_{DD}$(2)	
V_{IH}	High level input voltage	Standard IO input high level voltage	$0.41*(V_{DD}-2\ V)+1.3\ V$(1)	-	-	
		IO FT(3) input high level voltage	$0.42*(V_{DD}-2\ V)+1\ V$(1)	-	-	
		All I/Os except BOOT0	$0.65V_{DD}$(2)	-	-	
V_{hys}	Standard IO Schmitt trigger voltage hysteresis(4)	-	200	-	-	mV
	IO FT Schmitt trigger voltage hysteresis(4)	-	5% V_{DD}(5)	-	-	
I_{lkg}	Input leakage current (6)	$V_{SS} \le V_{IN} \le V_{DD}$ Standard I/Os	-	-	±1	µA
		V_{IN} = 5 V I/O FT	-	-	3	
R_{PU}	Weak pull-up equivalent resistor(7)	$V_{IN} = V_{SS}$	30	40	50	kΩ
R_{PD}	Weak pull-down equivalent resistor(7)	$V_{IN} = V_{DD}$	30	40	50	
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Data based on design simulation.
2. Tested in production.
3. FT = Five-volt tolerant, In order to sustain a voltage higher than V_{DD}+0.3 the internal pull-up/pull-down resistors must be disabled.
4. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization, not tested in production.
5. With a minimum of 100 mV.
6. Leakage could be higher than max, if negative current is injected on adjacent pins.
7. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimum (~10% order).

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 24* and *Table 36*, respectively.

Unless otherwise specified, the parameters given in *Table 36* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

Table 36. I/O AC characteristics(1)

MODEx [1:0] bit value(1)	Symbol	Parameter	Conditions	Max	Unit
10	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	2	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	125(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time		125(3)	
01	$f_{max(IO)out}$	Maximum frequency(2)	C_L= 50 pF, V_{DD} = 2 V to 3.6 V	10	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L= 50 pF, V_{DD} = 2 V to 3.6 V	25(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time		25(3)	
11	$F_{max(IO)out}$	Maximum Frequency(2)	C_L= 30 pF, V_{DD} = 2.7 V to 3.6 V	50	MHz
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	30	MHz
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	20	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	5(3)	ns
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	8(3)	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	12(3)	
	$t_{r(IO)out}$	Output low to high level rise time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	5(3)	
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	8(3)	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	12(3)	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller	-	10	ns

1. The I/O speed is configured using the MODEx[1:0] bits. Refer to the STM32F10xxx reference manual for a description of GPIO Port configuration register.
2. The maximum frequency is defined in *Figure 24*.
3. Guaranteed by design, not tested in production.

Table 39. I^2C characteristics

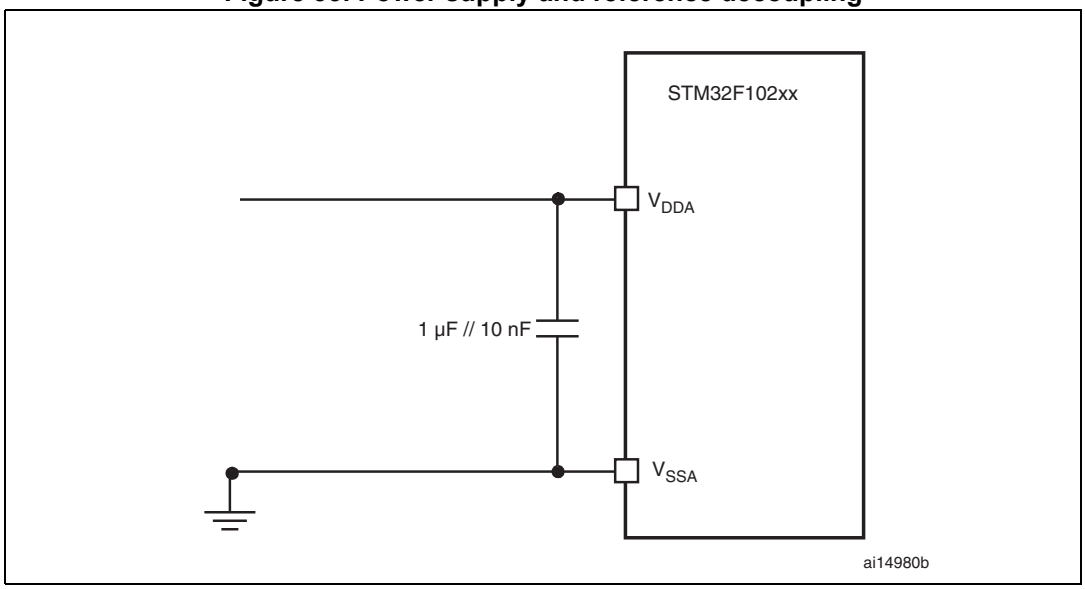
Symbol	Parameter	Standard mode I^2C(1)(2)		Fast mode I^2C(1)(2)		Unit
		Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	-	3450(3)	-	900(3)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	-	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	
$t_{h(STA)}$	Start condition hold time	4.0	-	0.6	-	µs
$t_{su(STA)}$	Repeated Start condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	Stop condition setup time	4.0	-	0.6	-	µs
$t_{w(STO:STA)}$	Stop to Start condition time (bus free)	4.7	-	1.3	-	µs
t_{SP}	Pulse width of spikes that are suppressed by the analog filter	0	50(4)	0	50(4)	ns
C_b	Capacitive load for each bus line	-	400	-	400	pF

1. Values guaranteed by design, not tested in production.
2. f_{PCLK1} must be at least 2 MHz to achieve standard mode I^2C frequencies. It must be at least 4 MHz to achieve fast mode I^2C frequencies. It must be a multiple of 10 MHz to reach the 400 kHz maximum I2C fast mode clock.
3. The maximum Data hold time has only to be met if the interface does not stretch the low period of the SCL signal.
4. The analog filter minimum filtered spikes is above $t_{SP(max)}$ to ensure that spikes width up to $t_{SP(max)}$ are filtered.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 33*. The 10 nF capacitors should be ceramic (good quality). They should be placed as close as possible to the chip.

Figure 33. Power supply and reference decoupling



5.3.18 Temperature sensor characteristics

Table 49. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	±1.5	-	°C
Avg_Slope(1)	Average slope	-	4.35	-	mV/°C
V_{25}(1)	Voltage at 25°C	-	1.42	-	V
t_{START}(2)	Startup time	4	-	10	µs
T_{S_temp}(3)(2)	ADC sampling time when reading the temperature	-	-	17.1	µs

1. Guaranteed by characterization, not tested in production.
2. Data guaranteed by design, not tested in production.
3. Shortest sampling time can be determined in the application by multiple iterations.

Table 54. Document revision history (continued)

Date	Revision	Changes
02-Aug-2013	4	*Figure 2: Clock tree*: added FLITFCLK and *Note 3.*, and modified *Note 1.*. Removed sentence in “Unless otherwise specified the parameters ...” in *I2C interface characteristics* section. Added V_{IN} in *Table 8: General operating conditions*. Added note *5* in *Table 23: HSI oscillator characteristics* Added $DuCy_{(HSI)}$ in *Table 23: HSI oscillator characteristics* *Table 24: LSI oscillator characteristics*: removed note 2 related to oscillator selection, updated *Note 2.*, and $t_{SU(LSE)}$ specified for various ambient temperature values. Modified charge device model in *Table 33: I/O current injection susceptibility*. Updated ‘V_{IL}’ and ‘V_{IH}’ in *Table 34: I/O static characteristics*. Added notes to *Figure 20: Standard I/O input characteristics - CMOS port*, *Figure 21: Standard I/O input characteristics - TTL port*, *Figure 22: 5 V tolerant I/O input characteristics - CMOS port* and *Figure 23: 5 V tolerant I/O input characteristics - TTL port* *Table 37: Output voltage characteristics*: updated V_{OL} and V_{OH} conditions for TTL and CMOS outputs and added *Note 2.* Updated *Figure 24: I/O AC characteristics definition* Updated *Figure 25: Recommended NRST pin protection* Updated note *2.* and *3.* in *Table 39: I^2C characteristics* Updated *Figure 26: I2C bus AC waveforms and measurement circuit(1)* Updated title of *Table 40: SCL frequency (f_{PCLK1}= 36 MHz, V_{DD_I2C} = 3.3 V)* In *Table 43: SPI characteristics*, removed note 1 related to SPI1 remapped characteristics. Updated *Table 47: ADC characteristics* Updated *Section 6.1: Package mechanical data*
14-May-2015	5	Updated *Table 18: Peripheral current consumption* and *Table 39: I2C characteristics*. Updated *Section 6: Package characteristics*. Updated *Section 6.1: LQFP64 package information* with addition of *Device marking for LQFP64* and *Figure 36*. Updated *Section 6.2: LQFP48 package information* with addition of *Device marking for LQFP48* and *Figure 39*. Updated Disclaimer.