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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	37
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f102c6t6atr

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Low-power modes

The STM32F102xx medium-density USB access line supports three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**
In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.
- **Stop mode**
The Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low power mode.
The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output or the RTC alarm.
- **Standby mode**
The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and registers content are lost except for registers in the Backup domain and Standby circuitry.
The device exits Standby mode when an external reset (NRST pin), a IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

DMA

The flexible 7-channel general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I²C, USART, general purpose timers TIMx and ADC.

RTC (real-time clock) and backup registers

The RTC and the backup registers are supplied through a switch that takes power either on V_{DD} supply when present or through the V_{BAT} pin. The backup registers are ten 16-bit registers used to store 20 bytes of user application data when V_{DD} power is not present.

The real-time clock provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and a periodic interrupt. It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low power RC oscillator or the high-speed external clock divided by 128. The internal low power RC has a typical frequency of 40 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural crystal deviation. The RTC features a 32-bit programmable counter for long term measurement using the Compare

register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

SysTick timer

This timer is dedicated for OS, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

General-purpose timers (TIMx)

There are 2 synchronizable general-purpose timers embedded in the STM32F102xx medium-density USB access line devices. These timers are based on a 16-bit auto-reload up/down counter, a 16-bit prescaler and feature 4 independent channels each for input capture, output compare, PWM or one-pulse mode output. This gives up to 12 input captures / output compares / PWMs on the LQFP48 and LQFP64 packages. The general-purpose timers can work together via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode.

Any of the general-purpose timers can be used to generate PWM outputs. They both have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

I²C bus

One I²C bus interface can operate in multi-master and slave modes. It can support standard and fast modes. It supports dual slave addressing (7-bit only) and both 7/10-bit addressing in master mode. A hardware CRC generation/verification is embedded.

The I²C interface can be served by DMA and they support SM Bus 2.0/PM Bus.

Universal synchronous/asynchronous receiver transmitter (USART)

The available USART interfaces communicate at up to 2.25 Mbit/s. They provide hardware management of the CTS and RTS signals, support IrDA SIR ENDEC, are ISO 7816 compliant and have LIN Master/Slave capability.

The USART interfaces can be served by the DMA controller.

Serial peripheral interface (SPI)

The SPI is able to communicate up to 12 Mbit/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

The SPI can be served by the DMA controller.

Universal serial bus (USB)

The STM32F102xx medium-density USB access line embeds an USB device peripheral compatible with the USB Full-speed 12 Mbs. The USB interface implements a full-speed (12 Mbit/s) function interface. It has software configurable endpoint setting and suspend/resume support. The dedicated 48 MHz clock is generated from the internal main PLL (the clock source must use a HSE crystal oscillator).

GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current capable.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

ADC (analog to digital converter)

The 12-bit analog to digital converter has up to 16 external channels and performs conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between $2\text{ V} < V_{\text{DDA}} < 3.6\text{ V}$. The temperature sensor is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.

Serial wire JTAG debug port (SWJ-DP)

The ARM® SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

3 Pinout and pin description

Figure 3. STM32F102xx medium-density USB access line LQFP48 pinout

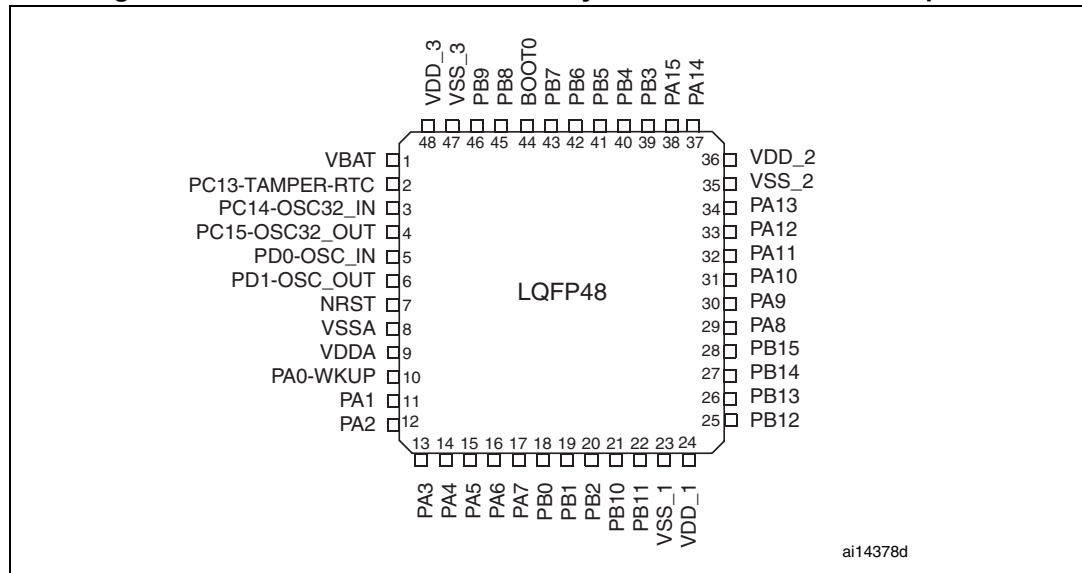


Figure 4. STM32F102xx medium-density USB access line LQFP64 pinout

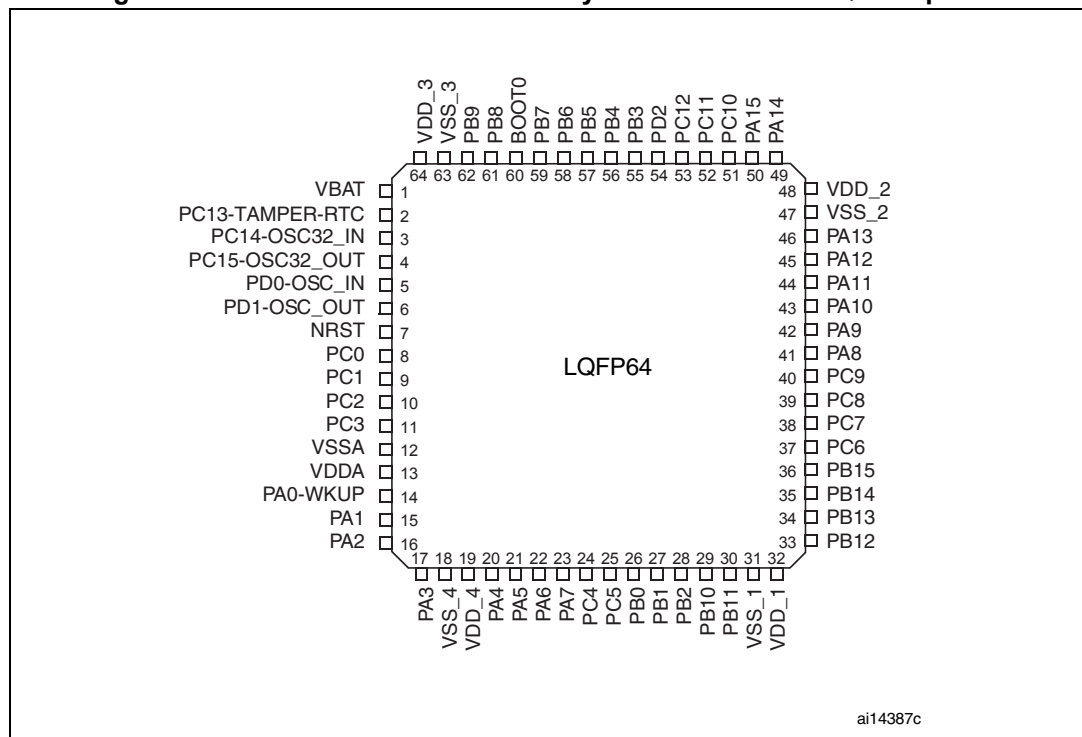


Table 4. Low-density STM32F102xx pin definitions (continued)

Pins		Pin name	Type ⁽¹⁾	I/O level ⁽²⁾	Main function ⁽³⁾ (after reset)	Alternate functions ^{(3) (4)}	
LQFP48	LQFP64					Default	Remap
20	28	PB2	I/O	FT	PB2/BOOT1	-	-
21	29	PB10	I/O	FT	PB10	⁽⁸⁾	TIM2_CH3
22	30	PB11	I/O	FT	PB11	⁽⁸⁾	TIM2_CH4
23	31	V _{SS_1}	S	-	V _{SS_1}	-	-
24	32	V _{DD_1}	S	-	V _{DD_1}	-	-
25	33	PB12	I/O	FT	PB12	⁽⁸⁾	-
26	34	PB13	I/O	FT	PB13	-	-
27	35	PB14	I/O	FT	PB14	-	-
28	36	PB15	I/O	FT	PB15	-	-
-	37	PC6	I/O	FT	PC6	-	TIM3_CH1
-	38	PC7	I/O	FT	PC7	-	TIM3_CH2
-	39	PC8	I/O	FT	PC8	-	TIM3_CH3
-	40	PC9	I/O	FT	PC9	-	TIM3_CH4
29	41	PA8	I/O	FT	PA8	USART1_CK/MCO	-
30	42	PA9	I/O	FT	PA9	USART1_TX ⁽⁸⁾	-
31	43	PA10	I/O	FT	PA10	USART1_RX ⁽⁸⁾	-
32	44	PA11	I/O	FT	PA11	USART1_CTS/USB_DM	-
33	45	PA12	I/O	FT	PA12	USART1_RTS/USB_DP	-
34	46	PA13	I/O	FT	JTMS-SWDIO	-	PA13
35	47	V _{SS_2}	S	-	V _{SS_2}	-	-
36	48	V _{DD_2}	S	-	V _{DD_2}	-	-
37	49	PA14	I/O	FT	JTCK/SWCLK	-	PA14
38	50	PA15	I/O	FT	JTDI	-	TIM2_CH1_ETR / PA15 / SPI_NSS
-	51	PC10	I/O	FT	PC10	-	-
-	52	PC11	I/O	FT	PC11	-	-
-	53	PC12	I/O	FT	PC12	-	-
-	54	PD2	I/O	FT	PD2	-	-
39	55	PB3	I/O	FT	JTDO	-	TIM2_CH2/PB3/ TRACESWO/ SPI_SCK

Table 4. Low-density STM32F102xx pin definitions (continued)

Pins		Pin name	Type ⁽¹⁾	I/O level ⁽²⁾	Main function ⁽³⁾ (after reset)	Alternate functions ^{(3) (4)}	
LQFP48	LQFP64					Default	Remap
40	56	PB4	I/O	FT	JNTRST	-	TIM3_CH1 / PB4 SPI_MISO
41	57	PB5	I/O	-	PB5	I2C_SMBA	TIM3_CH2 / SPI_MOSI
42	58	PB6	I/O	FT	PB6	I2C_SCL ⁽⁸⁾	USART1_TX
43	59	PB7	I/O	FT	PB7	I2C_SDA ⁽⁸⁾	USART1_RX
44	60	BOOT0	I	-	BOOT0	-	-
45	61	PB8	I/O	FT	PB8	-	I2C_SCL
46	62	PB9	I/O	FT	PB9	-	I2C_SDA
47	63	V _{SS_3}	S	-	V _{SS_3}	-	-
48	64	V _{DD_3}	S	-	V _{DD_3}	-	-

1. I = input, O = output, S = supply.

2. FT= 5 V tolerant.

3. Function availability depends on the chosen device. For devices having reduced peripheral counts, it is always the lower number of peripherals that is included. For example, if a device has only one SPI, two USARTs and two timers, they will be called SPI1, USART1 & USART2 and TIM2 & TIM 3, respectively. Refer to [Table 3 on page 12](#).

4. If several peripherals share the same I/O pin, to avoid conflict between these alternate functions only one peripheral should be enabled at a time through the peripheral clock enable bit (in the corresponding RCC peripheral clock enable register).

5. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited: the speed should not exceed 2 MHz with a maximum load of 30 pF and these IOs must not be used as a current source (e.g. to drive an LED).

6. Main function after the first backup domain power-up. Later on, it depends on the contents of the Backup registers even after reset (because these registers are not reset by the main reset). For details on how to manage these IOs, refer to the Battery backup domain and BKP register description sections in the STM32F102xx reference manual, available from the STMicroelectronics website: www.st.com.

7. The pins number 5 and 6 in the LQFP48 package are configured as OSC_IN/OSC_OUT after reset, however the functionality of PD0 and PD1 can be remapped by software on these pins. For more details, refer to the Alternate function I/O and debug configuration section in the STM32F10xxx reference manual. The use of PD0 and PD1 in output mode is limited as they can only be used at 50 MHz in output mode.

8. This alternate function can be remapped by software to some other port pins (if available on the used package). For more details, refer to the Alternate function I/O and debug configuration section in the STM32F10xxx reference manual, available from the STMicroelectronics website: www.st.com.

5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS} .

5.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A = 25\text{ }^{\circ}\text{C}$ and $T_A = T_{A\text{max}}$ (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation ($\text{mean} \pm 3\sigma$).

5.1.2 Typical values

Unless otherwise specified, typical data are based on $T_A = 25\text{ }^{\circ}\text{C}$, $V_{DD} = 3.3\text{ V}$ (for the $2\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated ($\text{mean} \pm 2\sigma$).

5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

5.1.4 Loading capacitor

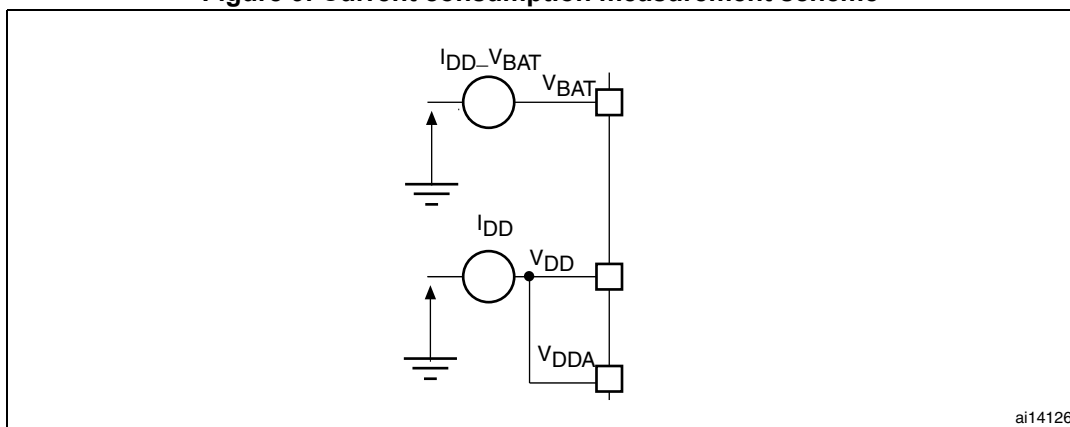
The loading conditions used for pin parameter measurement are shown in [Figure 6](#).

5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in [Figure 7](#).

5.1.7 Current consumption measurement

Figure 9. Current consumption measurement scheme



5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in [Table 5: Voltage characteristics](#), [Table 6: Current characteristics](#), and [Table 7: Thermal characteristics](#) may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 5. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
$V_{DD} - V_{SS}$	External main supply voltage (including V_{DDA} and V_{DD}) ⁽¹⁾	-0.3	4.0	V
V_{IN} ⁽²⁾	Input voltage on five volt tolerant pin	$V_{SS} - 0.3$	$V_{DD} + 4.0$	
	Input voltage on any other pin	$V_{SS} - 0.3$	4.0	
$ \Delta V_{DDx} $	Variations between different V_{DD} power pins	-	50	mV
$ V_{SSx} - V_{SS} $	Variations between all the different ground pins	-	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see Section 5.3.11: Absolute maximum ratings (electrical sensitivity)		

1. All main power (V_{DD} , V_{DDA}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to [Table 6: Current characteristics](#) for the maximum allowed injected current values.

5.3.3 Embedded reset and power control block characteristics

The parameters given in [Table 10](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 8](#).

Table 10. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection	PLS[2:0]=000 (rising edge)	2.1	2.18	2.26	V
		PLS[2:0]=000 (falling edge)	2.0	2.08	2.16	V
		PLS[2:0]=001 (rising edge)	2.19	2.28	2.37	V
		PLS[2:0]=001 (falling edge)	2.09	2.18	2.27	V
		PLS[2:0]=010 (rising edge)	2.28	2.38	2.48	V
		PLS[2:0]=010 (falling edge)	2.18	2.28	2.38	V
		PLS[2:0]=011 (rising edge)	2.38	2.48	2.58	V
		PLS[2:0]=011 (falling edge)	2.28	2.38	2.48	V
		PLS[2:0]=100 (rising edge)	2.47	2.58	2.69	V
		PLS[2:0]=100 (falling edge)	2.37	2.48	2.59	V
		PLS[2:0]=101 (rising edge)	2.57	2.68	2.79	V
		PLS[2:0]=101 (falling edge)	2.47	2.58	2.69	V
		PLS[2:0]=110 (rising edge)	2.66	2.78	2.9	V
		PLS[2:0]=110 (falling edge)	2.56	2.68	2.8	V
		PLS[2:0]=111 (rising edge)	2.76	2.88	3	V
		PLS[2:0]=111 (falling edge)	2.66	2.78	2.9	V
$V_{PVDhyst}^{(2)}$	PVD hysteresis	-	-	100	-	mV
$V_{POR/PDR}$	Power on/power down reset threshold	Falling edge	1.8 ⁽¹⁾	1.88	1.96	V
		Rising edge	1.84	1.92	2.0	V
$V_{PDRhyst}$	PDR hysteresis	-	-	40	-	mV
$t_{RSTTEMPO}^{(2)}$	Reset temporization	-	1.5	2.5	4.5	ms

1. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.

2. Guaranteed by design, not tested in production.

5.3.4 Embedded reference voltage

The parameters given in [Table 11](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 8](#).

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in [Table 18](#). The MCU is placed under the following conditions:

- all I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
 - with all peripherals clocked off
 - with only one peripheral clocked on
- ambient operating temperature and V_{DD} supply voltage conditions as summarized in [Table 5](#).

Table 18. Peripheral current consumption⁽¹⁾

Peripheral		$\mu A/MHz$
AHB (up to 48 MHz)	DMA1	15.97
	CRC	1.67
	BusMatrix ⁽²⁾	8.33
APB1 (up to 24 MHz)	APB1-Bridge	7.22
	TIM2	33.33
	TIM3	33.61
	USART2	12.78
	I2C1	10.83
	USB	16.94
	WWDG	3.33
	PWR	1.94
	BKP	2.78
	IWDG	1.39
APB2 (up to 48 MHz)	APB2-Bridge	3.33
	GPIOA	7.50
	GPIOB	6.81
	GPIOC	7.22
	GIPOD	6.94
	SPI1	4.86
	USART1	12.78
	ADC1 ^{(3) (4)}	15.54

1. $f_{HCLK} = 48\text{ MHz}$, $f_{APB1} = f_{HCLK}/2$, $f_{APB2} = f_{HCLK}$, default prescaler value for each peripheral.

2. The BusMatrix is automatically active when at least one master is ON.

3. Specific conditions for ADC: $f_{HCLK} = 48\text{ MHz}$, $f_{APB1} = f_{HCLK}/2$, $f_{APB2} = f_{HCLK}$, $f_{ADCCLK} = f_{APB2}/4$.

4. When ADON bit in the ADC_CR2 register is set to 1, there is an additional current consumption of 0,68 mA. When we enable the ADC, there is an additional current consumption of 0,06 mA.

Figure 16. High-speed external clock source AC timing diagram

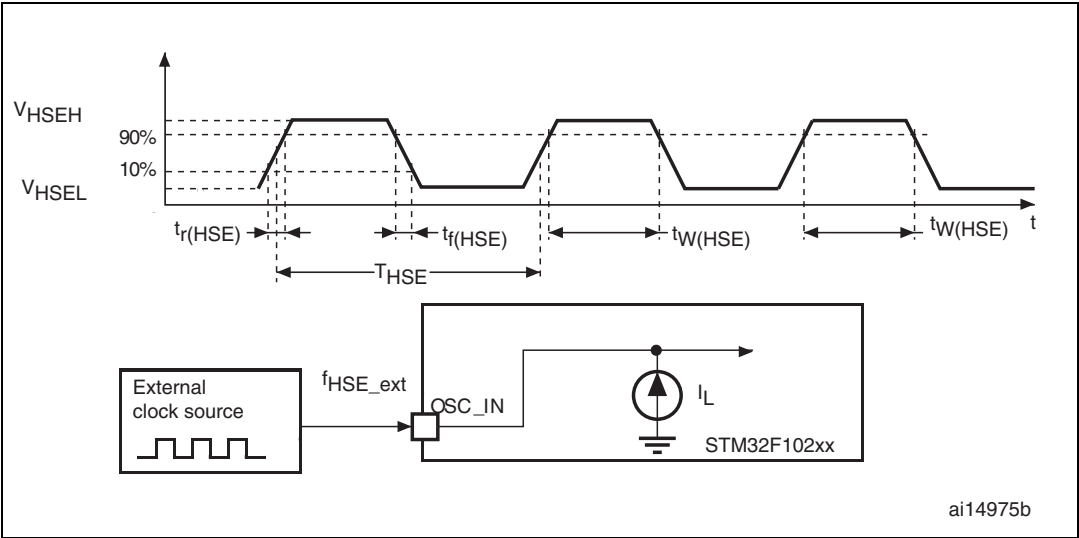
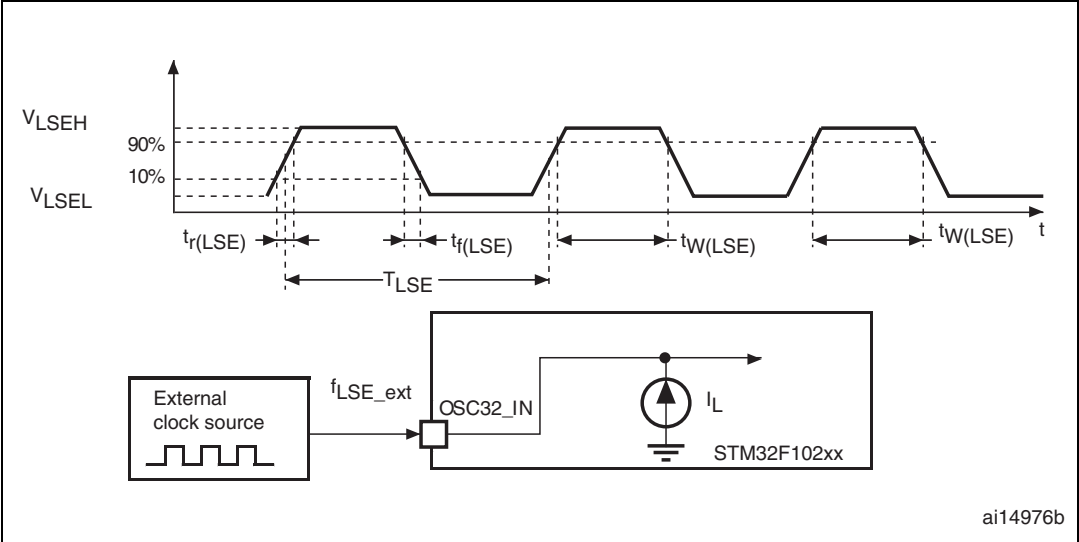


Figure 17. Low-speed external clock source AC timing diagram



2. Refer to application note AN2868 "STM32F10xxx internal RC oscillator (HSI) calibration" available from the ST website www.st.com.
3. Guaranteed by design, not tested in production.
4. Based on characterization, not tested in production.
5. The actual frequency of HSI oscillator may be impacted by a reflow, but does not drift out of the specified range.

Low-speed internal (LSI) RC oscillator

Table 24. LSI oscillator characteristics ⁽¹⁾

Symbol	Parameter	Min ⁽²⁾	Typ	Max	Unit
f_{LSI}	Frequency	30	40	60	kHz
$t_{su(LSI)}^{(3)}$	LSI oscillator startup time	-	-	85	μ s
$I_{DD(LSI)}^{(3)}$	LSI oscillator power consumption	-	0.65	1.2	μ A

1. $V_{DD} = 3$ V, $T_A = -40$ to 85 °C unless otherwise specified.
2. Based on characterization, not tested in production.
3. Guaranteed by design, not tested in production.

Wakeup time from low-power mode

The wakeup times given in [Table 25](#) is measured on a wakeup phase with a 8-MHz HSI RC oscillator. The clock source used to wake up the device depends from the current operating mode:

- Stop or Standby mode: the clock source is the RC oscillator
- Sleep mode: the clock source is the clock that was set before entering Sleep mode.

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 8](#).

Table 25. Low-power mode wakeup timings

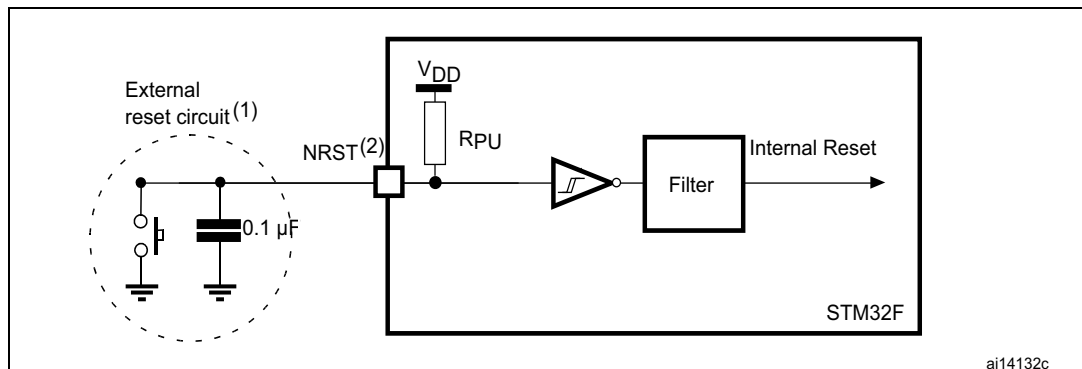
Symbol	Parameter	Typ	Unit
$t_{WUSLEEP}^{(1)}$	Wakeup from Sleep mode	1.8	μ s
$t_{WUSTOP}^{(1)}$	Wakeup from Stop mode (regulator in run mode)	3.6	μ s
	Wakeup from Stop mode (regulator in low-power mode)	5.4	
$t_{WUSTDBY}^{(1)}$	Wakeup from Standby mode	50	μ s

1. The wakeup times are measured from the wakeup event to the point at which the user application code reads the first instruction.

5.3.8 PLL characteristics

The parameters given in [Table 26](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 8](#).

Figure 25. Recommended NRST pin protection



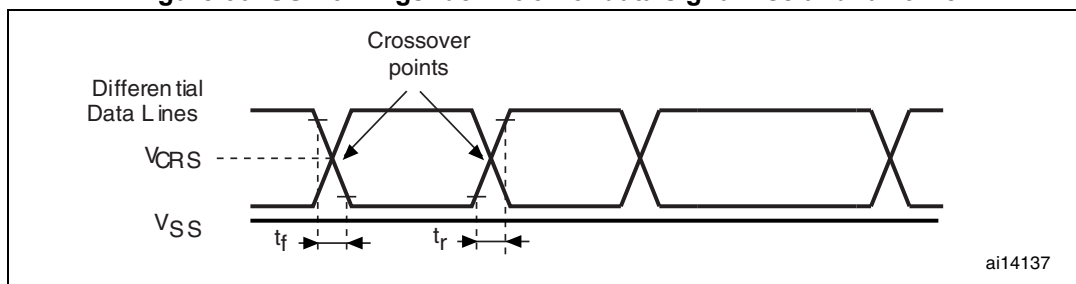
1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in [Table 39](#). Otherwise the reset will not be taken into account by the device.

Table 43. USB DC electrical characteristics

Symbol		Parameter	Conditions	Min. ⁽¹⁾	Max. ⁽¹⁾	Unit
Input levels	V _{DD}	USB operating voltage ⁽²⁾	-	3.0 ⁽³⁾	3.6	V
	V _{DI} ⁽⁴⁾	Differential input sensitivity	I(USB_DP, USB_DM)	0.2	-	V
	V _{CM} ⁽⁴⁾	Differential common mode range	Includes V _{DI} range	0.8	2.5	
	V _{SE} ⁽⁴⁾	Single ended receiver threshold	-	1.3	2.0	
Output levels	V _{OL}	Static output level low	R _L of 1.5 kΩ to 3.6 V ⁽⁵⁾	-	0.3	V
	V _{OH}	Static output level high	R _L of 15 kΩ to V _{SS} ⁽⁵⁾	2.8	3.6	

1. All the voltages are measured from the local ground potential.
2. To be compliant with the USB 2.0 full-speed electrical specification, the USB_DP (D+) pin should be pulled up with a 1.5 k Ω resistor to a 3.0-to-3.6 V voltage range.
3. The STM32F102xx USB functionality is ensured down to 2.7 V but not the full USB electrical characteristics which are degraded in the 2.7-to-3.0 V V_{DD} voltage range.
4. Guaranteed by design, not tested in production.
5. R_L is the load connected on the USB drivers

Figure 30. USB timings: definition of data signal rise and fall time

Table 44. USB: Full speed electrical characteristics of the driver⁽¹⁾

Symbol	Parameter	Conditions	Min	Max	Unit
t_r	Rise time ⁽²⁾	$C_L = 50$ pF	4	20	ns
t_f	Fall time ⁽²⁾	$C_L = 50$ pF	4	20	ns
t_{rfm}	Rise/ fall time matching	t_r / t_f	90	110	%
V_{CRS}	Output signal crossover voltage	-	1.3	2.0	V

1. Guaranteed by design, not tested in production.
2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).

5.3.17 12-bit ADC characteristics

Unless otherwise specified, the parameters given in [Table 45](#) are derived from tests performed under ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in [Table 8](#).

Note: *It is recommended to perform a calibration after each power-up.*

Table 46. R_{AIN} max for $f_{ADC} = 12 \text{ MHz}^{(1)}$

T_s (cycles)	t_s (μs)	R_{AIN} max ($k\Omega$)
1.5	0.13	0.4
7.5	0.63	5.9
13.5	1.13	11.4
28.5	2.38	25.2
41.5	3.46	37.2
55.5	4.63	50
71.5	5.96	NA
239.5	19.96	NA

1. Data guaranteed by design, not tested in production.

Table 47. ADC accuracy - limited test conditions⁽¹⁾

Symbol	Parameter	Test conditions	Typ	Max ⁽²⁾	Unit
ET	Total unadjusted error	$f_{PCLK2} = 48 \text{ MHz}$. $f_{ADC} = 12 \text{ MHz}$, $R_{AIN} < 10 \text{ k}\Omega$ $V_{DDA} = 3 \text{ V to } 3.6 \text{ V}$ $T_A = 25^\circ\text{C}$ Measurements made after ADC calibration	± 1.3	± 2	LSB
EO	Offset error		± 1	± 1.5	
EG	Gain error		± 0.5	± 1.5	
ED	Differential linearity error		± 0.7	± 1	
EL	Integral linearity error		± 0.8	± 1.5	

1. ADC DC accuracy values are measured after internal calibration.

2. Based on characterization, not tested in production.

Table 48. ADC accuracy^{(1) (2) (3)}

Symbol	Parameter	Test conditions	Typ	Max ⁽⁴⁾	Unit
ET	Total unadjusted error	$f_{PCLK2} = 48 \text{ MHz}$. $f_{ADC} = 12 \text{ MHz}$, $R_{AIN} < 10 \text{ k}\Omega$ $V_{DDA} = 2.4 \text{ V to } 3.6 \text{ V}$ Measurements made after ADC calibration	± 2	± 5	LSB
EO	Offset error		± 1.5	± 2.5	
EG	Gain error		± 1.5	± 3	
ED	Differential linearity error		± 1	± 2	
EL	Integral linearity error		± 1.5	± 3	

1. ADC DC accuracy values are measured after internal calibration.

2. Better performance could be achieved in restricted V_{DD} , frequency and temperature ranges.

3. ADC accuracy vs. negative injection current: Injecting a negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in [Section 5.3.13](#) does not affect the ADC accuracy.

4. Based on characterization, not tested in production.

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