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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	51
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f102r4t6a

List of tables

List of figures

1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of STM32F102x4 and STM32F102x6 low-density USB access line microcontrollers. For more details on the whole STMicroelectronics STM32F102xx family. please refer to *Section 2.2: Full compatibility throughout the family*.

The medium-density STM32F102xx datasheet should be read in conjunction with the low-, medium- and high-density STM32F10xxx reference manual.

For information on programming, erasing and protection of the internal Flash memory please refer to the *STM32F10xxx Flash programming manual.*

The reference and Flash programming manuals are both available from the STMicroelectronics website *www.st.com*.

For information on the Cortex®-M3 core please refer to the Cortex®-M3 Technical Reference Manual, available from the ARM® website.

2.1 Device overview

Table 2. STM32F102x4 and STM32F102x6 low-density USB access line features and peripheral counts

Peripheral		STM32F102Cx		STM32F102Rx	
Flash - Kbytes		16	32	16	32
SRAM - Kbytes		4	6	4	6
Timers	General-purpose	2	2	2	2
Communication interfaces	SPI	1	1	1	1
	I^2C	1	1	1	1
	USART	2	2	2	2
	USB	1	1	1	1
12-bit synchronized ADC number of channels		1 10 channels		1 16 channels	
GPIOs		37		51	
CPU frequency		48 MHz			
Operating voltage		2.0 to 3.6 V			
Operating temperatures		Ambient temperature: –40 to +85 °C (see *Table 8*) Junction temperature: –40 to +105 °C (see *Table 8*)			
Packages		LQFP48		LQFP64	

2.2 Full compatibility throughout the family

The STM32F102xx is a complete family whose members are fully pin-to-pin, software and feature compatible. In the reference manual, the STM32F102x4 and STM32F102x6 are referred to as low-density devices and the STM32F102x8 and STM32F102xB are referred to as medium-density devices.

Low-density devices are an extension of the STM32F102x8/B devices, they are specified in the STM32F102x4/6 datasheet. Low-density devices feature lower Flash memory and RAM capacities, a timer and a few communication interfaces less.
The STM32F102x4 and STM32F102x6 are a drop-in replacement for the STM32F102x8/B medium-density devices, allowing the user to try different memory densities and providing a greater degree of freedom during the development cycle.

Moreover the STM32F102xx family is fully compatible with all existing STM32F101xx access line and STM32F103xx performance line devices.

Table 3. STM32F102xx USB access line family

Pinout	Low-density STM32F102xx devices		Medium-density STM32F102xx devices	
	16 KB Flash	32 KB Flash(1)	64 KB Flash	128 KB Flash
	4 KB RAM	6 KB RAM	10 KB RAM	16 KB RAM
64 48	2 × USARTs, 2 × 16-bit timers 1 × SPI, 1 × I^2C, 1 × ADC, 1 × USB		3 × USARTs, 3 × 16-bit timers 2 × SPIs, 2 × I2Cs, 1 × ADC, 1 × USB	
36	-	-	2 × USARTs, 3 × 16-bit timers 1× SPI, 1× I2C, 1 × ADC, 1 × USB	-

1. For orderable part numbers that do not show the A internal code after the temperature range code (6), the reference datasheet for electrical characteristics is that of the STM32F102x8/B medium-density devices.

2.3 Overview

ARM® Cortex®-M3 core with embedded Flash and SRAM

The ARM® Cortex®-M3 processor is the latest generation of ARM® processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM® Cortex®-M3 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM® core in the memory size usually associated with 8- and 16-bit devices.

The STM32F102xx medium-density USB access line having an embedded ARM® core is therefore compatible with all ARM® tools and software.

Embedded Flash memory

16 or 32 Kbytes of embedded Flash is available for storing programs and data.

Table 4. Low-density STM32F102xx pin definitions

Pins		Pin name	Type[1]	I / O level[2]	Main function[3] (after reset)	Alternate functions[3] [4]	
LQFP48	LQFP64					Default	Remap
1	1	V_{BAT}	S	-	V_{BAT}	-	-
2	2	PC13-TAMPER-RTC[5]	I/O	-	PC13[6]	TAMPER-RTC	-
3	3	PC14-OSC32_IN[5]	I/O	-	PC14[6]	OSC32_IN	-
4	4	PC15-OSC32_OUT[5]	I/O	-	PC15[6]	OSC32_OUT	-
5	5	OSC_IN	I/O	FT	OSC_IN	-	PD0[7]
6	6	OSC_OUT	I/O	FT	OSC_OUT	-	PD1[7]
7	7	NRST	I/O	-	NRST	-	-
-	8	PC0	I/O	-	PC0	ADC_IN10	-
-	9	PC1	I/O	-	PC1	ADC_IN11	-
-	10	PC2	I/O	-	PC2	ADC_IN12	-
-	11	PC3	I/O	-	PC3	ADC_IN13	-
8	12	V_{SSA}	S	-	V_{SSA}	-	-
9	13	V_{DDA}	S	-	V_{DDA}	-	-
10	14	PA0-WKUP	I/O	-	PA0	WKUP/USART2_CTS/ ADC_IN0/ TIM2_CH1_ETR[8]	-
11	15	PA1	I/O	-	PA1	USART2_RTS/ ADC_IN1/TIM2_CH2[8]	-
12	16	PA2	I/O	-	PA2	USART2_TX/ ADC_IN2/TIM2_CH3[8]	-
13	17	PA3	I/O	-	PA3	USART2_RX/ ADC_IN3/TIM2_CH4[8]	-
-	18	V_{SS_4}	S	-	V_{SS_4}	-	-
-	19	V_{DD_4}	S	-	V_{DD_4}	-	-
14	20	PA4	I/O	-	PA4	SPI_NSS[8]/ADC_IN4 USART2_CK/	-
15	21	PA5	I/O	-	PA5	SPI_SCK[8]/ADC_IN5	-
16	22	PA6	I/O	-	PA6	SPI_MISO[8]/ADC_IN6/ TIM3_CH1[8]	-
17	23	PA7	I/O	-	PA7	SPI_MOSI[8]/ADC_IN7/ TIM3_CH2[8]	-
-	24	PC4	I/O	-	PC4	ADC_IN14	-
-	25	PC5	I/O	-	PC5	ADC_IN15	-
18	26	PB0	I/O	-	PB0	ADC_IN8/TIM3_CH3[8]	-
19	27	PB1	I/O	-	PB1	ADC_IN9/TIM3_CH4[8]	-

Table 6. Current characteristics

Symbol	Ratings	Max.	Unit
I_{VDD}	Total current into V_{DD}/V_{DDA} power lines (source)(1)	150	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)(1)	150	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current source by any I/Os and control pin	-25	
$I_{INJ(PIN)}$ (2)	Injected current five volt tolerant pins(3)	-5/+0	
	Injected current on any other pin(4)	± 5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(5)	± 25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. Negative injection disturbs the analog performance of the device.
3. Positive injection is not possible on these I/Os. A negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 5* for maximum allowed input voltage values.
4. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 5* for maximum allowed input voltage values.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 7. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

Table 11. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +85 °C	1.16	1.20	1.24	V
$T_{S\_vrefint}$(1)	ADC sampling time when reading the internal reference voltage	-	-	5.1	17.1(2)	µs
V_{RERINT}(2)	Internal reference voltage spread over the temperature range	V_{DD} = 3 V ±10 mV	-	-	10	mV
T_{Coeff}(2)	Temperature coefficient	-	-	-	100	ppm/ °C

1. Shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design, not tested in production.

5.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.
The current consumption is measured as described in *Figure 9: Current consumption measurement scheme*.
All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to Dhrystone 2.1 code.

Maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except if it is explicitly mentioned
- The Flash access time is adjusted to f_{HCLK} frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz)
- Prefetch in on (reminder: this bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled $f_{PCLK1} = f_{HCLK/2}$, $f_{PCLK2} = f_{HCLK}$

The parameters given in *Table 12* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

Table 14. Maximum current consumption in Sleep mode, code running from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Max(1)	Unit
				T_A = 85 °C	
I_{DD}	Supply current in Sleep mode	External clock(2), all peripherals enabled	48 MHz	17	mA
			36 MHz	14	
			24 MHz	10	
			16 MHz	7	
			8 MHz	4	
		External clock(2), all peripherals disabled	48 MHz	6	
			36 MHz	5	
			24 MHz	4.5	
			16 MHz	4	
			8 MHz	3	

1. Based on characterization, tested in production at V_{DD} max and f_{HCLK} max with peripherals enabled.
2. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Table 15. Typical and maximum current consumptions in Stop and Standby modes

Symbol	Parameter	Conditions	Typ(1)			Max	Unit
			V_{DD}/ V_{BAT} = 2.4 V	V_{DD}/V_{BAT} = 3.3 V	V_{DD}/V_{BAT} = 2.0 V	T_A = 85 °C	
I_{DD}	Supply current in Stop mode	Regulator in Run mode. Low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	21.3	21.7	-	160	µA
		Regulator in Low Power mode. Low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	11.3	11.7	-	145	
	Supply current in Standby mode(2)	Low-speed internal RC oscillator and independent watchdog ON	2.75	3.4	-	-	
		Low-speed internal RC oscillator ON, independent watchdog OFF	2.55	3.2	-	-	
		Low-speed internal RC oscillator and independent watchdog OFF, low-speed oscillator and RTC OFF	1.55	1.9	-	3.2	
I_{DD_VBAT}	Backup domain supply current	Low-speed oscillator and RTC ON	1.1	1.4	0.9	1.9(3)	

1. Typical values are measured at T_A = 25 °C.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 18*. The MCU is placed under the following conditions:

- all I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- ambient operating temperature and V_{DD} supply voltage conditions as summarized in *Table 5*.

Table 18. Peripheral current consumption(1)

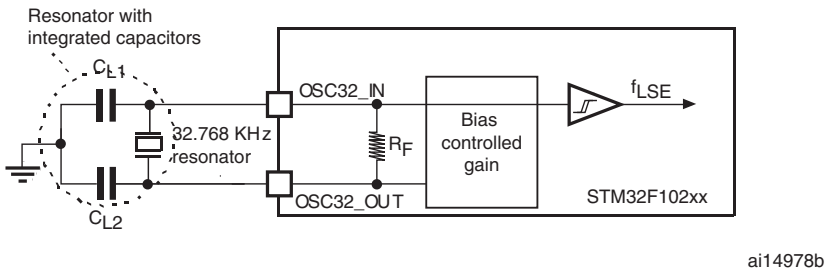
Peripheral		µA/MHz
AHB (up to 48 MHz)	DMA1	15.97
	CRC	1.67
	BusMatrix(2)	8.33
APB1 (up to 24 MHz)	APB1-Bridge	7.22
	TIM2	33.33
	TIM3	33.61
	USART2	12.78
	I2C1	10.83
	USB	16.94
	WWDG	3.33
	PWR	1.94
	BKP	2.78
	IWDG	1.39
APB2 (up to 48 MHz)	APB2-Bridge	3.33
	GPIOA	7.50
	GPIOB	6.81
	GPIOC	7.22
	GPIOD	6.94
	SPI1	4.86
	USART1	12.78
	ADC1(3) (4)	15.54

1. f_{HCLK} = 48 MHz, $f_{APB1} = f_{HCLK}/2$, $f_{APB2} = f_{HCLK}$, default prescaler value for each peripheral.
2. The BusMatrix is automatically active when at least one master is ON.
3. Specific conditions for ADC: f_{HCLK} = 48 MHz, $f_{APB1} = f_{HCLK}/2$, $f_{APB2} = f_{HCLK}$, $f_{ADCCLK} = f_{APB2}/4$.
4. When ADON bit in the ADC_CR2 register is set to 1, there is an additional current consumption of 0, 68 mA. When we enable the ADC, there is an additional current consumption of 0, 06 mA.

Note: For CL1 and CL2 it is recommended to use high-quality ceramic capacitors in the 5 pF to 15 pF range selected to match the requirements of the crystal or resonator. CL1 and CL2 are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of CL1 and CL2.
Load capacitance CL has the following formula: CL = CL1 x CL2 / (CL1 + CL2) + C_{stray} where C_{stray} is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF.

Caution: To avoid exceeding the maximum value of CL1 and CL2 (15 pF) it is strongly recommended to use a resonator with a load capacitance CL ≤7 pF. Never use a resonator with a load capacitance of 12.5 pF.
Example: if you choose a resonator with a load capacitance of CL = 6 pF, and Cstray = 2 pF, then CL1 = CL2 = 8 pF.

Figure 19. Typical application with a 32.768 kHz crystal



5.3.7 Internal clock source characteristics

The parameters given in *Table 23* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

High-speed internal (HSI) RC oscillator

Table 23. HSI oscillator characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{HSI}	Frequency	-		-	8	-	MHz
$DuCy_{(HSI)}$	Duty cycle	-		45	-	55	%
ACC_{HSI}	Accuracy of the HSI oscillator	User-trimmed with the RCC_CR register(2)		-	-	1(3)	%
		Factory-calibrated(4)(5)	T_A = –40 to 105 °C	–2.0	-	2.5	%
			T_A = –10 to 85 °C	–1.5	-	2.2	%
			T_A = 0 to 70 °C	–1.3	-	2	%
			T_A = 25 °C	–1.1	-	1.8	%
$t_{su(HSI)}$(4)	HSI oscillator startup time	-		1	-	2	µs
$I_{DD(HSI)}$(4)	HSI oscillator power consumption	-		-	80	100	µA

1. V_{DD} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.

5.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (Electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports), the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 29*. They are based on the EMS levels and classes defined in application note AN1709.

Table 29. EMS characteristics

Symbol	Parameter	Conditions	Level/Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK}= 48 MHz conforms to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK} = 48 MHz conforms to IEC 61000-4-4	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and pre qualification tests in relation with the EMC level requested for his application.

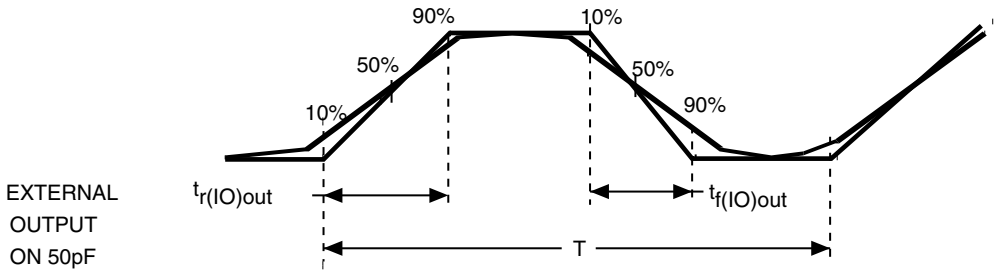
Software recommendations: the software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers, etc.)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second. To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Figure 24. I/O AC characteristics definition



Maximum frequency is achieved if $(t_r + t_f) \leq 2/3)T$ and if the duty cycle is (45-55%)
when loaded by 50pF

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5.3.14 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 34*).

Unless otherwise specified, the parameters given in *Table 37* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

Table 37. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST Input low level voltage	-	–0.5	-	0.8	V
$V_{IH(NRST)}$(1)	NRST Input high level voltage	-	2	-	V_{DD}+0.5	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	30	40	50	kΩ
$V_{F(NRST)}$(1)	NRST Input filtered pulse	-	-	-	100	ns
$V_{NF(NRST)}$(1)	NRST Input not filtered pulse	-	300	-	-	ns

1. Guaranteed by design, not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

Table 39. I^2C characteristics

Symbol	Parameter	Standard mode I^2C(1)(2)		Fast mode I^2C(1)(2)		Unit
		Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	-	3450(3)	-	900(3)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	-	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	
$t_{h(STA)}$	Start condition hold time	4.0	-	0.6	-	µs
$t_{su(STA)}$	Repeated Start condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	Stop condition setup time	4.0	-	0.6	-	µs
$t_{w(STO:STA)}$	Stop to Start condition time (bus free)	4.7	-	1.3	-	µs
t_{SP}	Pulse width of spikes that are suppressed by the analog filter	0	50(4)	0	50(4)	ns
C_b	Capacitive load for each bus line	-	400	-	400	pF

1. Values guaranteed by design, not tested in production.
2. f_{PCLK1} must be at least 2 MHz to achieve standard mode I^2C frequencies. It must be at least 4 MHz to achieve fast mode I^2C frequencies. It must be a multiple of 10 MHz to reach the 400 kHz maximum I2C fast mode clock.
3. The maximum Data hold time has only to be met if the interface does not stretch the low period of the SCL signal.
4. The analog filter minimum filtered spikes is above $t_{SP(max)}$ to ensure that spikes width up to $t_{SP(max)}$ are filtered.

Table 43. USB DC electrical characteristics

Symbol		Parameter	Conditions	Min.(1)	Max.(1)	Unit
Input levels	V_{DD}	USB operating voltage(2)	-	3.0(3)	3.6	V
	V_{DI}(4)	Differential input sensitivity	I(USB_DP, USB_DM)	0.2	-	V
	V_{CM}(4)	Differential common mode range	Includes V_{DI} range	0.8	2.5	
	V_{SE}(4)	Single ended receiver threshold	-	1.3	2.0	
Output levels	V_{OL}	Static output level low	R_L of 1.5 kΩ to 3.6 V(5)	-	0.3	V
	V_{OH}	Static output level high	R_L of 15 kΩ to V_{SS}(5)	2.8	3.6	

1. All the voltages are measured from the local ground potential.
2. To be compliant with the USB 2.0 full-speed electrical specification, the USB_DP (D+) pin should be pulled up with a 1.5 kΩ resistor to a 3.0-to-3.6 V voltage range.
3. The STM32F102xx USB functionality is ensured down to 2.7 V but not the full USB electrical characteristics which are degraded in the 2.7-to-3.0 V V_{DD} voltage range.
4. Guaranteed by design, not tested in production.
5. R_L is the load connected on the USB drivers

Figure 30. USB timings: definition of data signal rise and fall time

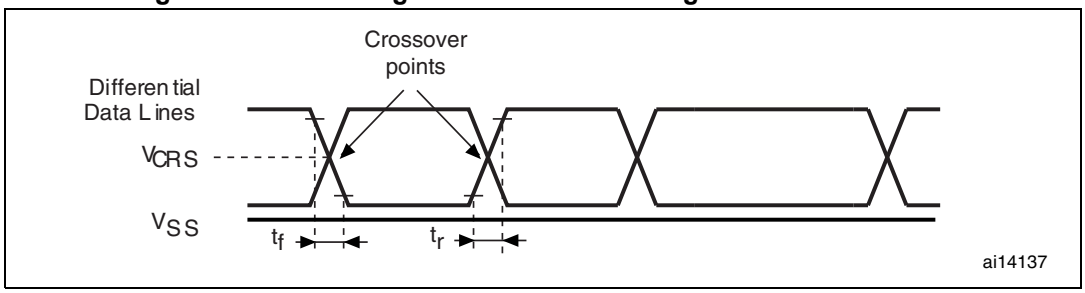


Table 44. USB: Full speed electrical characteristics of the driver(1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_r	Rise time(2)	C_L = 50 pF	4	20	ns
t_f	Fall time(2)	C_L = 50 pF	4	20	ns
t_{rfm}	Rise/ fall time matching	t_r / t_f	90	110	%
V_{CRS}	Output signal crossover voltage	-	1.3	2.0	V

1. Guaranteed by design, not tested in production.
2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).

5.3.17 12-bit ADC characteristics

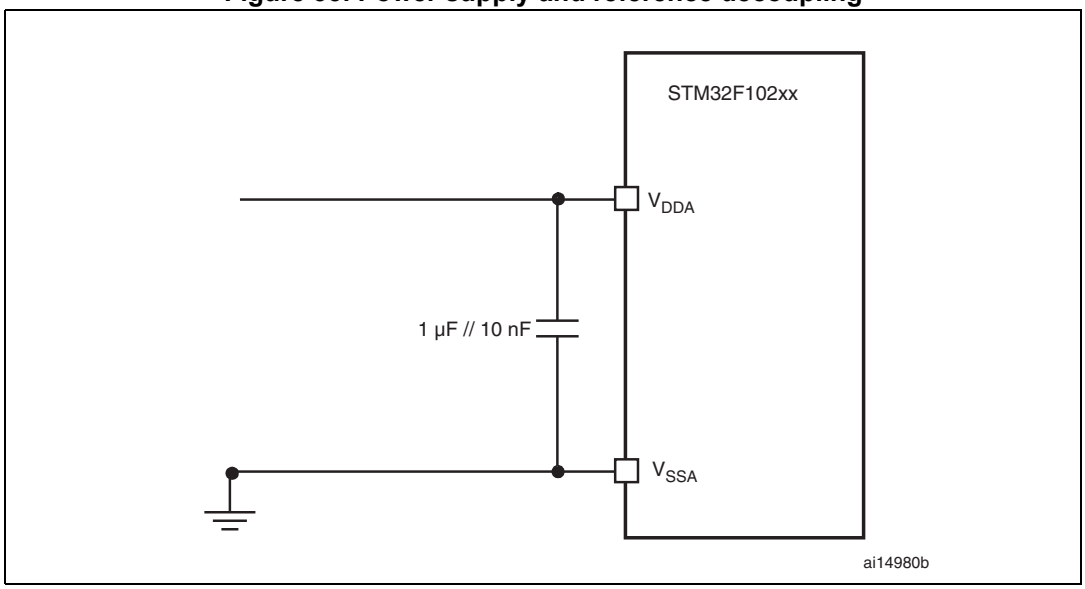
Unless otherwise specified, the parameters given in *Table 45* are derived from tests performed under ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 8*.

Note: It is recommended to perform a calibration after each power-up.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 33*. The 10 nF capacitors should be ceramic (good quality). They should be placed as close as possible to the chip.

Figure 33. Power supply and reference decoupling



5.3.18 Temperature sensor characteristics

Table 49. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	±1.5	-	°C
Avg_Slope(1)	Average slope	-	4.35	-	mV/°C
V_{25}(1)	Voltage at 25°C	-	1.42	-	V
t_{START}(2)	Startup time	4	-	10	µs
T_{S_temp}(3)(2)	ADC sampling time when reading the temperature	-	-	17.1	µs

1. Guaranteed by characterization, not tested in production.
2. Data guaranteed by design, not tested in production.
3. Shortest sampling time can be determined in the application by multiple iterations.

Table 51. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

7 Ordering information scheme

Table 53. Ordering information scheme

Example: STM32 F 102 C 6 T 6 A xxx

Device family

STM32 = ARM®-based 32-bit microcontroller

Product type

F = general-purpose

Device subfamily

102 = USB access line, USB 2.0 full-speed interface

Pin count

C = 48 pins

R = 64 pins

Flash memory size

4 = 16 Kbytes of Flash memory

6 = 32 Kbytes of Flash memory

Package

T = LQFP

Temperature range

6 = Industrial temperature range, –40 to 85 °C.

Internal code

“A” or blank(1)

Options

xxx = programmed parts

TR = tape and reel

1. For STM32F102x6 devices with a **blank** Internal code, please refer to the STM32F103x8/B datasheet available from the ST website: *www.st.com*.

Table 54. Document revision history (continued)

Date	Revision	Changes
02-Aug-2013	4	*Figure 2: Clock tree*: added FLITFCLK and *Note 3.*, and modified *Note 1.*. Removed sentence in “Unless otherwise specified the parameters ...” in *I2C interface characteristics* section. Added V_{IN} in *Table 8: General operating conditions*. Added note *5* in *Table 23: HSI oscillator characteristics* Added $DuCy_{(HSI)}$ in *Table 23: HSI oscillator characteristics* *Table 24: LSI oscillator characteristics*: removed note 2 related to oscillator selection, updated *Note 2.*, and $t_{SU(LSE)}$ specified for various ambient temperature values. Modified charge device model in *Table 33: I/O current injection susceptibility*. Updated ‘V_{IL}’ and ‘V_{IH}’ in *Table 34: I/O static characteristics*. Added notes to *Figure 20: Standard I/O input characteristics - CMOS port*, *Figure 21: Standard I/O input characteristics - TTL port*, *Figure 22: 5 V tolerant I/O input characteristics - CMOS port* and *Figure 23: 5 V tolerant I/O input characteristics - TTL port* *Table 37: Output voltage characteristics*: updated V_{OL} and V_{OH} conditions for TTL and CMOS outputs and added *Note 2.* Updated *Figure 24: I/O AC characteristics definition* Updated *Figure 25: Recommended NRST pin protection* Updated note *2.* and *3.* in *Table 39: I^2C characteristics* Updated *Figure 26: I2C bus AC waveforms and measurement circuit(1)* Updated title of *Table 40: SCL frequency (f_{PCLK1}= 36 MHz, V_{DD_I2C} = 3.3 V)* In *Table 43: SPI characteristics*, removed note 1 related to SPI1 remapped characteristics. Updated *Table 47: ADC characteristics* Updated *Section 6.1: Package mechanical data*
14-May-2015	5	Updated *Table 18: Peripheral current consumption* and *Table 39: I2C characteristics*. Updated *Section 6: Package characteristics*. Updated *Section 6.1: LQFP64 package information* with addition of *Device marking for LQFP64* and *Figure 36*. Updated *Section 6.2: LQFP48 package information* with addition of *Device marking for LQFP48* and *Figure 39*. Updated Disclaimer.