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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	51
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f102r6t6a

1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of STM32F102x4 and STM32F102x6 low-density USB access line microcontrollers. For more details on the whole STMicroelectronics STM32F102xx family. please refer to *Section 2.2: Full compatibility throughout the family*.

The medium-density STM32F102xx datasheet should be read in conjunction with the low-, medium- and high-density STM32F10xxx reference manual.

For information on programming, erasing and protection of the internal Flash memory please refer to the *STM32F10xxx Flash programming manual.*

The reference and Flash programming manuals are both available from the STMicroelectronics website *www.st.com*.

For information on the Cortex®-M3 core please refer to the Cortex®-M3 Technical Reference Manual, available from the ARM® website.

2 Description

The STM32F102xx medium-density USB access line incorporates the high-performance ARM® Cortex®-M3 32-bit RISC core operating at a 48 MHz frequency, high-speed embedded memories (Flash memory of 16 or 32 Kbytes and SRAM of 4 or 6 Kbytes), and an extensive range of enhanced peripherals and I/Os connected to two APB buses. All devices offer standard communication interfaces (one I^2C, one SPI, one USB and two USARTs), one 12-bit ADC and two general-purpose 16-bit timers.

The STM32F102xx family operates in the –40 to +85 °C temperature range, from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power applications.

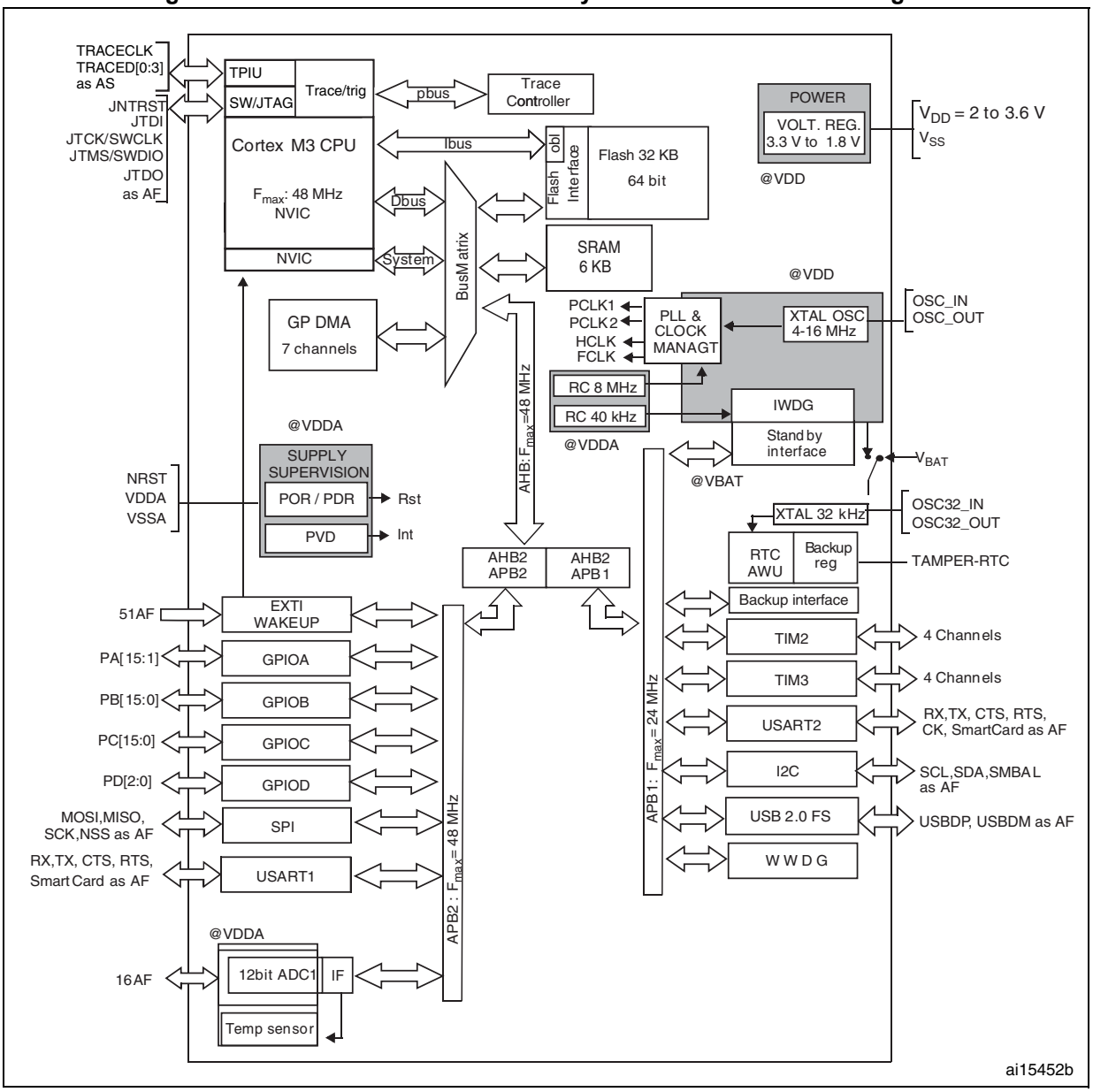
The STM32F102xx medium-density USB access line is delivered in the LQFP48 7 × 7 mm and LQFP64 10 × 10 mm packages.

The STM32F102xx medium-density USB access line microcontrollers are suitable for a wide range of applications.

- Application control and user interface
- Medical and handheld equipment
- PC peripherals, gaming and GPS platforms
- Industrial applications: PLC, inverters, printers, and scanners
- Alarm systems, Video intercom, and HVAC

Figure 1 shows the general block diagram of the device family.

Figure 1. STM32F102T8 medium-density USB access line block diagram



1. AF = alternate function on I/O port pin.
2. T_A = –40 °C to +85 °C (junction temperature up to 105 °C).

Table 4. Low-density STM32F102xx pin definitions (continued)

Pins		Pin name	Type(1)	I / O level(2)	Main function(3) (after reset)	Alternate functions(3) (4)	
LQFP48	LQFP64					Default	Remap
20	28	PB2	I/O	FT	PB2/BOOT1	-	-
21	29	PB10	I/O	FT	PB10	(8)	TIM2_CH3
22	30	PB11	I/O	FT	PB11	(8)	TIM2_CH4
23	31	V_{SS_1}	S	-	V_{SS_1}	-	-
24	32	V_{DD_1}	S	-	V_{DD_1}	-	-
25	33	PB12	I/O	FT	PB12	(8)	-
26	34	PB13	I/O	FT	PB13	-	-
27	35	PB14	I/O	FT	PB14	-	-
28	36	PB15	I/O	FT	PB15	-	-
-	37	PC6	I/O	FT	PC6	-	TIM3_CH1
-	38	PC7	I/O	FT	PC7	-	TIM3_CH2
-	39	PC8	I/O	FT	PC8	-	TIM3_CH3
-	40	PC9	I/O	FT	PC9	-	TIM3_CH4
29	41	PA8	I/O	FT	PA8	USART1_CK/MCO	-
30	42	PA9	I/O	FT	PA9	USART1_TX(8)	-
31	43	PA10	I/O	FT	PA10	USART1_RX(8)	-
32	44	PA11	I/O	FT	PA11	USART1_CTS/USB_DM	-
33	45	PA12	I/O	FT	PA12	USART1_RTS/USB_DP	-
34	46	PA13	I/O	FT	JTMS-SWDIO	-	PA13
35	47	V_{SS_2}	S	-	V_{SS_2}	-	-
36	48	V_{DD_2}	S	-	V_{DD_2}	-	-
37	49	PA14	I/O	FT	JTCK/ SWCLK	-	PA14
38	50	PA15	I/O	FT	JTDI	-	TIM2_CH1_ETR / PA15 /SPI_NSS
-	51	PC10	I/O	FT	PC10	-	-
-	52	PC11	I/O	FT	PC11	-	-
-	53	PC12	I/O	FT	PC12	-	-
-	54	PD2	I/O	FT	PD2	-	-
39	55	PB3	I/O	FT	JTDO	-	TIM2_CH2/ PB3/ TRACESWO/ SPI_SCK

Table 4. Low-density STM32F102xx pin definitions (continued)

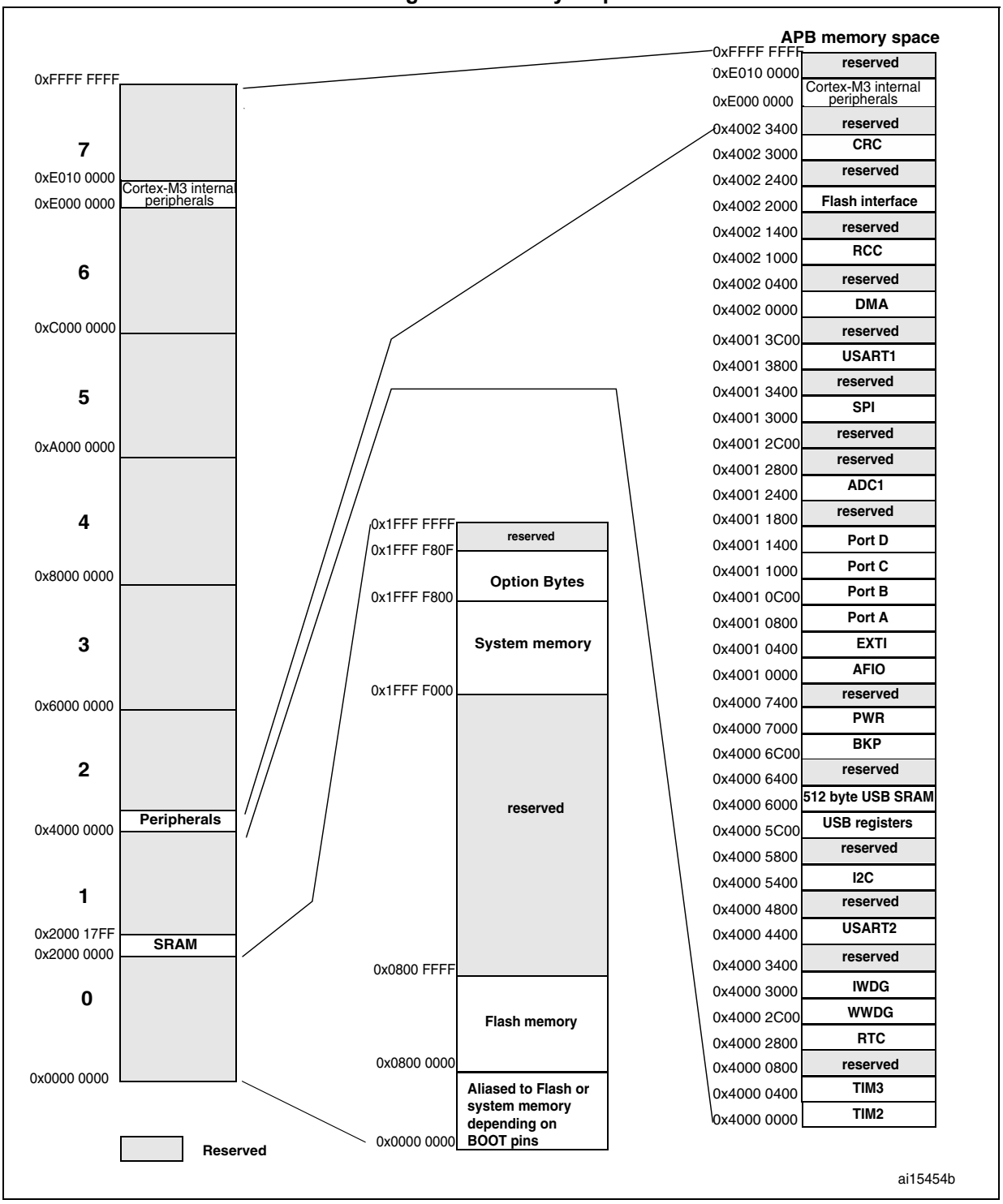
Pins		Pin name	Type(1)	I / O level(2)	Main function(3) (after reset)	Alternate functions(3) (4)	
LQFP48	LQFP64					Default	Remap
40	56	PB4	I/O	FT	JNTRST	-	TIM3_CH1 / PB4 SPI_MISO
41	57	PB5	I/O	-	PB5	I2C_SMBA	TIM3_CH2 / SPI_MOSI
42	58	PB6	I/O	FT	PB6	I2C_SCL(8)	USART1_TX
43	59	PB7	I/O	FT	PB7	I2C_SDA(8)	USART1_RX
44	60	BOOT0	I	-	BOOT0	-	-
45	61	PB8	I/O	FT	PB8	-	I2C_SCL
46	62	PB9	I/O	FT	PB9	-	I2C_SDA
47	63	V_{SS_3}	S	-	V_{SS_3}	-	-
48	64	V_{DD_3}	S	-	V_{DD_3}	-	-

1. I = input, O = output, S = supply.
2. FT= 5 V tolerant.
3. Function availability depends on the chosen device. For devices having reduced peripheral counts, it is always the lower number of peripherals that is included. For example, if a device has only one SPI, two USARTs and two timers, they will be called SPI1, USART1 & USART2 and TIM2 & TIM 3, respectively. Refer to *Table 3 on page 12*.
4. If several peripherals share the same I/O pin, to avoid conflict between these alternate functions only one peripheral should be enabled at a time through the peripheral clock enable bit (in the corresponding RCC peripheral clock enable register).
5. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited: the speed should not exceed 2 MHz with a maximum load of 30 pF and these IOs must not be used as a current source (e.g. to drive an LED).
6. Main function after the first backup domain power-up. Later on, it depends on the contents of the Backup registers even after reset (because these registers are not reset by the main reset). For details on how to manage these IOs, refer to the Battery backup domain and BKP register description sections in the STM32F102xx reference manual, available from the STMicroelectronics website: www.st.com.
7. The pins number 5 and 6 in the LQFP48 package are configured as OSC_IN/OSC_OUT after reset, however the functionality of PD0 and PD1 can be remapped by software on these pins. For more details, refer to the Alternate function I/O and debug configuration section in the STM32F10xxx reference manual.
   The use of PD0 and PD1 in output mode is limited as they can only be used at 50 MHz in output mode.
8. This alternate function can be remapped by software to some other port pins (if available on the used package). For more details, refer to the Alternate function I/O and debug configuration section in the STM32F10xxx reference manual, available from the STMicroelectronics website: www.st.com.

4 Memory mapping

The memory map is shown in *Figure 5*.

Figure 5. Memory map



5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}.

5.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3σ).

5.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.3 V (for the 2 V $\leq V_{DD} \leq$ 3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 6*.

5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 7*.

5.3.3 Embedded reset and power control block characteristics

The parameters given in *Table 10* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

Table 10. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection	PLS[2:0]=000 (rising edge)	2.1	2.18	2.26	V
		PLS[2:0]=000 (falling edge)	2.0	2.08	2.16	V
		PLS[2:0]=001 (rising edge)	2.19	2.28	2.37	V
		PLS[2:0]=001 (falling edge)	2.09	2.18	2.27	V
		PLS[2:0]=010 (rising edge)	2.28	2.38	2.48	V
		PLS[2:0]=010 (falling edge)	2.18	2.28	2.38	V
		PLS[2:0]=011 (rising edge)	2.38	2.48	2.58	V
		PLS[2:0]=011 (falling edge)	2.28	2.38	2.48	V
		PLS[2:0]=100 (rising edge)	2.47	2.58	2.69	V
		PLS[2:0]=100 (falling edge)	2.37	2.48	2.59	V
		PLS[2:0]=101 (rising edge)	2.57	2.68	2.79	V
		PLS[2:0]=101 (falling edge)	2.47	2.58	2.69	V
		PLS[2:0]=110 (rising edge)	2.66	2.78	2.9	V
		PLS[2:0]=110 (falling edge)	2.56	2.68	2.8	V
		PLS[2:0]=111 (rising edge)	2.76	2.88	3	V
		PLS[2:0]=111 (falling edge)	2.66	2.78	2.9	V
$V_{PVDhyst}$(2)	PVD hysteresis	-	-	100	-	mV
$V_{POR/PDR}$	Power on/power down reset threshold	Falling edge	1.8(1)	1.88	1.96	V
		Rising edge	1.84	1.92	2.0	V
$V_{PDRhyst}$	PDR hysteresis	-	-	40	-	mV
$t_{RSTTEMPO}$(2)	Reset temporization	-	1.5	2.5	4.5	ms

1. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.
2. Guaranteed by design, not tested in production.

5.3.4 Embedded reference voltage

The parameters given in *Table 11* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

Figure 10. Typical current consumption in Run mode versus temperature (at 3.6 V) - code with data processing running from RAM, peripherals enabled

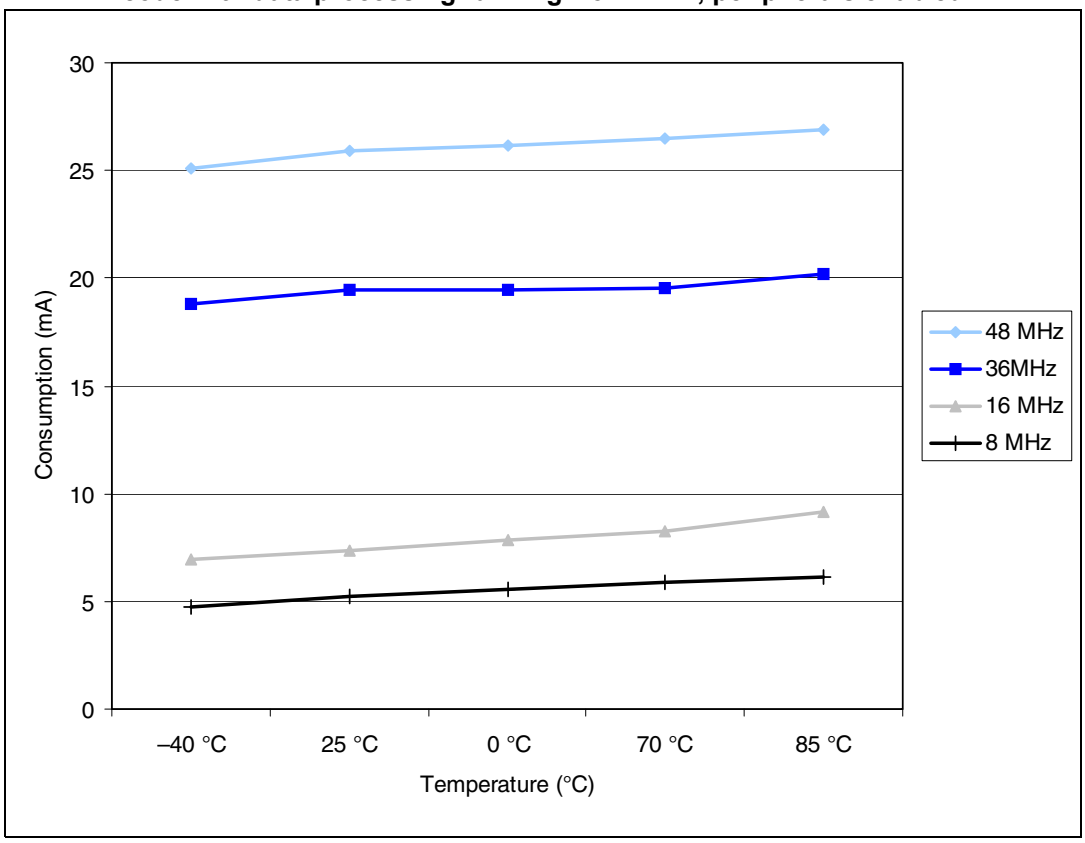


Figure 11. Typical current consumption in Run mode versus temperature (at 3.6 V) - code with data processing running from RAM, peripherals disabled

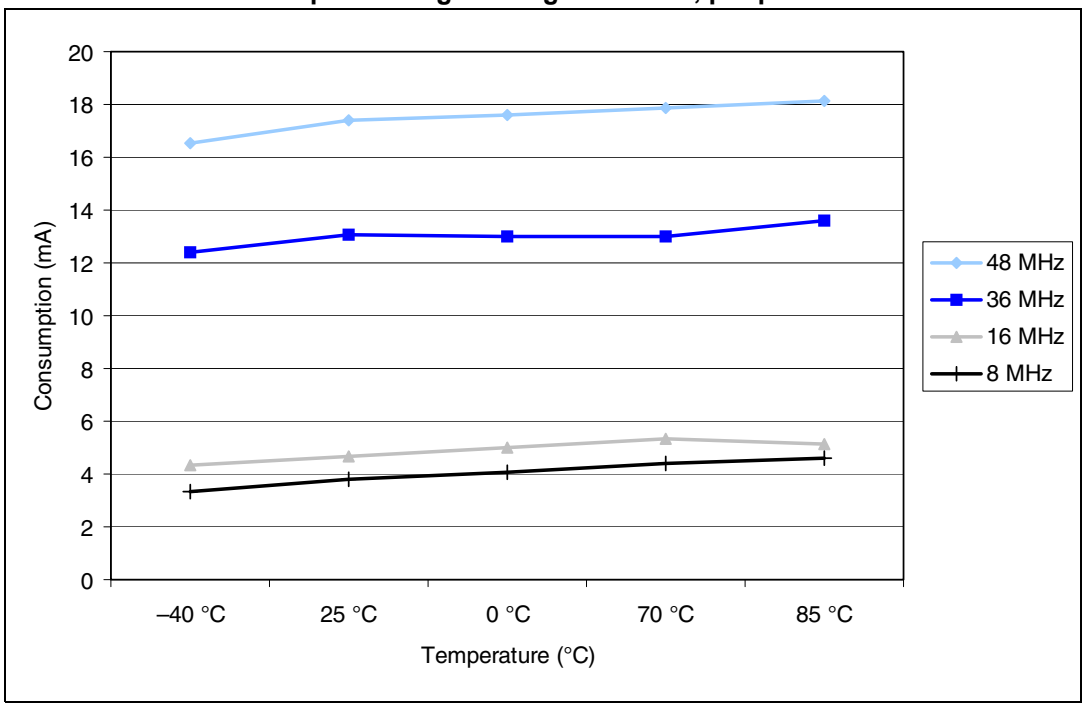


Table 14. Maximum current consumption in Sleep mode, code running from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Max(1)	Unit
				T_A = 85 °C	
I_{DD}	Supply current in Sleep mode	External clock(2), all peripherals enabled	48 MHz	17	mA
			36 MHz	14	
			24 MHz	10	
			16 MHz	7	
			8 MHz	4	
		External clock(2), all peripherals disabled	48 MHz	6	
			36 MHz	5	
			24 MHz	4.5	
			16 MHz	4	
			8 MHz	3	

1. Based on characterization, tested in production at V_{DD} max and f_{HCLK} max with peripherals enabled.
2. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Table 15. Typical and maximum current consumptions in Stop and Standby modes

Symbol	Parameter	Conditions	Typ(1)			Max	Unit
			V_{DD}/ V_{BAT} = 2.4 V	V_{DD}/V_{BAT} = 3.3 V	V_{DD}/V_{BAT} = 2.0 V	T_A = 85 °C	
I_{DD}	Supply current in Stop mode	Regulator in Run mode. Low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	21.3	21.7	-	160	µA
		Regulator in Low Power mode. Low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	11.3	11.7	-	145	
	Supply current in Standby mode(2)	Low-speed internal RC oscillator and independent watchdog ON	2.75	3.4	-	-	
		Low-speed internal RC oscillator ON, independent watchdog OFF	2.55	3.2	-	-	
		Low-speed internal RC oscillator and independent watchdog OFF, low-speed oscillator and RTC OFF	1.55	1.9	-	3.2	
I_{DD_VBAT}	Backup domain supply current	Low-speed oscillator and RTC ON	1.1	1.4	0.9	1.9(3)	

1. Typical values are measured at T_A = 25 °C.

3. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Table 17. Typical current consumption in Sleep mode, code running from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Typ(1)	Typ(1)	Unit
				All peripherals enabled(2)	All peripherals disabled	
I_{DD}	Supply current in Sleep mode	External clock(3)	48 MHz	8.7	3.8	mA
			36 MHz	6.7	3.1	
			24 MHz	4.8	2.3	
			16 MHz	3.4	1.8	
			8 MHz	2	1.2	
			4 MHz	1.5	1.1	
			2 MHz	1.25	1	
			1 MHz	1.1	0.98	
			500 kHz	1.05	0.96	
			125 kHz	1	0.95	
		Running on High Speed Internal RC (HSI), AHB prescaler used to reduce the frequency	48 MHz	8.1	3.2	
			36 MHz	6.1	2.5	
			24 MHz	4.2	1.7	
			16 MHz	2.8	1.2	
			8 MHz	1.4	0.55	
			4 MHz	0.9	0.5	
			2 MHz	0.7	0.45	
			1 MHz	0.55	0.42	
			500 kHz	0.48	0.4	
			125 kHz	0.4	0.38	

1. Typical values are measures at T_A = 25 °C, V_{DD} = 3.3 V.
2. Add an additional power consumption of 0.8 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).
3. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Figure 16. High-speed external clock source AC timing diagram

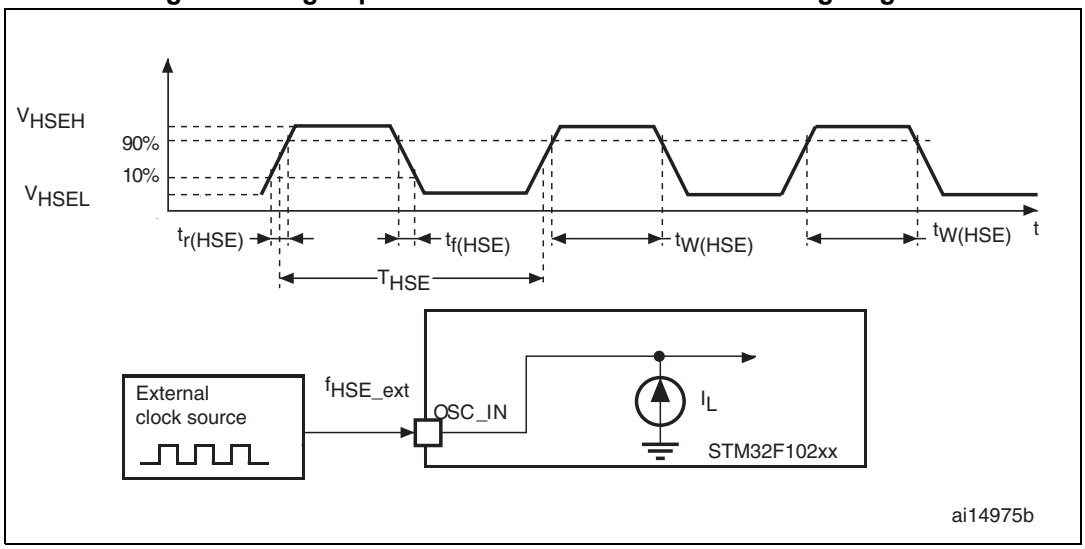
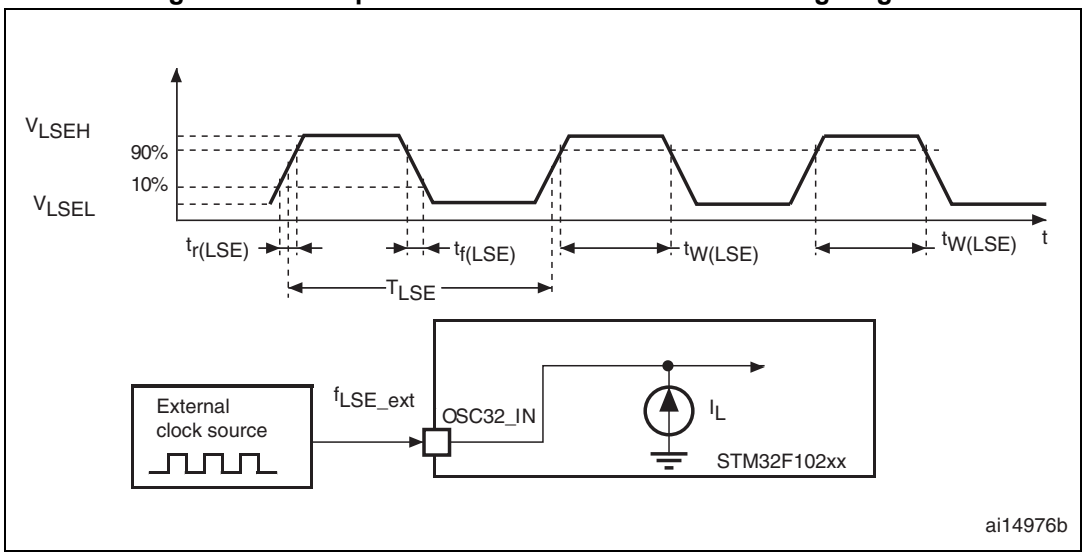


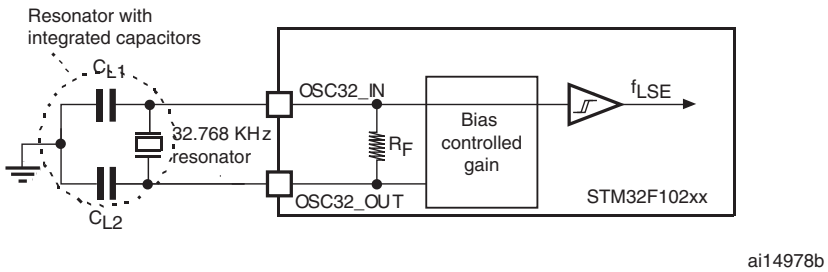
Figure 17. Low-speed external clock source AC timing diagram



Note: For CL1 and CL2 it is recommended to use high-quality ceramic capacitors in the 5 pF to 15 pF range selected to match the requirements of the crystal or resonator. CL1 and CL2 are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of CL1 and CL2.
Load capacitance CL has the following formula: CL = CL1 x CL2 / (CL1 + CL2) + C_{stray} where C_{stray} is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF.

Caution: To avoid exceeding the maximum value of CL1 and CL2 (15 pF) it is strongly recommended to use a resonator with a load capacitance CL ≤7 pF. Never use a resonator with a load capacitance of 12.5 pF.
Example: if you choose a resonator with a load capacitance of CL = 6 pF, and Cstray = 2 pF, then CL1 = CL2 = 8 pF.

Figure 19. Typical application with a 32.768 kHz crystal



5.3.7 Internal clock source characteristics

The parameters given in *Table 23* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

High-speed internal (HSI) RC oscillator

Table 23. HSI oscillator characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{HSI}	Frequency	-		-	8	-	MHz
$DuCy_{(HSI)}$	Duty cycle	-		45	-	55	%
ACC_{HSI}	Accuracy of the HSI oscillator	User-trimmed with the RCC_CR register(2)		-	-	1(3)	%
		Factory-calibrated(4)(5)	T_A = –40 to 105 °C	–2.0	-	2.5	%
			T_A = –10 to 85 °C	–1.5	-	2.2	%
			T_A = 0 to 70 °C	–1.3	-	2	%
			T_A = 25 °C	–1.1	-	1.8	%
$t_{su(HSI)}$(4)	HSI oscillator startup time	-		1	-	2	µs
$I_{DD(HSI)}$(4)	HSI oscillator power consumption	-		-	80	100	µA

1. V_{DD} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.

2. Refer to application note AN2868 “STM32F10xxx internal RC oscillator (HSI) calibration” available from the ST website www.st.com.
3. Guaranteed by design, not tested in production.
4. Based on characterization, not tested in production.
5. The actual frequency of HSI oscillator may be impacted by a reflow, but does not drift out of the specified range.

Low-speed internal (LSI) RC oscillator

Table 24. LSI oscillator characteristics (1)

Symbol	Parameter	Min(2)	Typ	Max	Unit
f_{LSI}	Frequency	30	40	60	kHz
$t_{su(LSI)}$(3)	LSI oscillator startup time	-	-	85	µs
$I_{DD(LSI)}$(3)	LSI oscillator power consumption	-	0.65	1.2	µA

1. V_{DD} = 3 V, T_A = -40 to 85 °C unless otherwise specified.
2. Based on characterization, not tested in production.
3. Guaranteed by design, not tested in production.

Wakeup time from low-power mode

The wakeup times given in *Table 25* is measured on a wakeup phase with a 8-MHz HSI RC oscillator. The clock source used to wake up the device depends from the current operating mode:

- Stop or Standby mode: the clock source is the RC oscillator
- Sleep mode: the clock source is the clock that was set before entering Sleep mode.

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

Table 25. Low-power mode wakeup timings

Symbol	Parameter	Typ	Unit
$t_{WUSLEEP}$(1)	Wakeup from Sleep mode	1.8	µs
t_{WUSTOP}(1)	Wakeup from Stop mode (regulator in run mode)	3.6	µs
	Wakeup from Stop mode (regulator in low-power mode)	5.4	
$t_{WUSTDBY}$(1)	Wakeup from Standby mode	50	µs

1. The wakeup times are measured from the wakeup event to the point at which the user application code reads the first instruction.

5.3.8 PLL characteristics

The parameters given in *Table 26* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device is monitored while a simple application is executed (toggling 2 LEDs through the I/O ports), This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 30. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{HCLK}]	Unit
				8/48 MHz	
S_{EMI}	Peak level	V_{DD} = 3.3 V, T_A = 25 °C.	0.1 MHz to 30 MHz	7	dBµV
			30 MHz to 130 MHz	8	
			130 MHz to 1GHz	13	
			SAE EMI Level	3.5	-

5.3.11 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 31. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to JESD22-A114	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to ANSI/ESD STM5.3.1	II	500	

1. Based on characterization results, not tested in production.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78 IC latch-up standard.

Table 32. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II level A

5.3.15 TIM timer characteristics

The parameters given in *Table 38* are guaranteed by design.

Refer to *Section 5.3.13: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 38. TIMx(1) characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48 MHz	20.84	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 48 MHz	0	24	MHz
Res_{TIM}	Timer resolution	-	-	16	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48 MHz	0.0208	1365	µs
t_{MAX_COUNT}	Maximum possible count	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48 MHz	-	89.48	s

1. TIMx is used as a general term to refer to the TIM2, TIM3 and TIM4 timers.

5.3.16 Communications interfaces

I²C interface characteristics

The STM32F102xx medium-density USB access line I²C interface meets the requirements of the standard I²C communication protocol with the following restrictions: the I/O pins SDA and SCL are mapped to are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.

The I²C characteristics are described in *Table 39*. Refer also to *Section 5.3.13: I/O port characteristics* for more details on the input/output alternate function characteristics (SDA and SCL).

Figure 27. SPI timing diagram - slave mode and CPHA=0

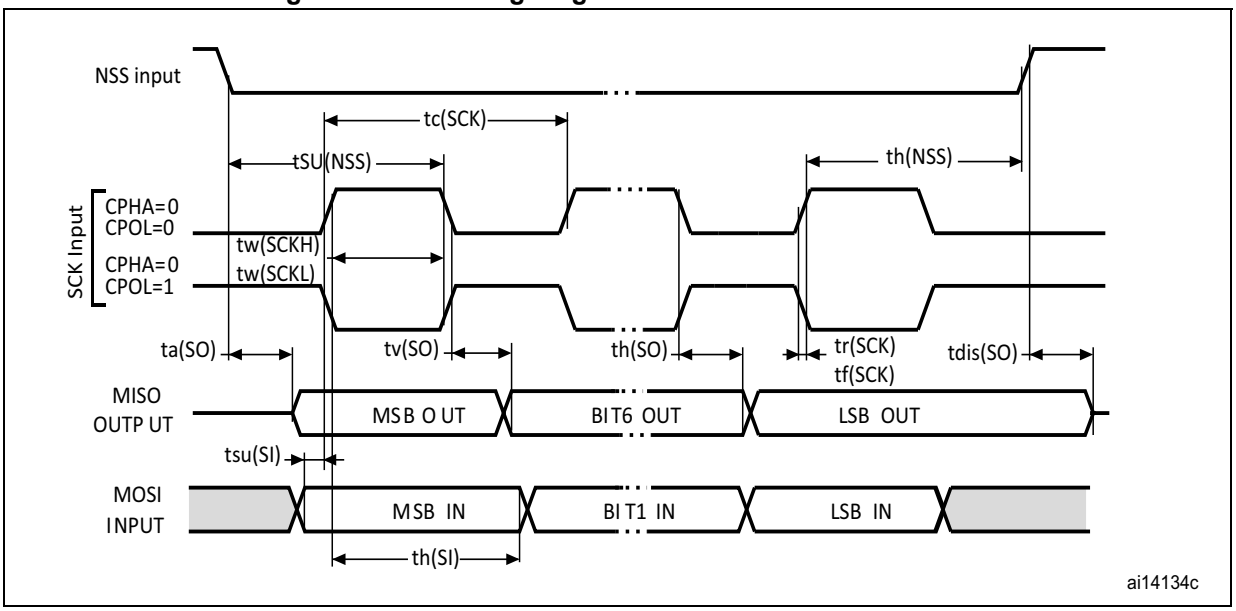
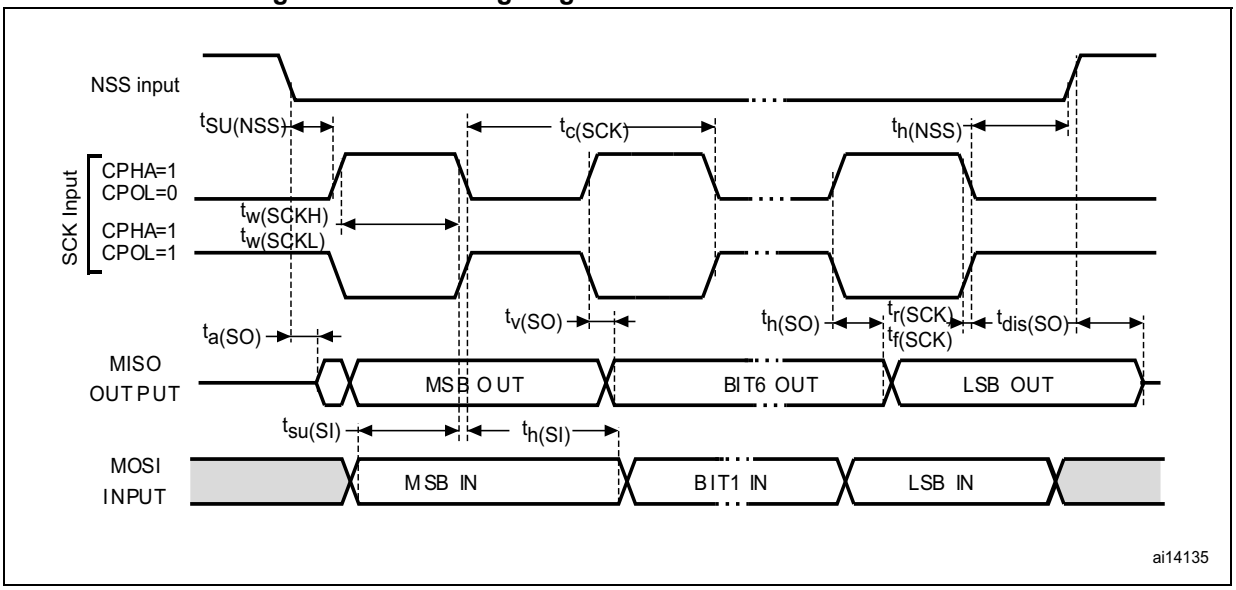
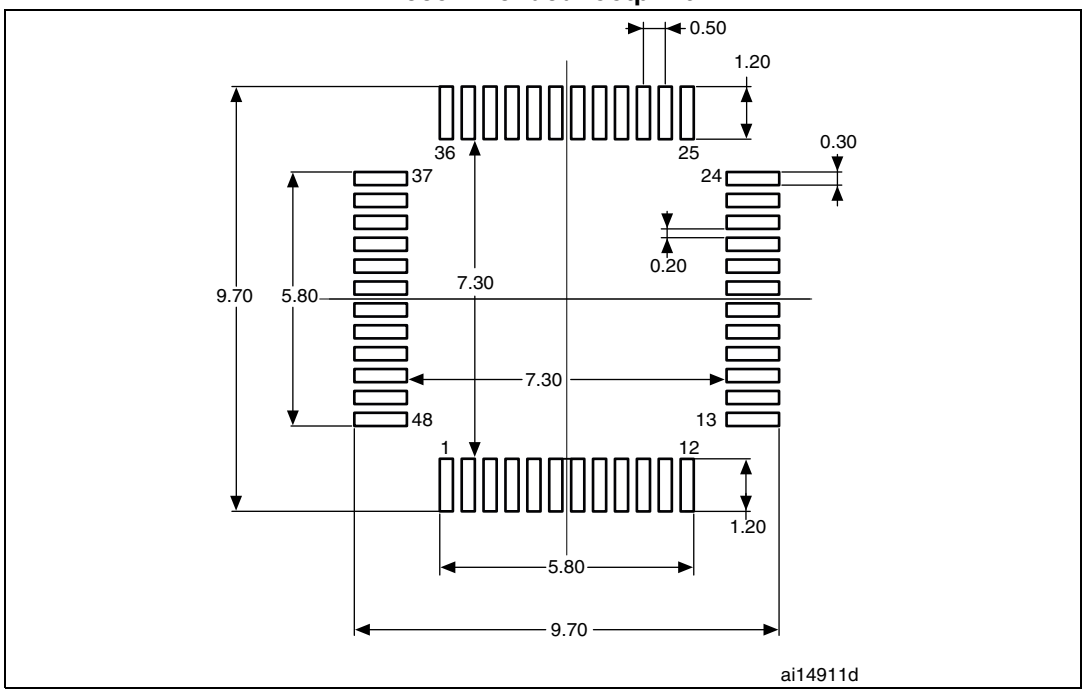


Figure 28. SPI timing diagram - slave mode and CPHA=1(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 38. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package recommended footprint

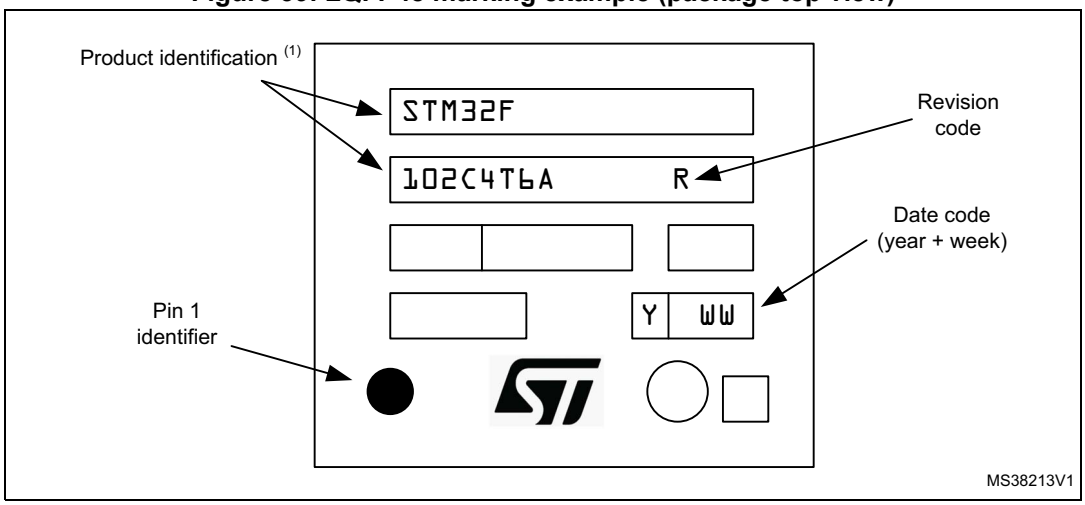


1. Dimensions are expressed in millimeters.

Device marking for LQFP48

Figure 39 gives an example of topside marking orientation versus pin 1 identifier location.

Figure 39. LQFP48 marking example (package top view)



1. Samples marked “ES” are to be considered as “Engineering Samples”: i.e. they are intended to be sent to customer for electrical compatibility evaluation and may be used to start customer qualification where specifically authorized by ST in writing. In no event ST will be liable for any customer usage in production. Only if ST has authorized in writing the customer qualification Engineering Samples can be used for reliability qualification trials.

6.3 Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the values given in *Table 8: General operating conditions*.

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

T_J max = T_A max + (P_D max × Θ_{JA})

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 52. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LQFP48 - 7 × 7 mm / 0.5 mm pitch	55	°C/W
	Thermal resistance junction-ambient LQFP64 - 10 × 10 mm / 0.5 mm pitch	45	

6.4 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.