



Welcome to [E-XFL.COM](#)

### Understanding [Embedded - DSP \(Digital Signal Processors\)](#)

[Embedded - DSP \(Digital Signal Processors\)](#) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

### Applications of [Embedded - DSP \(Digital Signal Processors\)](#)

#### Details

|                         |                                                                                                                                         |
|-------------------------|-----------------------------------------------------------------------------------------------------------------------------------------|
| Product Status          | Obsolete                                                                                                                                |
| Type                    | Audio                                                                                                                                   |
| Interface               | I <sup>2</sup> C, SPI                                                                                                                   |
| Clock Rate              | 110MHz                                                                                                                                  |
| Non-Volatile Memory     | -                                                                                                                                       |
| On-Chip RAM             | -                                                                                                                                       |
| Voltage - I/O           | 3.30V                                                                                                                                   |
| Voltage - Core          | 1.50V                                                                                                                                   |
| Operating Temperature   | -40°C ~ 85°C (TA)                                                                                                                       |
| Mounting Type           | Surface Mount                                                                                                                           |
| Package / Case          | 100-BQFP                                                                                                                                |
| Supplier Device Package | 100-PQFP/QIP (20x14)                                                                                                                    |
| Purchase URL            | <a href="https://www.e-xfl.com/product-detail/onsemi/lc75055pe-6158-h">https://www.e-xfl.com/product-detail/onsemi/lc75055pe-6158-h</a> |

# LC75055PE

**DC Electrical Characteristics** at  $T_a = -40$  to  $85^\circ\text{C}$ ,  $DV_{SS\_1}$  to 3 =  $COAV_{SS1}$  to 6 =  $AVB = XV_{SS} = AVCOV_{SS} = 0V$

| Parameter                              | Symbol      | Conditions and applicable pin                                          | min | typ                 | max  | Unit          |
|----------------------------------------|-------------|------------------------------------------------------------------------|-----|---------------------|------|---------------|
| Input high level current               | $I_{IH}$    | All digital input pin                                                  |     |                     | 10   | $\mu\text{A}$ |
| Input low level current                | $I_{IL}$    | All digital input pin                                                  | -10 |                     |      | $\mu\text{A}$ |
| Output high level voltage              | $V_{OH}$    | $I_{OH} = -2\text{mA}$ :<br>Digital output pin except for DSPIO4, SDAS | 2.4 |                     |      | V             |
|                                        |             | $I_{OH} = -4\text{mA}$ :<br>DSPIO4, SDAS                               | 2.4 |                     |      | V             |
| Output low level voltage               | $V_{OL}$    | $I_{OL} = 2\text{mA}$ :<br>Digital output pin except for DSPIO4, SDAS  |     |                     | 0.4  | V             |
|                                        |             | $I_{OL} = 4\text{mA}$ :<br>DSPIO4, SDAS                                |     |                     | 0.4  | V             |
| Output OFF leak current                | $I_{OFF}$   | Unloaded:<br>All digital output pin                                    | -10 |                     | 10   | $\mu\text{A}$ |
| Crystal oscillator feedback resistance | $R_f$       | XIN, XOUT                                                              |     | 1.0                 |      | $M\Omega$     |
| CODEC reference voltage                | $V_{REF}$   | ADC_REF, ADC_REF                                                       |     | $0.5 \cdot AV_{DD}$ |      | V             |
| Power supply current                   | $I_{DDA33}$ | $COAV_{DD1}$ , 2, 3, 4, 5, 6<br>$AVCOV_{DD}$                           |     | 110                 | 157  | mA            |
|                                        | $I_{DD33}$  | $DV_{DD33}$ , $XV_{DD}$                                                |     | 10                  | 12.5 | mA            |
|                                        | $I_{DD15}$  | $DV_{DD\_1}$ , 2                                                       |     | 120                 | 173  | mA            |

**AC Electrical Characteristics** at  $AV_{DD} = DV_{DD33} = AVCOV_{DD} = 3.3V$ ,

$DV_{SS\_1}$  to 3 =  $COAV_{SS1}$  to 6 =  $AVB = XV_{SS} = AVCOV_{SS} = 0V$

$T_a = 25^\circ\text{C}$ ,  $f_s = 44.1\text{kHz}$ , signal frequency 1kHz, measurement band = 10Hz to 20kHz

| Parameter                                       | Symbol | Conditions and applicable pin                                                                               | min    | typ  | max                  | Unit      |
|-------------------------------------------------|--------|-------------------------------------------------------------------------------------------------------------|--------|------|----------------------|-----------|
| (Input selector + ADC)                          |        |                                                                                                             |        |      |                      |           |
| Full-scale analog input level                   |        |                                                                                                             |        |      | $0.85 \cdot AV_{DD}$ | Vp-p      |
| Analog block input impedance                    |        |                                                                                                             | 20     | 30   |                      | $k\Omega$ |
| Gain setting level                              |        |                                                                                                             | -12    |      | +19                  | dB        |
| Gain setting step                               |        |                                                                                                             |        | 1    |                      | dB        |
| Error between gain setting steps                |        |                                                                                                             | -0.5   |      | +0.5                 | dB        |
| S/N                                             |        | w/ A-weighted                                                                                               | 90     | 95   |                      | dB        |
|                                                 |        | w/o A-weighted                                                                                              | 87     | 92   |                      | dB        |
| Dynamic range                                   |        | w/ A-weighted                                                                                               | 90     | 95   |                      | dB        |
|                                                 |        | w/o A-weighted                                                                                              | 87     | 92   |                      | dB        |
| THD+N                                           |        | Input condition: -3dBFS                                                                                     |        | -90  | -80                  | dB        |
| Cross talk 1                                    |        | Input condition: -3dBFS, 1kHz<br>Cross talk between AUX Lch and Rch when<br>AUX differential input is used. |        | -75  | -65                  | dB        |
| Cross talk 2                                    |        | Input condition: -3dBFS, 1kHz<br>Other than cross talk1                                                     |        | -90  | -80                  | dB        |
| (ADC digital filter)                            |        |                                                                                                             |        |      |                      |           |
| Pass band frequency                             |        |                                                                                                             | 0      |      | 0.4535               | fs        |
| Stop band frequency                             |        |                                                                                                             | 0.5465 |      |                      | fs        |
| Pass band ripple                                |        |                                                                                                             |        |      | $\pm 0.04$           | dB        |
| Stop band attenuation                           |        |                                                                                                             | -69    |      |                      | dB        |
| HPF cutoff frequency DC for offset cancellation |        | $f_s$ : 44.1kHz                                                                                             |        | 0.86 |                      | Hz        |
| (Audio DAC)                                     |        |                                                                                                             |        |      |                      |           |
| Full-scale analog output level                  |        |                                                                                                             |        |      | $0.85 \cdot AV_{DD}$ | Vp-p      |
| S/N                                             |        | w/ A-weighted                                                                                               | 94     | 100  |                      | dB        |
|                                                 |        | w/o A-weighted                                                                                              | 91     | 97   |                      | dB        |
| Dynamic range                                   |        | w/ A-weighted                                                                                               | 94     | 100  |                      | dB        |
|                                                 |        | w/o A-weighted                                                                                              | 91     | 97   |                      | dB        |
| THD+N                                           |        | -3dBFS                                                                                                      |        | -91  | -80                  | dB        |
| Cross talk                                      |        | Input condition: full-scale, 1kHz                                                                           |        | -100 | -85                  | dB        |
| Mute level                                      |        | w/ A-weighted                                                                                               | 94     | 100  |                      | dB        |

Continued on next page.

## LC75055PE

Continued from preceding page.

| Parameter                                       | Symbol | Conditions and applicable pin | min    | typ | max    | Unit |
|-------------------------------------------------|--------|-------------------------------|--------|-----|--------|------|
| (ADC digital filter)                            |        |                               |        |     |        |      |
| Pass band frequency                             |        |                               | 0      |     | 0.4535 | fs   |
| Stop band frequency                             |        |                               | 0.5465 |     |        | fs   |
| Pass band ripple                                |        |                               |        |     | ±0.015 | dB   |
| Stop band attenuation                           |        |                               | -62    |     |        | dB   |
| HPF cutoff frequency for DC offset cancellation |        | fs: 44.1kHz                   |        | 1.7 |        | Hz   |
| (EVR)                                           |        |                               |        |     |        |      |
| Input impedance                                 | ZEVR1  |                               | 20     | 25  |        | kΩ   |
| Volume setting range                            |        |                               | -70    |     | 0      | dB   |
| Mute level                                      |        |                               | 85     | 95  |        | dB   |
| Volume step                                     |        |                               |        | 1   |        | dB   |
| Volume setting step error                       |        |                               | -0.5   |     | 0.5    | dB   |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

### 1.5V reference level characteristics at Ta = -40 to 85°C, DVDD33 = 3.3V,

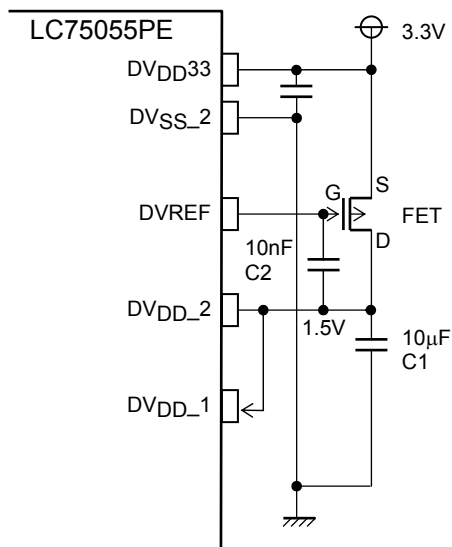
$$DVSS\_1 \text{ to } 3 = COAVSS1 \text{ to } 6 = AVB = XVSS = AVCOVSS = 0V$$

| Parameter                  | Symbol | Condition     | min | typ | max | Unit |
|----------------------------|--------|---------------|-----|-----|-----|------|
| FET Control Output voltage | DVREF  | DVDD33 = 3.3V | 0   |     | 3.3 | V    |

<Addition>

- 1.5V reference level circuit is a circuit that prepared 1.5V power-supply voltage needed in this LSI to be easily generable. The power supply of 1.5V is enabled by using recommendation FET shown in Figure 5-1.

<Figure 5-1> 1.5V reference level circuit peripheral block



\* FET Recommended Device No.  
NTR2101P (ON Semiconductor)

\* C1 is the capacitor to prevent oscillation.  
In the range of operating temperature, make sure to maintain low ESR and the capacitance recommended value is 10μF because oscillation may occur when the capacitance value changes due to the change of temperature.

- As for power supply ON, the order of DVDD33 power supply voltage (3.3V) to FET source supply voltage (3.3V) is recommended.

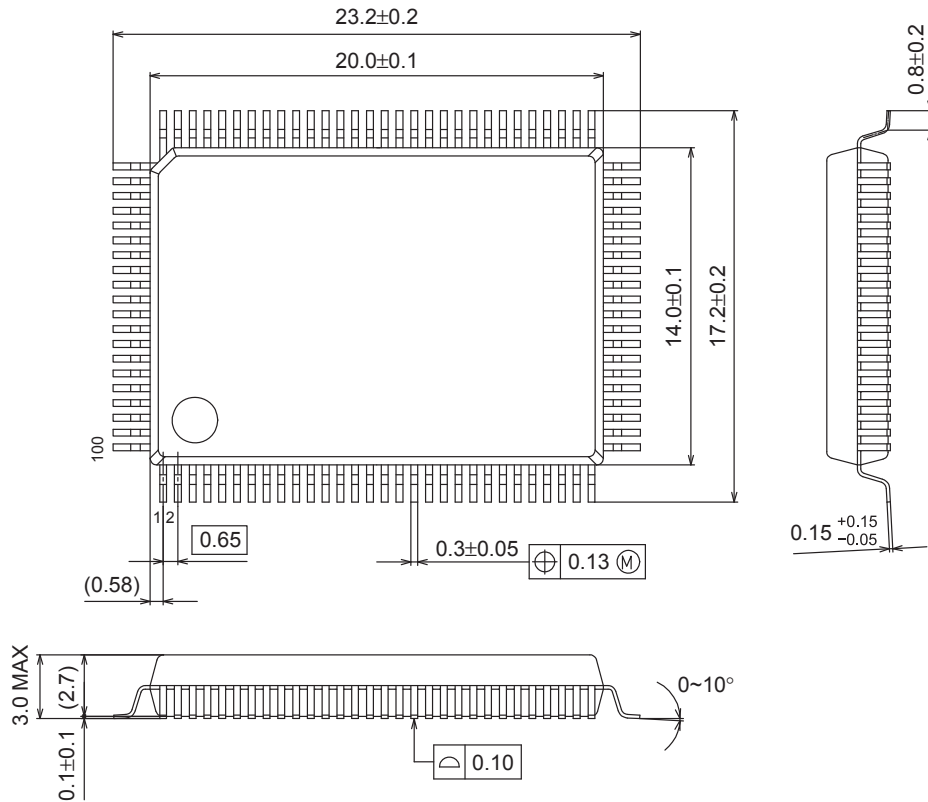
## Package Dimensions

unit : mm

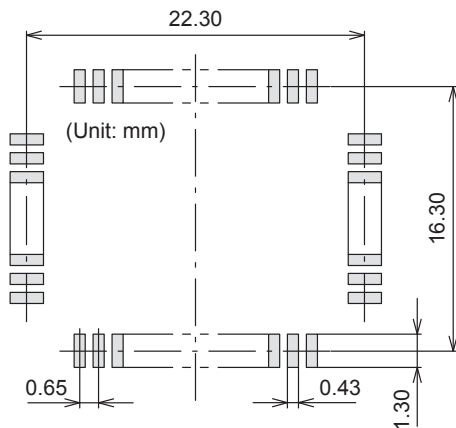
PQFP100 14x20 / QIP100E

CASE 122BV

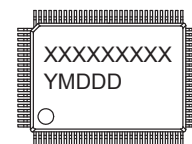
ISSUE A



### SOLDERING FOOTPRINT\*



### GENERIC MARKING DIAGRAM\*



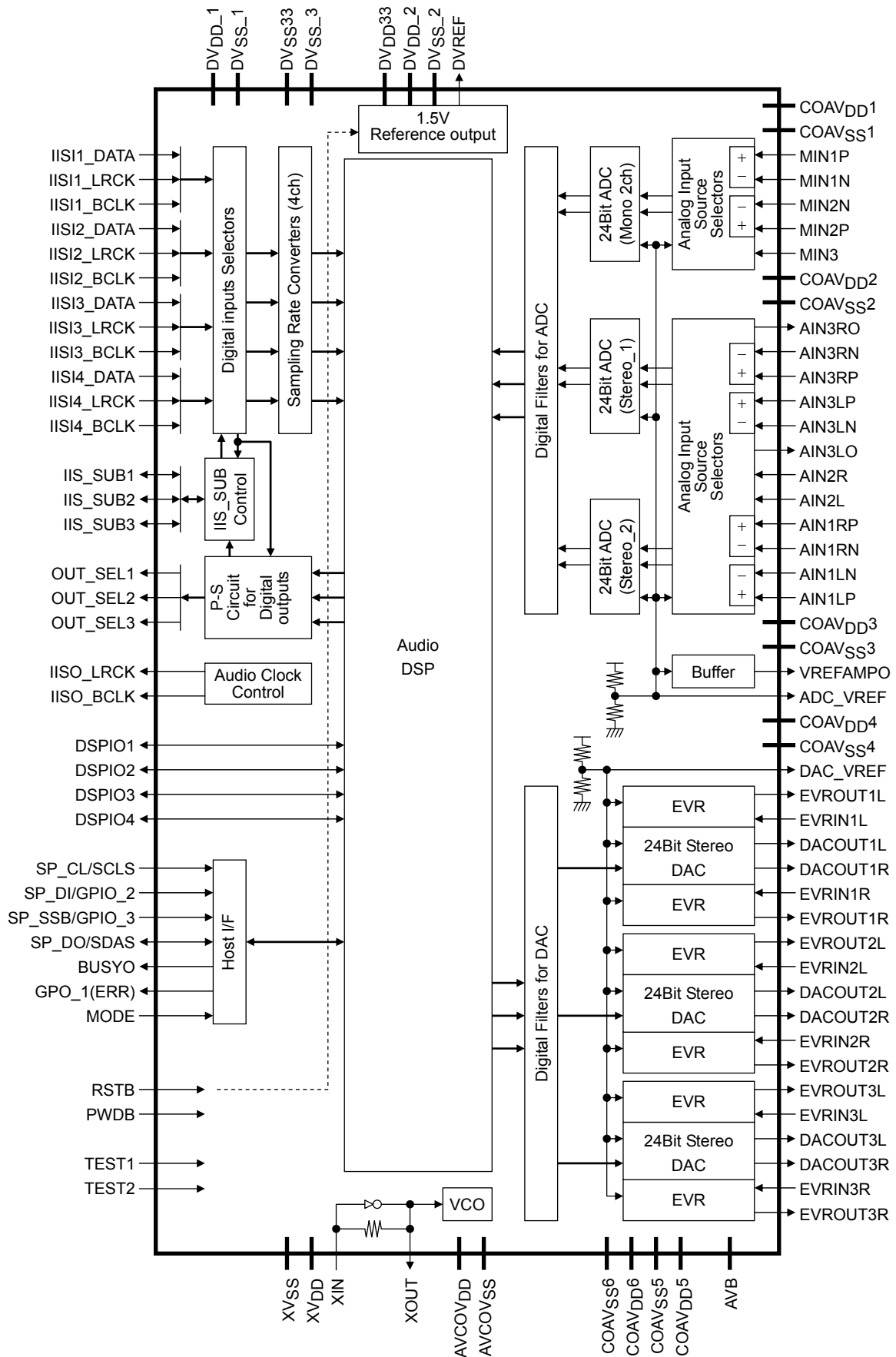
XXXXX = Specific Device Code  
Y = Year  
M = Month  
DDD = Additional Traceability Data

NOTE: The measurements are not to guarantee but for reference only.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present.

# Block Diagram



# LC75055PE

## Pin functions

| No | Pin name            | Input/output | Input/output (RSTB=L) | Functions                                                                                                                                               |
|----|---------------------|--------------|-----------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1  | COAV <sub>DD2</sub> |              |                       | Power supply for CODEC analog (3.3V)                                                                                                                    |
| 2  | COAV <sub>SS1</sub> |              |                       | Power supply for CODEC analog (GND)                                                                                                                     |
| 3  | COAV <sub>DD1</sub> |              |                       | Power supply for CODEC analog (3.3V)                                                                                                                    |
| 4  | VREFAMPO            | AO           | AO                    | Reference voltage buffer output pin, used as external reference voltage                                                                                 |
| 5  | ADC_VREF            | AO           | AO                    | Reference voltage output pin for CODEC ADC<br>A coupling capacitor is required between this pin and GND.                                                |
| 6  | DAC_VREF            | AO           | AO                    | Reference voltage output pin for CODEC DAC<br>A coupling capacitor is required between this pin and GND.                                                |
| 7  | MNI3                | AI           | AI                    | Analog single-end input pin for monaural3<br>When this pin is unused, connect it to GND via capacitor.                                                  |
| 8  | MNI2N               | AI           | AI                    | Negative analog input pin for monaural 2 or<br>Analog single-end input pin for monaural 5.<br>When this pin is unused, connect it to GND via capacitor. |
| 9  | MNI2P               | AI           | AI                    | Positive analog input pin for monaural 2 or<br>Analog single-end input pin for monaural 4.<br>When this pin is unused, connect it to GND via capacitor. |
| 10 | MNI1P               | AI           | AI                    | Positive analog input pin for monaural 1<br>When this pin is unused, connect it to GND via capacitor.                                                   |
| 11 | MNI1N               | AI           | AI                    | Negative analog input pin for monaural 1<br>When this pin is unused, connect it to GND via capacitor.                                                   |
| 12 | TEST1               | I            | I                     | Test mode setting input pin1. Normally connected to GND                                                                                                 |
| 13 | TEST2               | I            | I                     | Test mode setting input pin2. Normally connected to GND                                                                                                 |
| 14 | DV <sub>SS_3</sub>  |              |                       | Power supply for digital (GND)                                                                                                                          |
| 15 | DV <sub>DD33</sub>  |              |                       | Power supply for digital (3.3V)                                                                                                                         |
| 16 | MODE                | I            |                       | Select pin for serial communication mode ("0": I <sup>2</sup> C, "1": SPI)                                                                              |
| 17 | BUSYO               | O            | O (H)                 | System busy signal output pin for HOST CPU communication<br>(High level: the system is busy)                                                            |
| 18 | SP_DO/SDAS          | I/O          | I                     | Data output pin for SPI (slave) communication or<br>data input/ output pin for IIC (Slave) communication                                                |
| 19 | SP_CL/SCLS          | I            | I                     | Clock input pin for data transfer for SPI (slave) communication or<br>data transfer clock input pin for IIC (Slave) communication                       |
| 20 | SP_DI/GPIO_2        | I/O          | I                     | Data input pin for SPI (slave) communication or<br>General-purpose input/output pin2 for Audio DSP                                                      |
| 21 | SP_SSB/GPIO_3       | I/O          | I                     | Enable signal input pin for SPI (slave) communication (Active: low level) or<br>General-purpose input/output pin3 for audio DSP                         |
| 22 | GPO_1 (ERR)         | O            | O(L)                  | General-purpose output pin 1 for integrated DSP (will be designed to correspond to<br>communication error signal output)                                |
| 23 | PWDB                | I            | I                     | Power-down mode setting pin. Normally high level.                                                                                                       |
| 24 | RSTB                | I            | I                     | System reset pin. Make sure to set to low level when turning on power.                                                                                  |
| 25 | DSPIO1              | I/O          | I                     | Audio DSP general input/output pin 1                                                                                                                    |
| 26 | DV <sub>DD_2</sub>  |              |                       | Power supply for internal logic (1.5V)                                                                                                                  |
| 27 | DV <sub>SS_2</sub>  |              |                       | Power supply for digital (GND)                                                                                                                          |
| 28 | DVREF               | O            |                       | Control output pin for 1.5V level                                                                                                                       |
| 29 | DV <sub>DD33</sub>  |              |                       | Power supply for digital (3.3V)                                                                                                                         |
| 30 | DSPIO2              | I/O          | I                     | Audio DSP general-purpose input/output pin2                                                                                                             |
| 31 | DSPIO3              | I/O          | I                     | Audio DSP general-purpose input/output pin3                                                                                                             |
| 32 | DSPIO4              | I/O          | I                     | Audio DSP general-purpose input/output pin4 or 256fs_clock out pin.                                                                                     |
| 33 | IIS1_DATA           | I            | I                     | IIS data input pin1                                                                                                                                     |
| 34 | IIS1_LRCK           | I            | I                     | IIS word clock input pin1                                                                                                                               |
| 35 | IIS1_BCLK           | I            | I                     | IIS bit clock input pin1                                                                                                                                |
| 36 | IIS2_DATA           | I            | I                     | IIS data input pin2                                                                                                                                     |
| 37 | IIS2_LRCK           | I            | I                     | IIS word clock input pin2                                                                                                                               |
| 38 | IIS2_BCLK           | I            | I                     | IIS bit clock input pin2                                                                                                                                |
| 39 | IIS3_DATA           | I            | I                     | IIS data input pin3                                                                                                                                     |
| 40 | IIS3_LRCK           | I            | I                     | IIS word clock input pin3                                                                                                                               |
| 41 | IIS3_BCLK           | I            | I                     | IIS bit clock input pin3                                                                                                                                |
| 42 | IIS4_DATA           | I            | I                     | IIS data input pin4                                                                                                                                     |

Continued on next page.

# LC75055PE

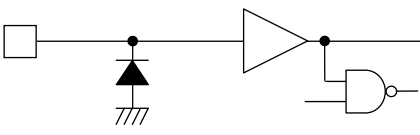
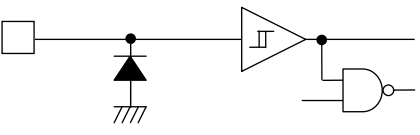
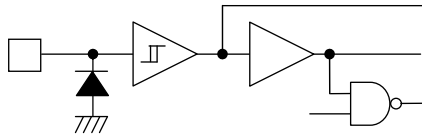
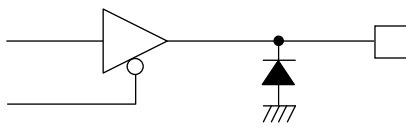
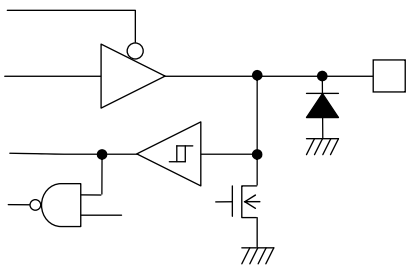
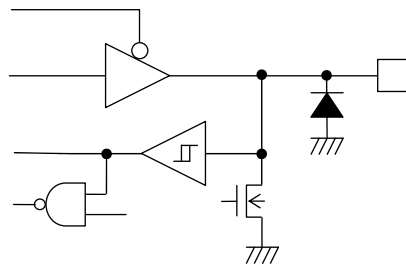
Continued from preceding page.

| No | Pin name   | Input/output | Input/output (RSTB=L) | Functions                                                                                                                                                                                |
|----|------------|--------------|-----------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 43 | IISI4_LRCK | I            | I                     | IIS word clock input pin4                                                                                                                                                                |
| 44 | IISI4_BCLK | I            | I                     | IIS bit clock input pin4                                                                                                                                                                 |
| 45 | IIS_SUB1   | I/O          | I                     | IIS data input pin5 or<br>IIS data output pin1 or IIS data output pin4                                                                                                                   |
| 46 | IIS_SUB2   | I/O          | I                     | IIS data input pin6 or IIS word clock input pin5 or<br>IIS data output pin2 or IIS word clock output pin4                                                                                |
| 47 | IIS_SUB3   | I/O          | I                     | IIS data input pin7 or IIS bit clock input pin5 or<br>IIS data output pin3 or IIS bit clock output pin4                                                                                  |
| 48 | IISO_BCLK  | O            | O (L)                 | IIS bit clock output pin (for IIS data output 1 to 3)                                                                                                                                    |
| 49 | IISO_LRCK  | O            | O (L)                 | IIS word clock output pin (for IIS data output 1 to 3)                                                                                                                                   |
| 50 | OUT_SEL1   | O            | O (L)                 | IIS data output pin1 or IIS data output pin4 or internal signal output pin1<br>(During reset, this pin is fixed to low level output.)                                                    |
| 51 | OUT_SEL2   | O            | O (L)                 | IIS data output pin2 or IIS word clock output pin4 or internal signal output pin2<br>(During reset, this pin is fixed to low level output.)                                              |
| 52 | OUT_SEL3   | O            | O (L)                 | IIS data output pin3 or IIS bit clock output pin4 or internal signal output pin3<br>(During reset, this pin is fixed to low level output.)                                               |
| 53 | DVDD_1     |              |                       | Power supply for internal logic (1.5V)                                                                                                                                                   |
| 54 | DVSS_1     |              |                       | Power supply for digital (GND)                                                                                                                                                           |
| 55 | XVSS       |              |                       | Crystal for oscillation circuit power supply. (GND)                                                                                                                                      |
| 56 | XIN        |              | Oscillation           | Crystal oscillation circuit input (11.2896MHz or 12.288MHz)                                                                                                                              |
| 57 | XOUT       |              | Oscillation           | Crystal oscillation circuit output                                                                                                                                                       |
| 58 | XVDD       |              |                       | Crystal for oscillation circuit power supply (3.3V)                                                                                                                                      |
| 59 | AVCOAVDD   |              |                       | VCO analog power supply for CODEC main clock generation(3.3V)                                                                                                                            |
| 60 | AVCOAVSS   |              |                       | VCO analog power supply for CODEC main clock generation (GND)                                                                                                                            |
| 61 | EVROUT3R   | AO           | AO                    | Electronic volume output pin.<br>When output of EVR3 is OFF, EVRIN3R input signal output to EVROUT3R via 50kΩ register.                                                                  |
| 62 | EVRIN3R    | AI           | AI                    | Electronic volume input pin. Make sure to connect this pin with DACOUT3R (DAC output) via coupling capacitor. When this pin is unused, leave it open or connect it to GND via capacitor. |
| 63 | DACOUT3R   | AO           | AO                    | DAC analog output pin. (R-channel output)<br>When output of DAC3 is OFF, pin output becomes GND.                                                                                         |
| 64 | DACOUT3L   | AO           | AO                    | DAC analog output pin. (L-channel output)<br>When output of DAC3 is OFF, pin output becomes GND.                                                                                         |
| 65 | EVRIN3L    | AI           | AI                    | Electronic volume input pin. Make sure to connect this pin with DACOUT3L (DAC output) via coupling capacitor. When this pin is unused, leave it open or connect it to GND via capacitor. |
| 66 | EVROUT3L   | AO           | AO                    | Electronic volume output pin.<br>When output of EVR3 is OFF, EVRIN3L input signal output to EVROUT3L via 50kΩ register.                                                                  |
| 67 | EVROUT2R   | AO           | AO                    | Electronic volume output pin.<br>When output of EVR2 OFF, EVRIN2R input signal output to EVROUT2R via 50kΩ register.                                                                     |
| 68 | EVRIN2R    | AI           | AI                    | Electronic volume input pin. Make sure to connect this pin with DACOUT2R (DAC output) via coupling capacitor. When this pin is unused, leave it open or connect it to GND via capacitor. |
| 69 | DACOUT2R   | AO           | AO                    | DAC analog output pin. (R-channel output)<br>When output of DAC2 is OFF, pin output becomes GND.                                                                                         |
| 70 | DACOUT2L   | AO           | AO                    | DAC analog output pin. (L-channel output)<br>When output of DAC2 is OFF, pin output becomes GND.                                                                                         |
| 71 | EVRIN2L    | AI           | AI                    | Electronic volume input pin. Make sure to connect this pin with DACOUT2L (DAC output) via coupling capacitor. When this pin is unused, leave it open or connect it to GND via capacitor. |
| 72 | EVROUT2L   | AO           | AO                    | Electronic volume output pin.<br>When output of EVR2 is OFF, EVRIN2L input signal output to EVROUT2L via 50kΩ register.                                                                  |
| 73 | EVROUT1R   | AO           | AO                    | Electronic volume output pin.<br>When output of EVR1 is OFF, EVRIN1R input signal output to EVROUT1R via 50kΩ register.                                                                  |

Continued on next page.

# LC75055PE

## Input/Output PIN equivalent circuit

| I/O                  | Equivalent circuit                                                                  | Pin                                                                                                                                                                                                                                                              | Comment                                   |
|----------------------|-------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------|
| Digital input        |    | TEST1 : 12<br>TEST2 : 13<br>MODE : 16                                                                                                                                                                                                                            | 5V-Tolerant                               |
| Digital input        |    | SP_CL/SCLS : 19<br>PWDB : 23<br>IISI1_DATA : 33<br>IISI1_LRCK : 34<br>IISI1_BCLK : 35<br>IISI2_DATA : 36<br>IISI2_LRCK : 37<br>IISI2_BCLK : 38<br>IISI3_DATA : 39<br>IISI3_LRCK : 40<br>IISI3_BCLK : 41<br>IISI4_DATA : 42<br>IISI4_LRCK : 43<br>IISI4_BCLK : 44 | 5V-Tolerant                               |
| Digital input        |    | RSTB : 24                                                                                                                                                                                                                                                        | 5V-Tolerant<br>3.3V Output<br>(Inverting) |
| Digital output       |  | BUSYO : 17<br>GPO_1(ERR) : 22<br>IISO_BCLK : 48<br>IISO_LRCK : 49<br>OUT_SEL1 : 50<br>OUT_SEL2 : 51<br>OUT_SEL3 : 52                                                                                                                                             | 5V-Tolerant                               |
| Digital input/output |  | SP_DI/GPIO_2 : 20<br>SP_SSB/GPIO_3 : 21<br>DSPIO1 : 25<br>DSPIO2 : 30<br>DSPIO3 : 31<br>IIS_SUB1 : 45<br>IIS_SUB2 : 46<br>IIS_SUB3 : 47                                                                                                                          | 5V-Tolerant                               |
| Digital input/output |  | SP_DO/SDAS : 18<br>DSPIO4 : 32                                                                                                                                                                                                                                   | 5V-Tolerant                               |

# LC75055PE

| I/O                 | Equivalent circuit | Pin                                                                                                                                                                                                                 |
|---------------------|--------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Oscillation circuit |                    | XIN : 56<br>XOUT : 57                                                                                                                                                                                               |
| DAC                 |                    | DACOUT3R : 63<br>DACOUT3L : 64<br>DACOUT2R : 69<br>DACOUT2L : 70<br>DACOUT1R : 75<br>DACOUT1L : 76                                                                                                                  |
| EVR In/Out          |                    | VINDA<br>EVRIN3R : 62<br>EVRIN3L : 65<br>EVRIN2R : 68<br>EVRIN2L : 71<br>EVRIN1R : 74<br>EVRIN1L : 77<br>VOUT<br>EVROUT3R : 61<br>EVROUT3L : 66<br>EVROUT2R : 67<br>EVROUT2L : 72<br>EVROUT1R : 73<br>EVROUT1L : 78 |
| VREF AMP Output     |                    | VREFAMPO : 4                                                                                                                                                                                                        |
| VREF Output         |                    | ADC_VREF : 5<br>DAC_VREF : 6                                                                                                                                                                                        |

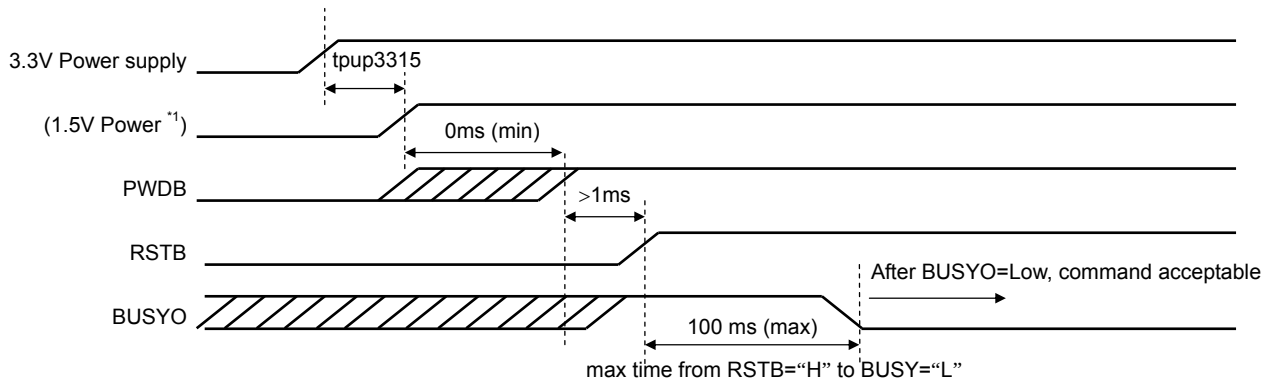


# LC75055PE

| I/O                                    | Equivalent circuit    | Pin                                                            |
|----------------------------------------|-----------------------|----------------------------------------------------------------|
| Analog<br>Selector input<br>(monaural) | <p>Inner ADC_VREF</p> | MIN3 : 7<br>MIN2P : 9<br>MIN1P : 10<br>MIN1N : 11<br>MIN2N : 8 |

## Power On/Off Timing

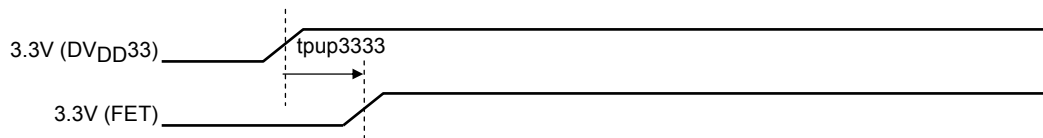
### (1) Power supply ON timing order



\*1) When a 1.5V power supply is applied in external power source directly, Please refer to this sequential order.

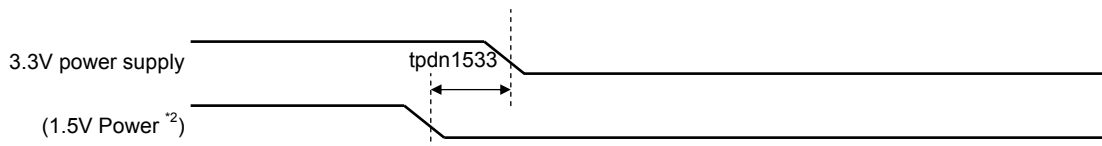
RSTB signal should be set in Low level more than 1ms from either late power supply turned on or positive edge of the PWDB signal.. In addition, the reset time is less than 100msec.

When a 1.5V power supply is produced using a onchip 1.5V reference level and external FET, It is recommended that 3.3V power supply of LC75055 (DV<sub>DD</sub>33) and 3.3V power of external FET are turned on the following order.



| Parameter              | Symbol   | Conditions | Min | Typ | Max | Unit |
|------------------------|----------|------------|-----|-----|-----|------|
| Power on (3.3V → 1.5V) | tpup3315 |            | 0   |     | 100 | msec |
| Power on (3.3V → 3.3V) | tpup3333 |            | 0   |     |     |      |

### (2) Power supply OFF timing order



\*2) When a 1.5V power supply is applied in external power source directly, Please refer to this sequential order.

| Parameter               | Symbol   | Conditions | Min | Typ | Max | Unit |
|-------------------------|----------|------------|-----|-----|-----|------|
| Power off (1.5V → 3.3V) | tpdn1533 |            | 0   |     | 100 | msec |

In addition, 5V-Tolerant input pin of LC75055 can input 3.6V voltage even if in power supply OFF condition. Furthermore, it can be applied to 5V after regular voltage was applied to each power supply. Be careful because the I/O direction of the pin is not decided before a 1.5V power supply being input.

In the voltage of each power supply, the voltage of the 3.3V power supply must be higher than the voltage of the 1.5V power supply.

## Audio input Function

### (1) Digital audio input

LC75055 has 4ch sampling rate converter as digital audio input, and Implement an independent selector circuitry every channel.

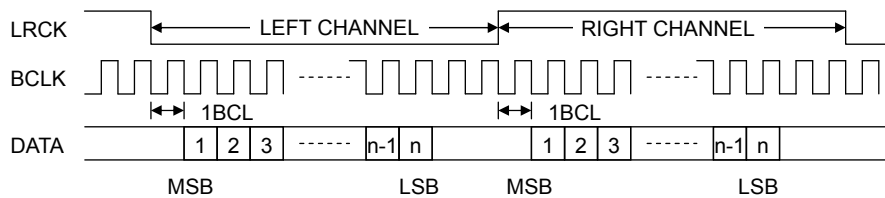
### (2) Digital input format

- |                   |                                                                                                                                                                                                                             |
|-------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1) Pin Name       | IISI1_DATA, IISI1_LRCK, IISI1_BCLK, IISI2_DATA, IISI2_LRCK, IISI2_BCLK, IISI3_DATA, IISI3_LRCK, IISI3_BCLK, IISI4_DATA, IISI4_LRCK, IISI4_BCLK, IIS_SUB1 <sup>(*)</sup> , IIS_SUB2 <sup>(*)</sup> , IIS_SUB3 <sup>(*)</sup> |
| 2) Mode           | MASTER MODE, SLAVE MODE                                                                                                                                                                                                     |
| 3) Format         | IIS MODE, LEFT JUSTIFIED MODE, RIGHT JUSTIFIED MODE <sup>(*)</sup>                                                                                                                                                          |
| 4) Bit length     | 16bit, 20bit, 24bit <sup>(*)</sup>                                                                                                                                                                                          |
| 5) BCLK Frequency | max 64fs (selectable from 32fs, 48fs, 64fs)                                                                                                                                                                                 |
| 6) Input fs       | 8kHz to 96kHz (Internal automatic distinction)                                                                                                                                                                              |

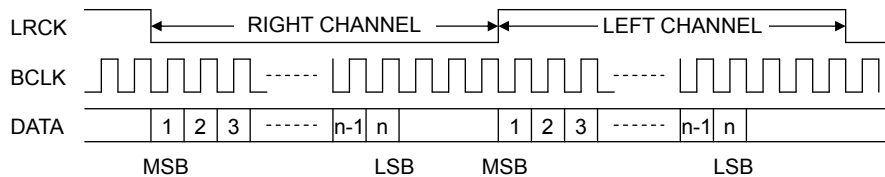
(\*) As for the pin of IIS\_SUB1/2/3, input or output is selectable.

(\*) These modes can be set independently in IIS1 and IIS2. The setting method is shown in software specifications.

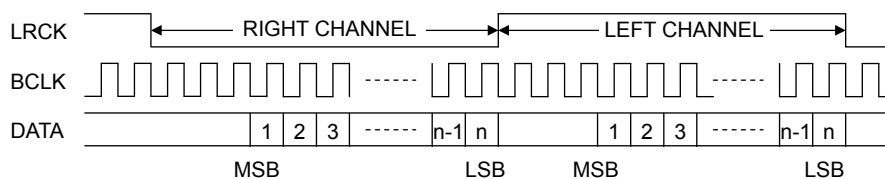
### (3) IIS MODE input timing



### (4) LEFT JUSTIFIED MODE Input Timing



### (5) RIGHT JUSTIFIED MODE Input Timing



### (6) Combination of IIS Input/Output

About IIS application pin, the following configurations are enabled.

- 4 independent input and 4 output
- 5 independent input and 3 output
- 3 independent input and 3 multi-channel input and 3 output

The setting method is shown in software specifications.

(9) Analog audio input

LC75055 has 2 ADCs (main/sub) for stereo sounds and 2 ADCs (INTA/INTB) for interruption monaural voices as analog audio in. In addition, a source select circuitry with gain setting is implemented in each ADC.

As stereo input, one of single end input or op-amp input or the differential input can be chosen.

As monaural voice inputting, one of single end input or the differential input can be chosen.

1) Main and Sub ADC input

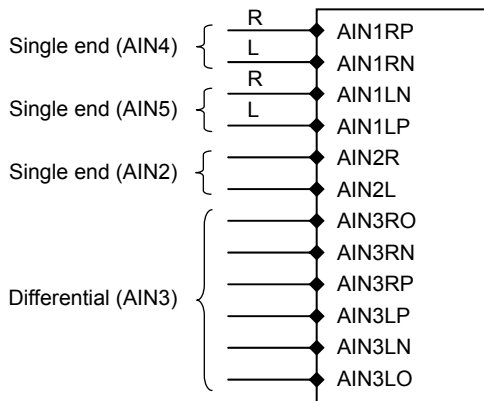
In audio main/sub ADC, a source selector of the single end input/op-amp input/differential input, and the Amp that can set a gain for each input individually are implemented. The gain set point of the main/sub is settable every each input source. Each amplifier gain is settable independently in the range of -12dB to +19dB (1dB step).

In addition, please do mute processing because a noise may occur when gain setting is changed. About the setting command, it is shown on software specifications.

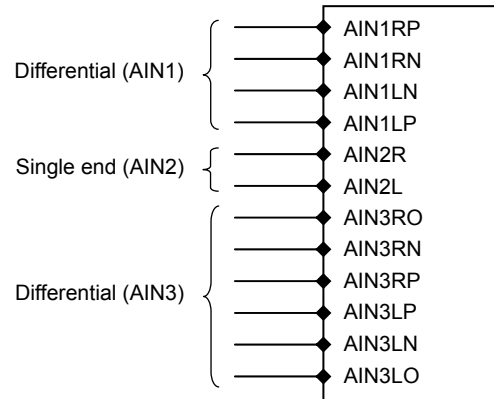
|                                  | single end input |        | differential input |                |
|----------------------------------|------------------|--------|--------------------|----------------|
|                                  | Lch              | Rch    | Lch                | Rch            |
| Single end: 3<br>Differential: 1 | AIN1LP           | AIN1LN | AIN3LP, AIN3LN     | AIN3RP, AIN3RN |
|                                  | AIN1RN           | AIN1RP |                    |                |
|                                  | AIN2L            | AIN2R  |                    |                |
| Single end: 1<br>Differential: 2 | AIN2L            | AIN2R  | AIN1LP, AIN1LN     | AIN1RP, AIN1RN |
|                                  |                  |        | AIN3LP, AIN3LN     | AIN3RP, AIN3RN |

About the method of these setting, it is appointed on software specifications.

(i) Single end input: 3, differential input: 1



(ii) Single end input: 1, differential input: 2



## 2) Monaural ADC input

Audio system ADC for interrupt sound (INTA/INTB) has the amplifier which can set a gain for a source selector of the single-end input/differential input and each input individually. The gain setting of INTA/INTB is settable every each input source. The range of the gain is -12 to +19dB (1dB steps), and set from the outside.

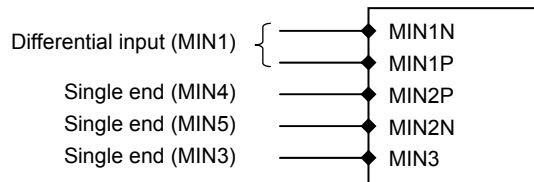
In addition, perform mute processing by all means because the noise outbreak is possible at the time of the gain setting change. About the method of the gain setting change, it is appointed on software specifications.

By a number and the kind of the interrupt sound, the following combination is enabled.

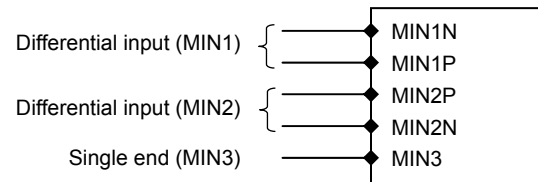
| Combination                      | single end input | differential input |
|----------------------------------|------------------|--------------------|
| Single end: 3<br>Differential: 1 | MIN2N            | MIN1P, MIN1N       |
|                                  | MIN2P            |                    |
|                                  | MIN3             |                    |
| Single end: 1<br>Differential: 2 | MIN3             | MIN1P, MIN1N       |
|                                  |                  | MIN2P, MIN2N       |

About the method of these setting, it is appointed on software specifications.

(i) Single end input: 3, differential input: 1

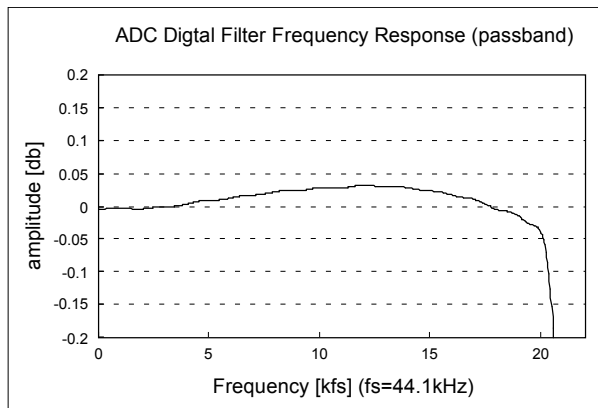
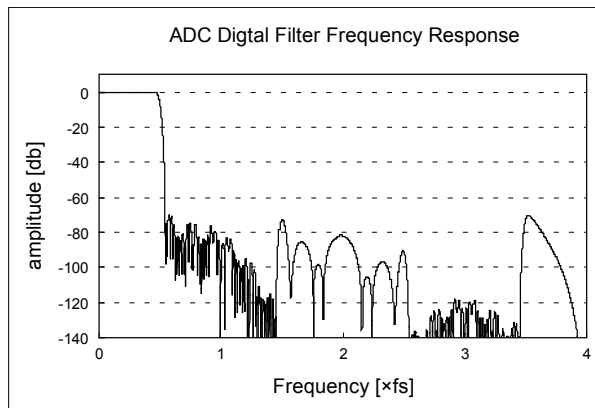


(ii) Single end input: 1, differential input: 2

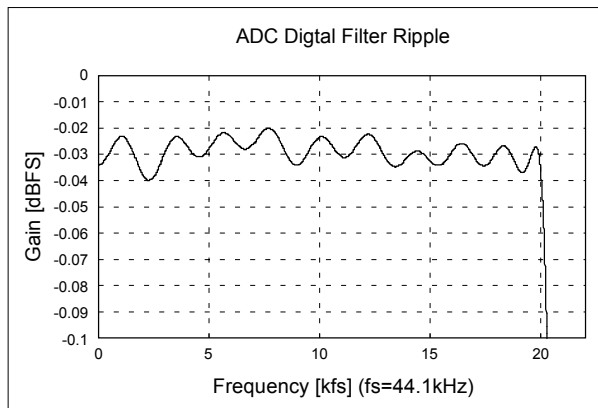
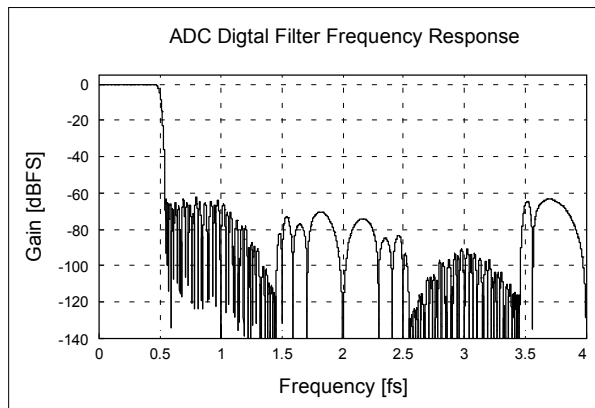


## (10) Internal digital filter characteristic in A/D and D/A converter block

### 1) A/D converter block



### 2) D/A converter block (8- TIMES OVER SAMPLING DIGITAL FILTER)



## MICON Interface

As communication interface of a host microcomputer and this LSI, one of IIC method or SPI methods is selectable. The choice of the communication mode is decided by MODE pin.

MODE: "0": IIC Interface  
"1": SPI Interface

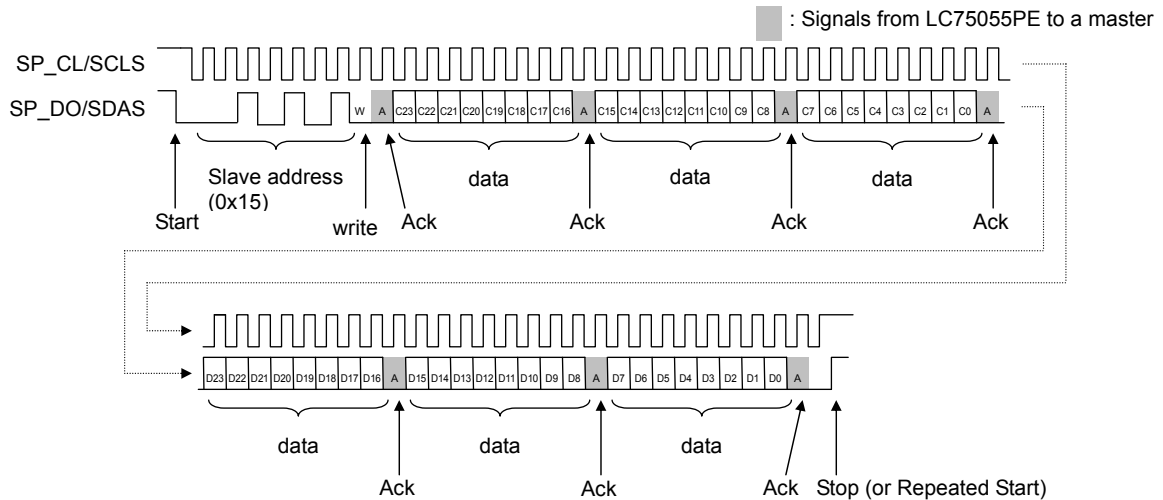
### (1) I<sup>2</sup>C Interface

The IIC slave transmission and reception interface of this LSI is based on IIC Interface Specification ver.2.1.

(Standard mode: 100Kbps, High speed mode: 400Kbps)

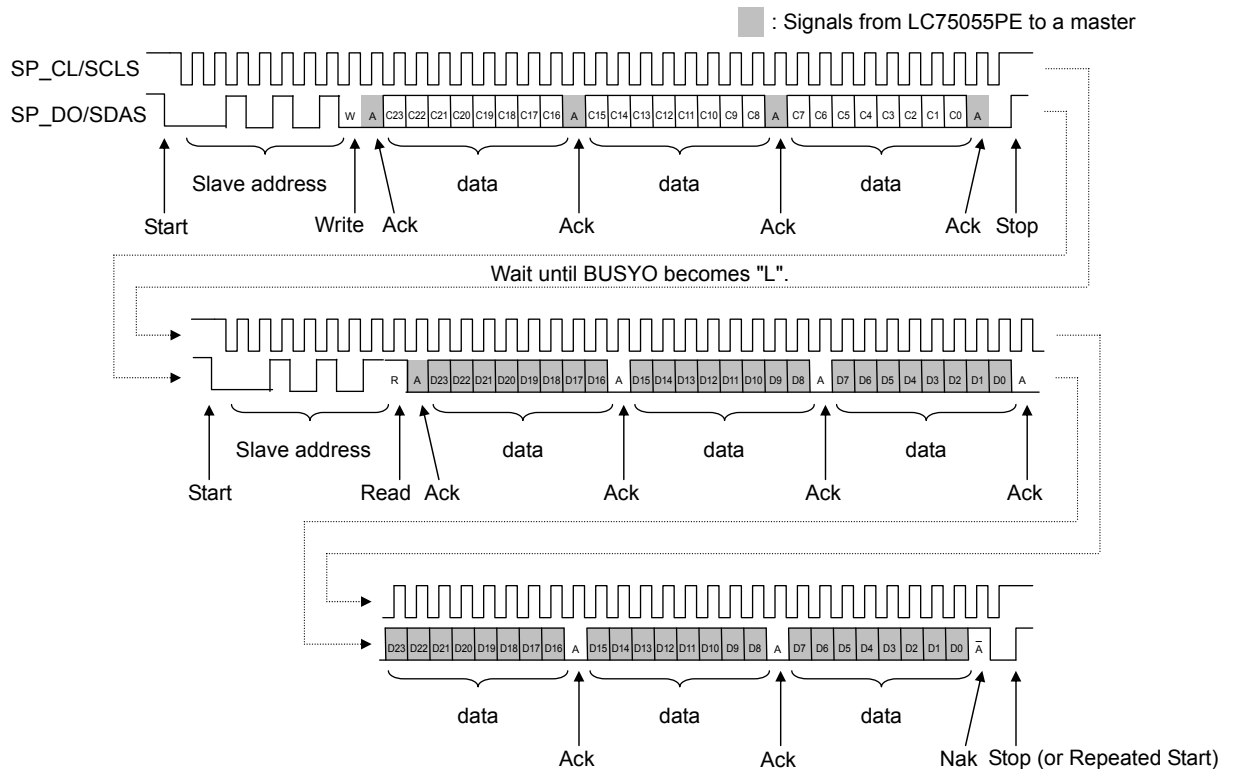
The slave address of this LSI is 0x15 (value of upper 7 bits). The data to transfer assume 8 bits 1 unit. The format of the data transmission is performed according to the following. In addition, each byte data are the MSB first.

#### Data write (6byte transmission example)



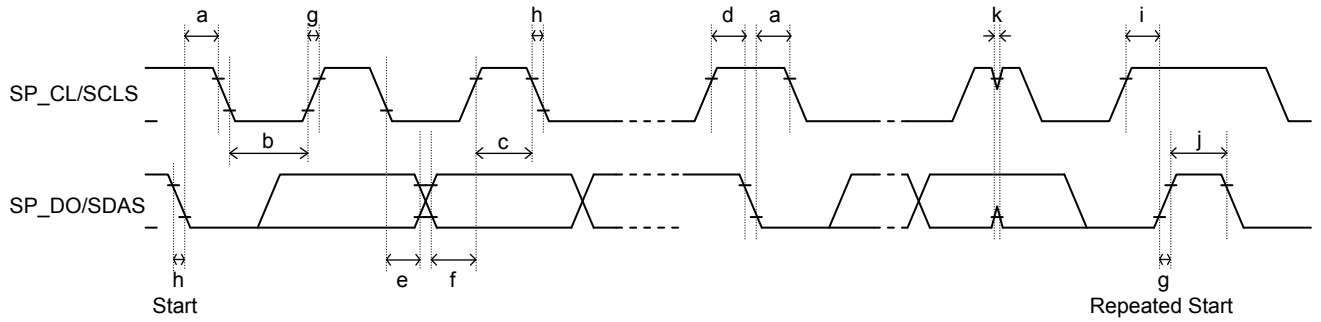
Make sure to perform communication when BUSYO pin is "L". If communication is started when BUSYO pin is "H", the operation of LC75055 will not be guaranteed.

#### Data read



The content of each data is specified by the software specification.

## Data access timing



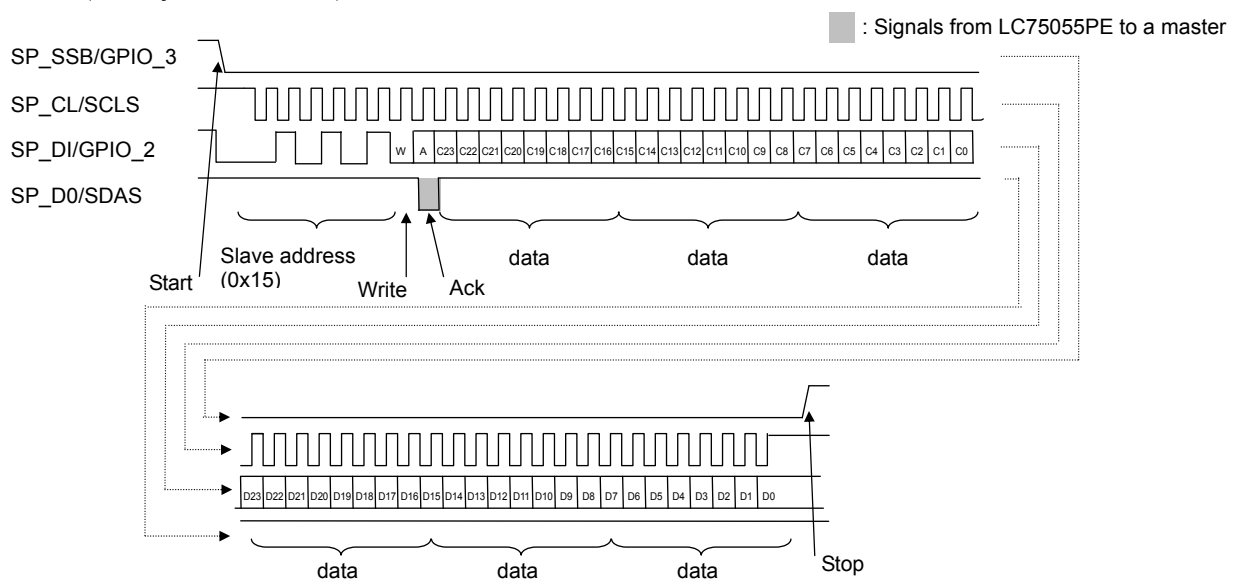
| Symbol | Timing Parameter                            | Standard mode<br>(100kbps) |      | Fast mode<br>(400kbps) |     | unit |
|--------|---------------------------------------------|----------------------------|------|------------------------|-----|------|
|        |                                             | Min                        | Max  | Min                    | Max |      |
| a      | Start (Repeated-Start) condition hold time  | 4000                       |      | 600                    | -   | ns   |
| b      | SP_CL/SCLS "P" level pulse width            | 4700                       |      | 1300                   | -   | ns   |
| c      | SP_CL/SCLS "HP" level pulse width           | 4000                       |      | 600                    | -   | ns   |
| d      | Start (Repeated-Start) condition setup time | 4700                       |      | 600                    | -   | ns   |
| e      | SP_DO/SDAS hold time                        | 0                          | 3450 | 0                      | 900 | ns   |
| f      | SP_DO/SDAS setup time                       | 250                        |      | 100                    | -   | ns   |
| g      | SP_CL/SCLS, SP_DO/SDAS rise time            | -                          | 1000 | $20+0.1C_b^{(1)}$      | 300 | ns   |
| h      | SP_CL/SCLS, SP_DO/SDAS fall time            | -                          | 300  | $20+0.1C_b^{(1)}$      | 300 | ns   |
| i      | Stop condition setup time                   | 4000                       |      | 600                    | -   | ns   |
| j      | Bus release time                            | 4700                       |      | 1300                   | -   | ns   |
| k      | Allowable spikes pulse width                | -                          |      | 0                      | -   | ns   |

$C_b$  = total capacitance of one bus line in pF.

## (2) SPI Interface

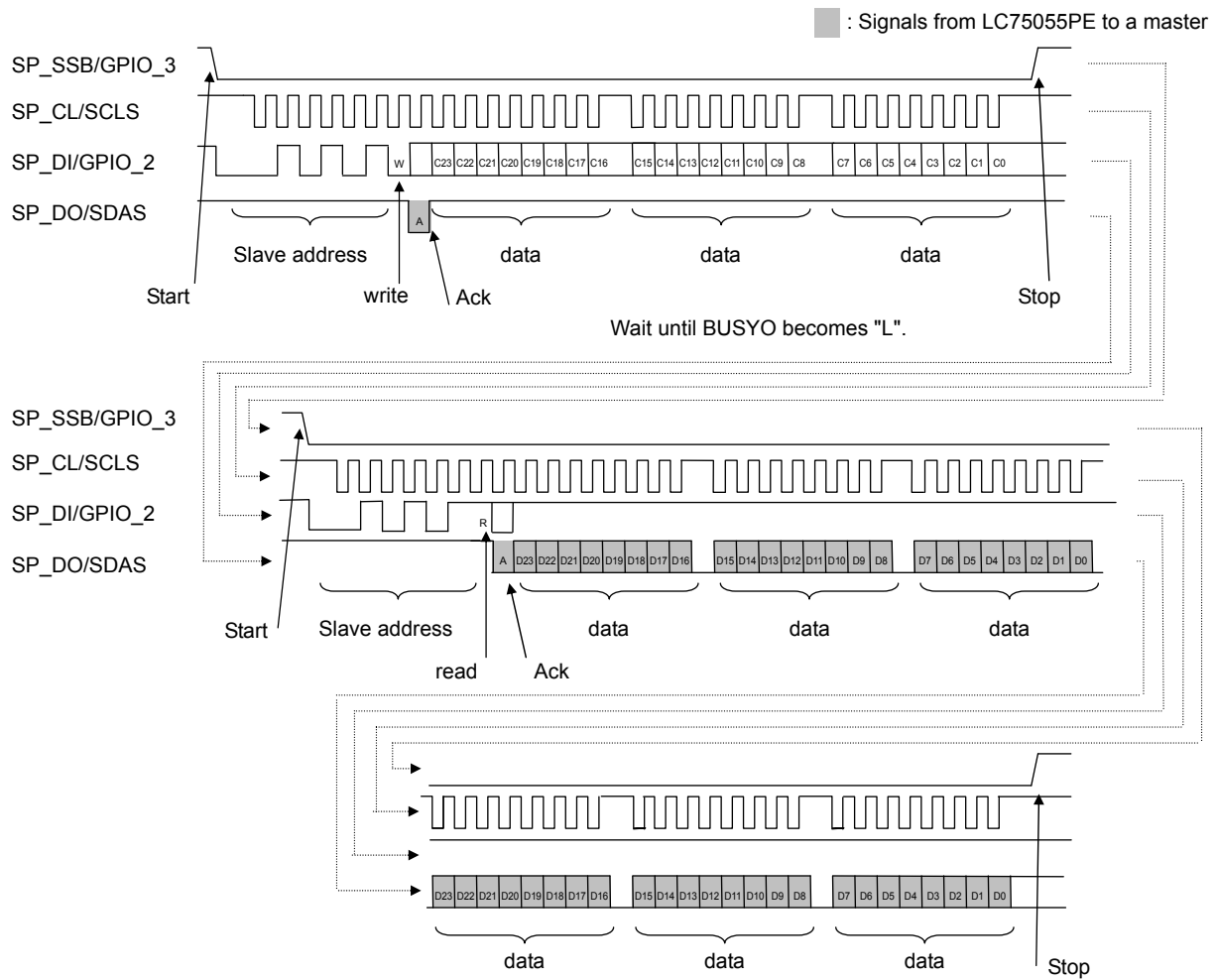
The SPI slave sending and receiving interface of this LSI communicates by using four terminals (SP\_SSB/GPIO\_3, SP\_CL/SCLS, SP\_DI/GPIO\_2, and SP\_DO/SDAS). The fast transfer in 2Mbps or less is possible unlike I2C method. The slave address is 0x15 (six bit value) when the data transfer is done to this LSI, and one unit of data is 8 bits. The data transfer is formatted as follows. Each byte data are the MSB first.

### Data write (Ex. 6byte transmission)



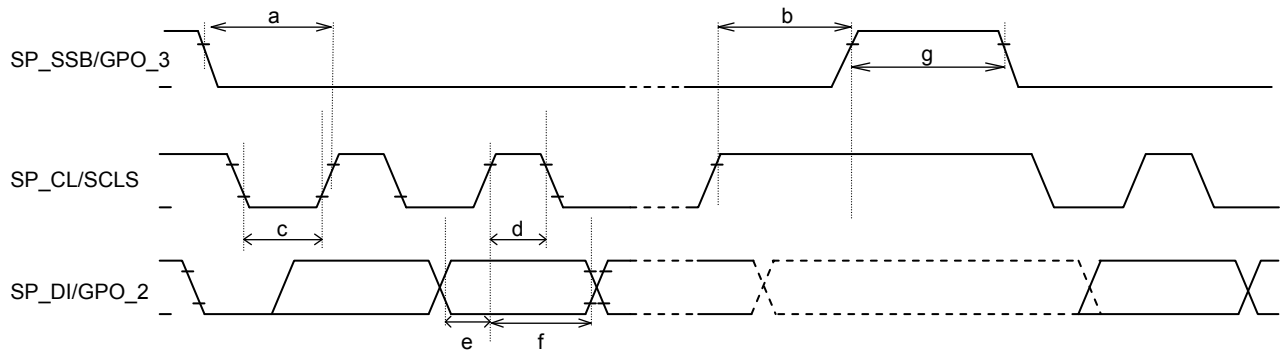
Make sure to perform communication when BUSYO pin is "L". If communication is started when BUSYO pin is "H", the operation of LC75055 will not be guaranteed.

## Data read

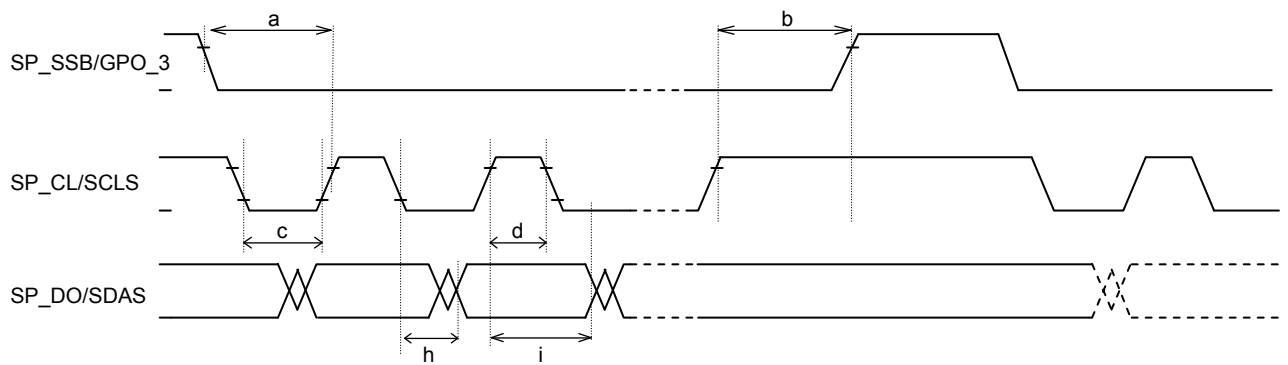


The content of each data is specified by the software specification.

## Data write timing

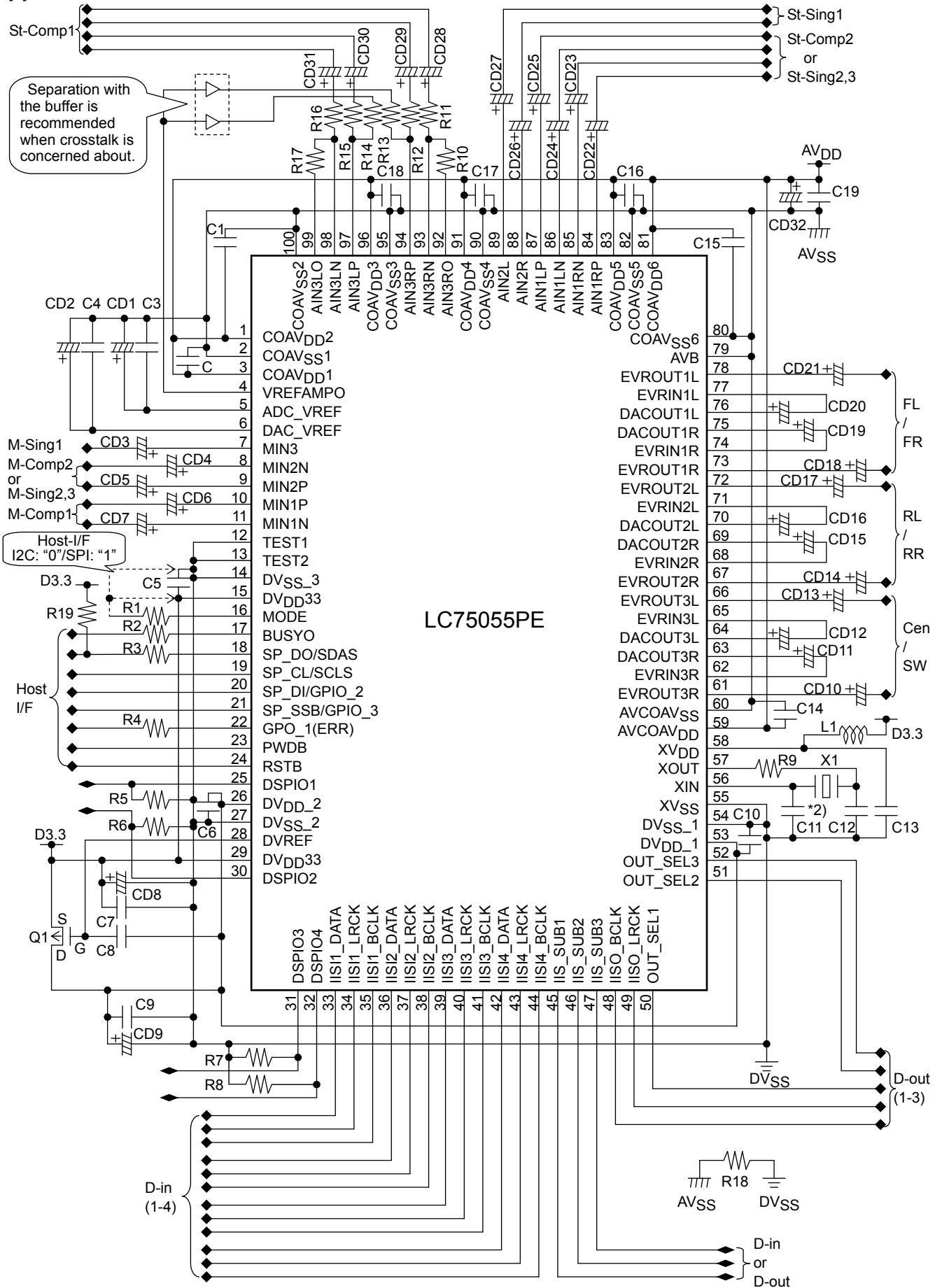


## Data read timing



| Symbol | Parametre                    | Min | Typ | Max | Unit |
|--------|------------------------------|-----|-----|-----|------|
| a      | SP_SSB setup time            | 500 |     |     | ns   |
| b      | SP_SSB hold time             | 250 |     |     | ns   |
| c      | SP_CL Low level pulse width  | 250 |     |     | ns   |
| d      | SP_CL High level pulse width | 250 |     |     | ns   |
| e      | SP_DI setup time             | 100 |     |     | ns   |
| f      | SP_DI hold time              | 100 |     |     | ns   |
| g      | Command transfer interval    | 500 |     |     | ns   |
| h      | SP_DO access time            | 0   |     | 100 | ns   |
| i      | SP_DO hold time              | 120 |     |     | ns   |

# Application Schematics



Note 1) This application schematics is just for reference and the characteristics are not guaranteed.

Note 2) The confirmation of the constant for the oscillator and the evaluation request to the oscillator vendor are recommended.

## LC75055PE

### \*) BOM for Application Schematics

| Name                   | Parameter               | Condition | Model    | Locations                                                                           | Notice                                                                                                                   |
|------------------------|-------------------------|-----------|----------|-------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------|
| Ceramic Capacitor      | 0.1μF                   |           | 1608     | C1, C2, C3, C4, C5, C6, C7, C10, C13, C14, C15, C16, C17, C18, C19                  |                                                                                                                          |
| Ceramic Capacitor      | 10μF                    |           | 3216     | C9                                                                                  |                                                                                                                          |
| Ceramic Capacitor      | 18pF                    |           | 1608     | C11, C12                                                                            | The confirmation of the constant for the oscillator and the evaluation request to the oscillator vendor are recommended. |
| Ceramic Capacitor      | 10nF                    |           | 1608     | C8                                                                                  |                                                                                                                          |
| Electrolytic Capacitor | 47μF                    | DC50V±20% |          | CD1, CD2, CD8, CD9, CD32                                                            |                                                                                                                          |
| Electrolytic Capacitor | 4.7μF                   | DC50V±20% |          | CD10, CD11, CD12, CD13, CD14, CD15, CD16, CD17, CD18, CD19, CD20, CD21              | The polarity depends on the constitution of other circuits.                                                              |
| Electrolytic Capacitor | 2.2μF                   | DC50V±20% |          | CD3, CD4, CD5, CD6, CD7, CD22, CD23, CD24, CD25, CD26, CD27, CD28, CD29, CD30, CD31 |                                                                                                                          |
| Chip Resistor          | 10kΩ                    |           | 1608     | R1, R5, R6, R7, R8, R19                                                             |                                                                                                                          |
| Chip Resistor          | 30kΩ                    |           | 1608     | R11, R16                                                                            |                                                                                                                          |
| Chip Resistor          | 30kΩ                    |           | 1608     | R12, R15                                                                            |                                                                                                                          |
| Chip Resistor          | 15kΩ                    |           | 1608     | R13, R14                                                                            |                                                                                                                          |
| Chip Resistor          | 15kΩ                    |           | 1608     | R10, R17                                                                            |                                                                                                                          |
| Chip Resistor          | 0                       |           | 1608     | R9, R18                                                                             |                                                                                                                          |
| Chip Resistor          | 100Ω                    |           | 1608     | R2, R4                                                                              |                                                                                                                          |
| Chip Resistor          | 33Ω                     |           | 1608     | R3                                                                                  |                                                                                                                          |
| Chip Bead              | MPZ1608R391A            |           | 1608     | L1                                                                                  |                                                                                                                          |
| FET                    |                         |           | NTR2101P | Q1                                                                                  |                                                                                                                          |
| Cristal Oscillator     | 11.2896MHz<br>12.288MHz |           | CX8045GA | X1                                                                                  | Selectable by System constitution.                                                                                       |

#### Notice:

- \*) The locations of the bypass capacitors (C1, C2, C5, C6, C10, C14, C15, C16, C17, C18) must be arranged close to the each LSI pin and in the aspect of the same side as the LC75055PE.
- \*) The location of the Q1 (FET) must be arranged close to the LC75055PE.
- \*) The locations of C7, CD8, C9, and CD9 must be arranged close to the Q1 (FET).
- \*) The length of the Lch and Rch of each Audio input/output wiring same as much as possible is recommended.  
(It is similar in the case of the length of the +ch and -ch of each differential input/output.)

## ORDERING INFORMATION

| Device           | Package                                    | Shipping (Qty / Packing) |
|------------------|--------------------------------------------|--------------------------|
| LC75055PE-6158-H | QIP100E(14X20)<br>(Pb-Free / Halogen Free) | 50 / Tray Foam           |

ON Semiconductor and the ON logo are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.