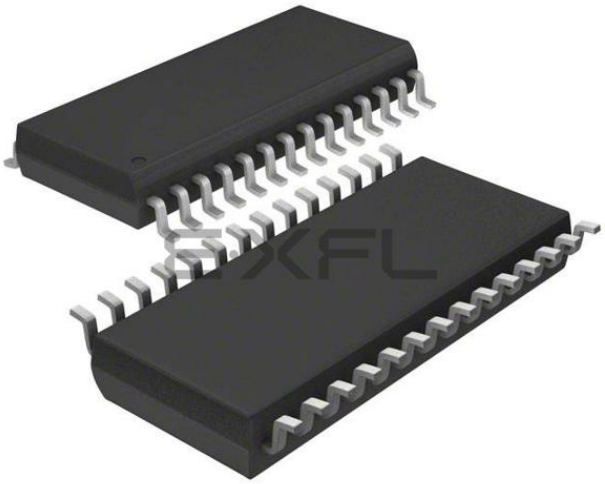

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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	Powerline Communication
Core Processor	M8C
Program Memory Type	FLASH (32KB)
Controller Series	CY8CLED
RAM Size	2K x 8
Interface	I²C, IrDA, SPI, UART/USART
Number of I/O	24
Voltage - Supply	4.75V ~ 5.25V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8cled16p01-28pvxi

1.2.3 Coupling Circuit Reference Design

The coupling circuit couples low voltage signals from the CY8CLED16P01 to the powerline. The topology of this circuit is determined by the voltage on the powerline and design constraints mandated by powerline usage regulations.

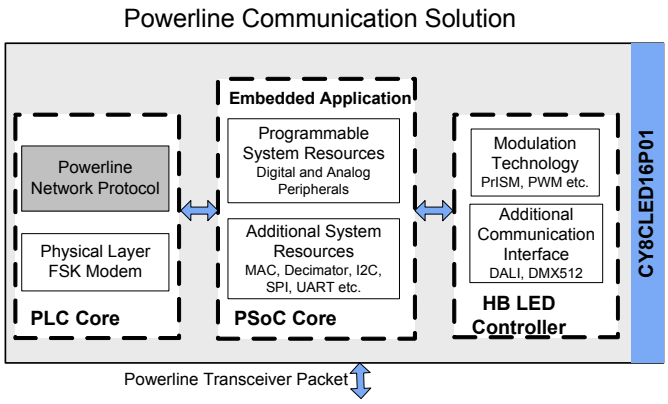
Cypress provides reference designs for a range of powerline voltages including 110V/240V AC and 12V/24V AC/DC. The CY8CLED16P01 is capable of data communication over other AC/DC Powerlines as well with the appropriate external coupling circuit. The 110V AC and 240V AC designs are compliant to the following powerline usage regulations:

- FCC Part 15 for North America
- EN 50065-1:2001 for Europe

1.3 Network Protocol

Cypress's powerline optimized network protocol performs the functions of the data link, network, and transport layers in an ISO/OSI-equivalent model.

Figure 1-3. Powerline Network Protocol



The network protocol implemented on the CY8CLED16P01 supports the following features:

- Bidirectional half duplex communication
- Master-slave or peer-to-peer network topologies
- Multiple masters on powerline network
- 8-bit logical addressing supports up to 256 powerline nodes
- 16-bit extended logical addressing supports up to 65536 powerline nodes
- 64-bit physical addressing supports up to 2^{64} powerline nodes
- Individual, broadcast or group mode addressing
- Carrier Sense Multiple Access (CSMA)
- Full control over transmission parameters
  - Acknowledged
  - Unacknowledged
  - Repeated Transmit

1.3.1 CSMA and Timing Parameters

- CSMA – The protocol provides the random selection of a period between 85 and 115 ms (out of seven possible values in this range). Within this period, the Band-In-Use (BIU) detector must indicate that the line is not in use, before attempting a transmission.
- BIU – A Band-In-Use detector, as defined under CENELEC EN 50065-1, is active whenever a signal that exceeds 86 dBμVrms anywhere in the range 131.5 kHz to 133.5 kHz is present for at least 4 ms. This threshold can be configured for different end-system applications not requiring CENELEC compliance.The modem tries to retransmit after every 85 to 115 ms when the band is in use. The transmitter times out after 1.1 seconds to 3 seconds (depending on the noise on the Powerline) and generates an interrupt to indicate that the transmitter was unable to acquire the powerline.

1.3.2 Powerline Transceiver Packet

The powerline network protocol defines a Powerline Transceiver (PLT) packet structure, which is used for data transfers between nodes across the powerline. Packet formation and data transmission across the powerline network is implemented internally in the CY8CLED16P01.

A PLT packet is divided into a variable length header (minimum 6 bytes to maximum 20 bytes, depending on address type), variable length payload (minimum 0 bytes to maximum 31 bytes), and a packet CRC byte.

This packet (preceded by a one byte preamble "0xAB") is then transmitted by the powerline modem PHY and the external coupling circuit across the powerline.

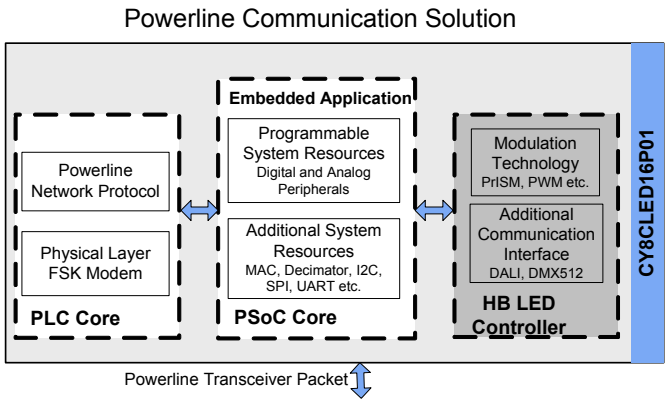
The format of the PLT packet is shown in the following table.

Table 1-1. Powerline Transceiver (PLT) Packet Structure

Byte Offset	Bit Offset							
	7	6	5	4	3	2	1	0
0x00	SA Type	DA Type		Service Type	RSVD	RSVD	Response	RSVD
0x01	Destination Address (8-Bit Logical, 16-Bit Extended Logical or 64-Bit Physical)							
0x02	Source Address (8-Bit Logical, 16-Bit Extended Logical or 64-Bit Physical)							
0x03	Command							
0x04	RSVD			Payload Length				
0x05	Seq Num				Powerline Packet Header CRC			
0x06	Payload (0 to 31 Bytes)							
	Powerline Transceiver Packet CRC							

2. High Brightness (HB) LED Controller

Figure 2-1. CY8CLED16P01: HB LED Controller



The HB LED Controller is based on Cypress's EZ-Color™ technology. EZ-Color offers the ideal control solution for high brightness (HB) LED applications requiring intelligent dimming control. EZ-Color devices combine the power and flexibility of PSoC (Programmable System-on-Chip) with Cypress's PrISM™ (Precise Illumination Signal Modulation) modulation technology providing lighting designers a fully customizable and integrated lighting solution platform.

The CY8CLED16P01 supports up to 16 independent LED channels with up to 32 bits of resolution per channel, giving lighting designers the flexibility to choose the LED array size and color quality. PSoC Designer software, with lighting-specific user modules, significantly cuts development time and simplifies implementation of fixed color points through temperature and LED binning compensation. EZ-Color's virtually limitless analog and digital customization enable simple integration of features in addition to intelligent lighting, such as battery charging, image stabilization, and motor control during the development process. These features, along with Cypress's best-in-class quality and design support, make EZ-Color the ideal choice for intelligent HB LED control applications.

The list of functions that EZ-Color devices implement are:

- LED Dimming Modulation
- Pulse Density Modulation Techniques
  - DMX512
  - DALI
- Digital Communication for Lighting
- LED Temperature Compensation
- 3- and 4-Channel Color Mixing
  - Including LED Binning Compensation
- Optical Feedback Algorithms

2.1 LED Dimming Modulation

The LED Dimming modulators are an important part of any HB LED application. All EZ-Color controllers are capable of three primary types of LED dimming modulations. These are:

- Pulse Width Modulation (PWM)
- Precise Illumination Signal Modulation (PrISM)
- Delta Sigma Modulated PWM (DSPWM)

PWM is among the most commonly used and conventional methods of modulation. It is straightforward to use and effective in practice. There are two additional techniques of modulation supported by EZ-Color that are superior to using the PWM alone:

- PrISM is a modulation technique that is developed and patented by Cypress. It results in reduced EMI as compared to the PWM technique while still providing adequate dimming control for LEDs.
- The Delta Sigma Modulated PWM technique provides higher resolution while using the same hardware resources as a conventional PWM.

LED dimming modulators use digital block resources. Digital blocks are configurable 8-bit digital peripherals. There are two types of digital blocks in the CY8CLED16P01: basic and communication. Usually, there are equal numbers of each. Any communication functions must be implemented using communication blocks but basic, noncommunication functions are implemented using either kind of block.

PWM and DSPWM modulators can have a dimming resolution of up to 16 bits. A PrISM modulator can theoretically have a dimming resolution of up to 32 bits, but the maximum recommended resolution for these modulators is 13 bits. This is because the output signal of a PrISM modulator has a frequency output range that increases with the resolution of the modulator. This increase in frequency output range is undesirable as it goes beyond the switching frequency of the current driver. Therefore, a resolution of 13 bits or lower is recommended for a PrISM modulator. Refer to application note AN47372, *PrISM Technology for LED Dimming* on http://www.cypress.com, for details.

To determine the number of digital blocks used by one PWM or PrISM modulator, use Equation 1. Note that a partial digital block cannot be used, so the result must always be rounded up. In Equation 1, n is the dimming resolution of the modulator. The resolution of dimming is determined by the color accuracy needed for the end application.

$$DigBlocks_{PWM,PRISM} = \frac{n}{8} \qquad \text{Equation 1}$$

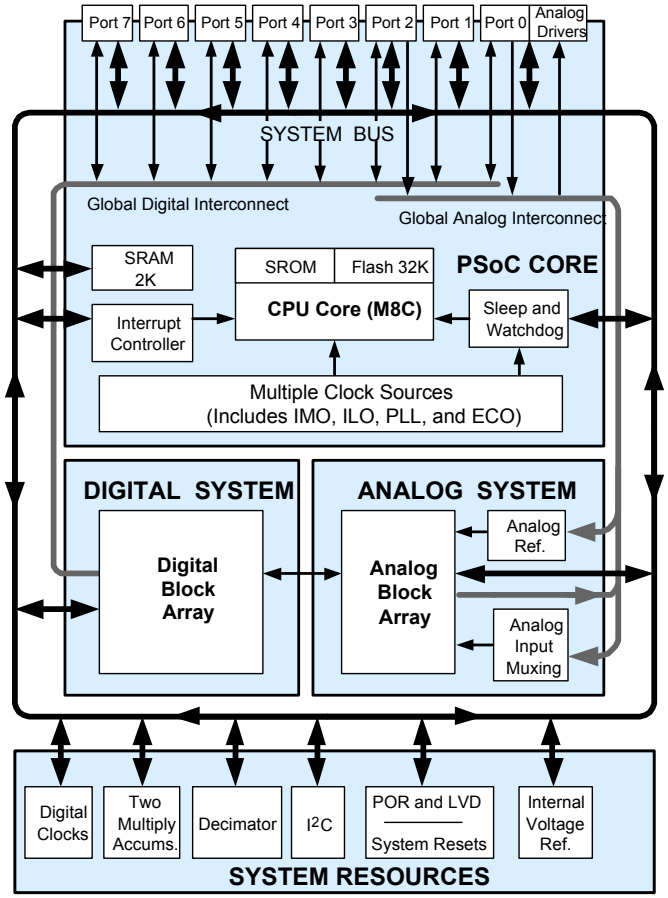
3. PSoC Core

The CY8CLED16P01 is based on the Cypress PSoC® 1 architecture. The PSoC platform consists of many *Programmable System-on-chip Controller* devices. These devices are designed to replace multiple traditional MCU-based system components with one, low cost single-chip programmable device. PSoC devices include configurable blocks of analog and digital logic, and programmable interconnects. This architecture enables the user to create customized peripheral configurations that match the requirements of each individual application. Additionally, a fast CPU, Flash program memory, SRAM data memory, and configurable I/Os are included in a range of convenient pinouts and packages.

The PSoC architecture, as shown in Figure 3-1., consists of four main areas: PSoC Core, Digital System, Analog System, and System Resources. Configurable global busing enables all the device resources to be combined into a complete custom system. The CY8CLED16P01 family can have up to five I/O ports that connect to the global digital and analog interconnects, providing access to 16 digital blocks and 12 analog blocks.

The PSoC Core is a powerful engine that supports a rich feature set. The core includes a CPU, memory, clocks, and configurable GPIO (General Purpose I/O).

Figure 3-1. PSoC Architecture



The M8C CPU core is a powerful processor with speeds up to 24 MHz, providing a 4 MIPS 8-bit Harvard architecture microprocessor. The CPU uses an interrupt controller with 25 vectors, to simplify programming of realtime embedded events. Program execution is timed and protected using the included Sleep and Watchdog timers (WDT).

Memory encompasses 32 KB of Flash for program storage, 2 KB of SRAM for data storage, and up to 2 KB of EEPROM emulated using Flash. Program Flash uses four protection levels on blocks of 64 bytes, enabling customized software IP protection.

The PSoC device incorporates flexible internal clock generators, including a 24 MHz IMO (internal main oscillator) accurate to 2.5 percent over temperature and voltage. The 24 MHz IMO can also be doubled to 48 MHz for the digital system use. A low power 32 kHz ILO (internal low speed oscillator) is provided for the sleep timer and WDT. If crystal accuracy is desired, the ECO (32.768 kHz external crystal oscillator) is available for use as a Real Time Clock (RTC) and can optionally generate a crystal-accurate 24 MHz system clock using a PLL. When operating the Powerline Transceiver (PLT) user module, the ECO must be selected to ensure accurate protocol timing. The clocks, together with programmable clock dividers (as a System Resource), provide the flexibility to integrate almost any timing requirement into the PSoC device.

PSoC GPIOs provide connection to the CPU, digital, and analog resources of the device. Each pin's drive mode may be selected from eight options, enabling great flexibility in external interfacing. Every pin also has the capability to generate a system interrupt on high level, low level, and change from last read.

5. Development Tools

PSoC Designer is a Microsoft® Windows-based, integrated development environment for the Programmable System-on-Chip (PSoC) devices. The PSoC Designer IDE runs on Windows XP or Windows Vista.

This system provides design database management by project, an integrated debugger with In-Circuit Emulator, in-system programming support, and built in support for third party assemblers and C compilers.

PSoC Designer also supports C language compilers developed specifically for the devices in the PSoC family.

5.1 PSoC Designer Software Subsystems

5.1.1 System-Level View

A drag-and-drop visual embedded system design environment based on PSoC Express. In the system level view you create a model of your system inputs, outputs, and communication interfaces. You define when and how an output device changes state based upon any or all other system devices. Based upon the design, PSoC Designer automatically selects one or more PSoC Programmable System-on-Chip Controllers that match your system requirements.

PSoC Designer generates all embedded code, then compiles and links it into a programming file for a specific PSoC device.

5.1.2 Chip-Level View

The chip-level view is a more traditional integrated development environment (IDE) based on PSoC Designer 4.4. Choose a base device to work with and then select different onboard analog and digital components called user modules that use the PSoC blocks. Examples of user modules are ADCs, DACs, Amplifiers, and Filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The device editor also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic configuration allows for changing configurations at run time.

5.1.3 Hybrid Designs

You can begin in the system-level view, allow it to choose and configure your user modules, routing, and generate code, then switch to the chip-level view to gain complete control over on-chip resources. All views of the project share a common code editor, builder, and common debug, emulation, and programming tools.

5.1.4 Code Generation Tools

PSoC Designer supports multiple third party C compilers and assemblers. The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. The choice is yours.

Assemblers. The assemblers allow assembly code to merge seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices.

The optimizing C compilers provide all the features of C tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

5.1.5 Debugger

The PSoC Designer Debugger subsystem provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow the designer to read and program and read and write data memory, read and write IO registers, read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows the designer to create a trace buffer of registers and memory locations of interest.

5.1.6 Online Help System

The online help system displays online, context-sensitive help for the user. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer in getting started.

5.2 In-Circuit Emulator (ICE)

A low cost, high functionality In-Circuit Emulator (ICE) is available for development support. This hardware has the capability to program single devices.

The emulator consists of a base unit that connects to the PC by way of a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full speed (24 MHz) operation.

7. Document Conventions

7.1 Acronyms Used

This table lists the acronyms used in this data sheet.

Table 7-1. Acronyms

Acronym	Description
AC	alternating current
ADC	analog-to-digital converter
API	application programming interface
CPU	central processing unit
CT	continuous time
DAC	digital-to-analog converter
DC	direct current
EEPROM	electrically erasable programmable read-only memory
FSR	full scale range
GPIO	general purpose IO
ICE	in-circuit emulator
IDE	integrated development environment
IO	input/output
ISSP	in-system serial programming
IPOR	imprecise power on reset
LSb	least-significant bit
LVD	low voltage detect
MSb	most-significant bit
PC	program counter
PGA	programmable gain amplifier
POR	power on reset
PPOR	precision power on reset
PSoC®	Programmable System-on-Chip
PWM	pulse width modulator
ROM	read only memory
SC	switched capacitor
SRAM	static random access memory

7.2 Units of Measure

A units of measure table is located in the section Electrical Specifications on page 25.

7.3 Numeric Naming

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexadecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (for example, 01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’, ‘b’, or 0x are decimal.

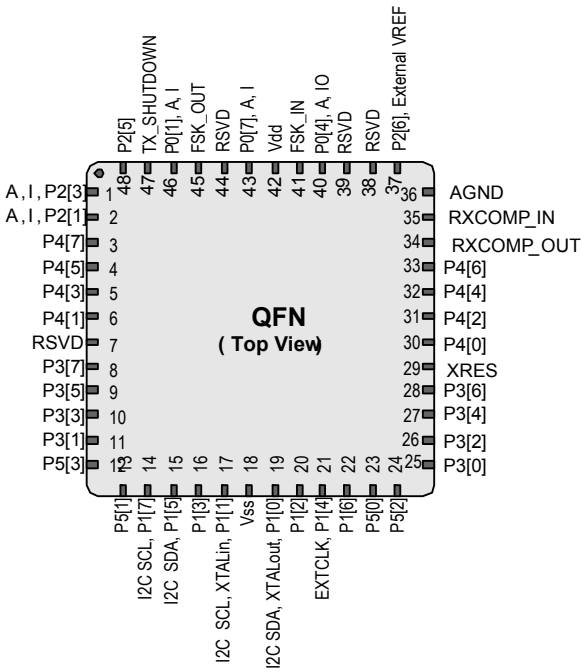
8.1 48-Pin Part Pinout

Table 8-2. 48-Pin Part Pinout (QFN)[3]

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	IO	I	P2[3]	Direct switched capacitor block input
2	IO	I	P2[1]	Direct switched capacitor block input
3	IO		P4[7]	
4	IO		P4[5]	
5	IO		P4[3]	
6	IO		P4[1]	
7	Reserved		RSVD	Reserved
8	IO		P3[7]	
9	IO		P3[5]	
10	IO		P3[3]	
11	IO		P3[1]	
12	IO		P5[3]	
13	IO		P5[1]	
14	IO		P1[7]	I2C Serial Clock (SCL)
15	IO		P1[5]	I2C Serial Data (SDA)
16	IO		P1[3]	XTAL_STABILITY. Connect a 0.1 uF capacitor between the pin and VSS.
17	IO		P1[1]	Crystal (XTALin)[2], I2C Serial Clock (SCL), ISSP-SCLK[1]
18	Power		Vss	Ground connection.
19	IO		P1[0]	Crystal (XTALout)[2], I2C Serial Data (SDA), ISSP-SDATA[1]
20	IO		P1[2]	
21	IO		P1[4]	Optional External Clock Input (EXTCLK)[2]
22	IO		P1[6]	
23	IO		P5[0]	
24	IO		P5[2]	
25	IO		P3[0]	
26	IO		P3[2]	
27	IO		P3[4]	
28	IO		P3[6]	
29	Input		XRES	Active high external reset with internal pull down
30	IO		P4[0]	
31	IO		P4[2]	
32	IO		P4[4]	
33	IO		P4[6]	
34		O	RXCOMP_OUT	Analog Output to external Low Pass Filter Circuitry
35		I	RXCOMP_IN	Analog Input from external Low Pass Filter Circuitry
36	Analog Ground		AGND	Analog Ground
37	IO		P2[6]	External Voltage Reference (VREF)
38	Reserved		RSVD	Reserved
39	Reserved		RSVD	Reserved
40	IO	IO	P0[4]	Analog column mux input and column output
41		I	FSK_IN	Analog FSK Input
42	Power		Vdd	Supply Voltage
43	IO	I	P0[7]	Analog column mux input
44	Reserved		RSVD	Reserved
45		O	FSK_OUT]	Analog FSK Output
46	IO	I	P0[1]	Analog column mux input
47	O		TX_SHUTDOWN	Output to disable transmit circuitry in receive mode Logic '0' - When the Modem is transmitting Logic '1' - When the Modem is not transmitting
48	IO		P2[5]	

LEGEND: A = Analog, I = Input, O = Output, and RSVD = Reserved (should be left unconnected).

Figure 8-2. CY8CLED16P01 48-Pin PLC Device



Note
3. The QFN package has a center pad that must be connected to ground (Vss).

8.1 100-Pin Part Pinout (On-Chip Debug)

The 100-pin TQFP part is for the CY8CLED16P01-OCD On-Chip Debug PLC device. Note that the OCD parts are only used for in-circuit debugging. OCD parts are not available for production.

Table 8-3. 100-Pin OCD Part Pinout (TQFP)

Pin No.	Digital	Analog	Name	Description	Pin No.	Digital	Analog	Name	Description
1			NC	No Connection	51			NC	No Connection
2			NC	No Connection	52	IO		P5[0]	
3	IO	I	P0[1]	Analog Column Mux Input	53	IO		P5[2]	
4	O		TX_SHUTDOWN	Output to disable transmit circuitry in receive mode Logic '0' - When the Modem is transmitting Logic '1' - When the Modem is not transmitting	54	IO		P5[4]	
5	IO		P2[5]		55	IO		P5[6]	
6	IO	I	P2[3]	Direct switched capacitor block input	56	IO		P3[0]	
7	IO	I	P2[1]	Direct switched capacitor block input	57	IO		P3[2]	
8	IO		P4[7]		58	IO		P3[4]	
9	IO		P4[5]		59	IO		P3[6]	
10	IO		P4[3]		60			HCLK	OCD high speed clock output
11	IO		P4[1]		61			CCLK	OCD CPU clock output
12			OCDE	OCD even data I/O	62	Input		XRES	Active high pin reset with internal pull down
13			OCDO	OCD odd data output	63	IO		P4[0]	
14	Reserved		RSVD	Reserved	64	IO		P4[2]	
15	Power		Vss	Ground Connection	65	Power		Vss	Ground Connection
16	IO		P3[7]		66	IO		P4[4]	
17	IO		P3[5]		67	IO		P4[6]	
18	IO		P3[3]		68		O	RXCOMP_OUT	Analog Output to external Low Pass Filter Circuitry
19	IO		P3[1]		69		I	RXCOMP_IN	Analog Input from external Low Pass Filter Circuitry
20	IO		P5[7]		70	Ground		AGND	Analog Ground
21	IO		P5[5]		71			NC	No Connection
22	IO		P5[3]		72	IO		P2[6]	External Voltage Reference (VREF) input
23	IO		P5[1]		73			NC	No Connection
24	IO		P1[7]	I2C Serial Clock (SCL)	74	Reserved		RSVD	Reserved
25			NC	No Connection	75			NC	No Connection
26			NC	No Connection	76			NC	No Connection
27			NC	No Connection	77	Reserved		RSVD	Reserved
28	IO		P1[5]	I2C Serial Data (SDA)	78			NC	No Connection
29	IO		P1[3]	I_{FMTEST}, XTAL_STABILITY. Connect a 0.1 uF capacitor between the pin and VSS.	79	IO	IO	P0[4]	Analog column mux input and column output, VREF
30	IO		P1[1]*	Crystal (XTALin)[2], I2C Serial Clock (SCL), TC SCLK	80			NC	No Connection
31			NC	No Connection	81		I	FSK_IN	Analog FSK Input
32	Power		Vdd	Supply Voltage	82	Power		Vdd	Supply Voltage
33			NC	No Connection	83	Power		Vdd	Supply Voltage
34	Power		Vss	Ground Connection	84	Power		Vss	Ground Connection
35			NC	No Connection	85	Power		Vss	Ground Connection
36	IO		P7[7]		86	IO		P6[0]	
37	IO		P7[6]		87	IO		P6[1]	
38	IO		P7[5]		88	IO		P6[2]	
39	IO		P7[4]		89	IO		P6[3]	
40	IO		P7[3]		90	IO		P6[4]	
41	IO		P7[2]		91	IO		P6[5]	
42	IO		P7[1]		92	IO		P6[6]	
43	IO		P7[0]		93	IO		P6[7]	
44	IO		P1[0]*	Crystal (XTALout)[2], I2C Serial Data (SDA), TC SDATA	94			NC	No Connection
45	IO		P1[2]	V_{FMTEST}	95	IO	I	P0[7]	Analog Column Mux Input
46	IO		P1[4]	Optional External Clock Input (EXTCLK)[2]	96			NC	No Connection
47	IO		P1[6]		97	Reserved		RSVD	Reserved
48			NC	No Connection	98			NC	No Connection
49			NC	No Connection	99		O	FSK_OUT	Analog FSK Output
50			NC	No Connection	100			NC	No Connection

LEGEND A = Analog, I = Input, O = Output, NC = No Connection, TC/TM: Test, TC/TM: Test, RSVD = Reserved (should be left unconnected).

9. Register Reference

This section lists the registers of the CY8CLED16P01 PLC device. For detailed register information, refer to the *PLC Technical Reference Manual*.

9.1 Register Conventions

The register conventions specific to this section are listed in the following table.

Convention	Description
R	Read register or bit(s)
W	Write register or bit(s)
L	Logical register or bit(s)
C	Clearable register or bit(s)
#	Access is bit specific

9.2 Register Mapping Tables

The CY8CLEDP01 device has a total register address space of 512 bytes. The register space is referred to as I/O space and is divided into two banks. The XOI bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XOI bit is set the user is in Bank 1.

Note In the following register mapping tables, blank fields are reserved and should not be accessed.

Table 9-1. Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW	DBB20DR0	40	#	ASC10CR0	80	RW	RDI2RI	C0	RW
PRT0IE	01	RW	DBB20DR1	41	W	ASC10CR1	81	RW	RDI2SYN	C1	RW
PRT0GS	02	RW	DBB20DR2	42	RW	ASC10CR2	82	RW	RDI2IS	C2	RW
PRT0DM2	03	RW	DBB20CR0	43	#	ASC10CR3	83	RW	RDI2LT0	C3	RW
PRT1DR	04	RW	DBB21DR0	44	#	ASD11CR0	84	RW	RDI2LT1	C4	RW
PRT1IE	05	RW	DBB21DR1	45	W	ASD11CR1	85	RW	RDI2RO0	C5	RW
PRT1GS	06	RW	DBB21DR2	46	RW	ASD11CR2	86	RW	RDI2RO1	C6	RW
PRT1DM2	07	RW	DBB21CR0	47	#	ASD11CR3	87	RW		C7	
PRT2DR	08	RW	DCB22DR0	48	#	ASC12CR0	88	RW	RDI3RI	C8	RW
PRT2IE	09	RW	DCB22DR1	49	W	ASC12CR1	89	RW	RDI3SYN	C9	RW
PRT2GS	0A	RW	DCB22DR2	4A	RW	ASC12CR2	8A	RW	RDI3IS	CA	RW
PRT2DM2	0B	RW	DCB22CR0	4B	#	ASC12CR3	8B	RW	RDI3LT0	CB	RW
PRT3DR	0C	RW	DCB23DR0	4C	#	ASD13CR0	8C	RW	RDI3LT1	CC	RW
PRT3IE	0D	RW	DCB23DR1	4D	W	ASD13CR1	8D	RW	RDI3RO0	CD	RW
PRT3GS	0E	RW	DCB23DR2	4E	RW	ASD13CR2	8E	RW	RDI3RO1	CE	RW
PRT3DM2	0F	RW	DCB23CR0	4F	#	ASD13CR3	8F	RW		CF	
PRT4DR	10	RW	DBB30DR0	50	#	ASD20CR0	90	RW	CUR_PP	D0	RW
PRT4IE	11	RW	DBB30DR1	51	W	ASD20CR1	91	RW	STK_PP	D1	RW
PRT4GS	12	RW	DBB30DR2	52	RW	ASD20CR2	92	RW		D2	
PRT4DM2	13	RW	DBB30CR0	53	#	ASD20CR3	93	RW	IDX_PP	D3	RW
PRT5DR	14	RW	DBB31DR0	54	#	ASC21CR0	94	RW	MVR_PP	D4	RW
PRT5IE	15	RW	DBB31DR1	55	W	ASC21CR1	95	RW	MVW_PP	D5	RW
PRT5GS	16	RW	DBB31DR2	56	RW	ASC21CR2	96	RW	I2C_CFG	D6	RW
PRT5DM2	17	RW	DBB31CR0	57	#	ASC21CR3	97	RW	I2C_SCR	D7	#
PRT6DR	18	RW	DCB32DR0	58	#	ASD22CR0	98	RW	I2C_DR	D8	RW
PRT6IE	19	RW	DCB32DR1	59	W	ASD22CR1	99	RW	I2C_MSCR	D9	#
PRT6GS	1A	RW	DCB32DR2	5A	RW	ASD22CR2	9A	RW	INT_CLR0	DA	RW
PRT6DM2	1B	RW	DCB32CR0	5B	#	ASD22CR3	9B	RW	INT_CLR1	DB	RW
PRT7DR	1C	RW	DCB33DR0	5C	#	ASC23CR0	9C	RW	INT_CLR2	DC	RW
PRT7IE	1D	RW	DCB33DR1	5D	W	ASC23CR1	9D	RW	INT_CLR3	DD	RW
PRT7GS	1E	RW	DCB33DR2	5E	RW	ASC23CR2	9E	RW	INT_MSK3	DE	RW
PRT7DM2	1F	RW	DCB33CR0	5F	#	ASC23CR3	9F	RW	INT_MSK2	DF	RW
DBB00DR0	20	#	AMX_IN	60	RW		A0		INT_MSK0	E0	RW
DBB00DR1	21	W		61			A1		INT_MSK1	E1	RW
DBB00DR2	22	RW		62			A2		INT_VC	E2	RC
DBB00CR0	23	#	ARF_CR	63	RW		A3		RES_WDT	E3	W
DBB01DR0	24	#	CMP_CR0	64	#		A4		DEC_DH	E4	RC
DBB01DR1	25	W	ASY_CR	65	#		A5		DEC_DL	E5	RC
DBB01DR2	26	RW	CMP_CR1	66	RW		A6		DEC_CR0	E6	RW
DBB01CR0	27	#		67			A7		DEC_CR1	E7	RW
DCB02DR0	28	#		68		MUL1_X	A8	W	MUL0_X	E8	W
DCB02DR1	29	W		69		MUL1_Y	A9	W	MUL0_Y	E9	W

Blank fields are Reserved and should not be accessed. # Access is bit specific.

10. Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8CLED16P01 device. For the most up to date electrical specifications, confirm that you have the most recent data sheet by going to the web at http://www.cypress.com.

Specifications are valid for -40°C ≤ T_A ≤ 85°C and T_J ≤ 100°C, except where noted.

The following table lists the units of measure that are used in this section.

Table 10-1. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
°C	degrees Celsius	µW	microwatts
dB	decibels	mA	milliamperes
fF	femtofarads	ms	milliseconds
Hz	hertz	mV	millivolts
KB	1024 bytes	nA	nanoamperes
Kbit	1024 bits	ns	nanoseconds
kHz	kilohertz	nV	nanovolts
kΩ	kilohms	Ω	ohms
MHz	megahertz	pA	picoamperes
MΩ	megaohms	pF	picofarads
µA	microamperes	pp	peak-to-peak
µF	microfarads	ppm	parts per million
µH	microhenrys	ps	picoseconds
µs	microseconds	sps	samples per second
µV	microvolts	σ	sigma: one standard deviation
µVrms	microvolts root-mean-square	V	volts

10.1 Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 10-2. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units	Notes
T_{STG}	Storage Temperature	-55	25	+100	°C	Higher storage temperatures reduce data retention time. Recommended storage temperature is +25°C ± 25°C. Extended duration storage temperatures above 65°C degrade reliability.
T_A	Ambient Temperature with Power Applied	-40	–	+85	°C	
Vdd	Supply Voltage on Vdd Relative to Vss	-0.5	–	+6.0	V	
V_{IO}	DC Input Voltage	Vss - 0.5	–	Vdd + 0.5	V	
V_{IOZ}	DC Voltage Applied to Tri-state	Vss - 0.5	–	Vdd + 0.5	V	
I_{MIO}	Maximum Current into any Port Pin	-25	–	+50	mA	
I_{MAIO}	Maximum Current into any Port Pin Configured as Analog Driver	-50	–	+50	mA	
ESD	Electro Static Discharge Voltage	2000	–	–	V	Human Body Model ESD
LU	Latch-up Current	–	–	200	mA	

10.2 Operating Temperature

Table 10-3. Operating Temperature

Symbol	Description	Min	Typ	Max	Units	Notes
T_A	Ambient Temperature	-40	–	+85	°C	
T_J	Junction Temperature	-40	–	+100	°C	The temperature rise from ambient to junction is package specific. See Thermal Impedances on page 41. The user must limit the power consumption to comply with this requirement.

10.3 DC Electrical Characteristics

10.3.1 DC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 10-4. DC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
Vdd	Supply Voltage	4.75	–	5.25	V	
I_{DD}	Supply Current	–	8	14	mA	Conditions are 5.0V, T_A = 25°C, CPU = 3 MHz, SYSCLK doubler disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 0.366 kHz.
V_{REF}	Reference Voltage (Bandgap)	1.28	1.3	1.32	V	Trimmed for appropriate Vdd.

10.3.2 DC General Purpose IO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature range: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 10-5. DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull Up Resistor	4	5.6	8	kΩ	
R_{PD}	Pull Down Resistor	4	5.6	8	kΩ	
V_{OH}	High Output Level	Vdd - 1.0	–	–	V	IOH = 10 mA, (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 80 mA maximum combined IOH budget.
V_{OL}	Low Output Level	–	–	0.75	V	IOL = 25 mA, (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 150 mA maximum combined IOL budget.
I_{OH}	High Level Source Current	10	–	–	mA	VOH = Vdd-1.0V, see the limitations of the total current in the note for VOH
I_{OL}	Low Level Source Current	25	–	–	mA	VOL = 0.75V, see the limitations of the total current in the note for VOL
V_{IL}	Input Low Level	–	–	0.8	V	
V_{IH}	Input High Level	2.1	–		V	
V_H	Input Hysterisis	–	60	–	mV	
I_{IL}	Input Leakage (Absolute Value)	–	1	–	nA	Gross tested to 1 μA.
C_{IN}	Capacitive Load on Pins as Input	–	3.5	10	pF	Package and pin dependent. Temp = 25°C.
C_{OUT}	Capacitive Load on Pins as Output	–	3.5	10	pF	Package and pin dependent. Temp = 25°C.

10.3.3 DC Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

The Operational Amplifier is a component of both the Analog Continuous Time PSoC blocks and the Analog Switched Capacitor PSoC blocks. The guaranteed specifications are measured in the Analog Continuous Time PSoC block. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 10-6. 5V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input Offset Voltage (Absolute Value) Power = Low, Opamp Bias = High Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 – – –	 1.6 1.3 1.2	 10 8 7.5	 mV mV mV	
TCV_{OSOA}	Average Input Offset Voltage Drift	–	7.0	35.0	µV/°C	
I_{EBOA}	Input Leakage Current (Port 0 Analog Pins)	–	200	–	pA	Gross tested to 1 µA.
C_{INOA}	Input Capacitance (Port 0 Analog Pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25°C.
V_{CMOA}	Common Mode Voltage Range. All cases, except highest. Power = High, Opamp Bias = High	0.0 0.5	– –	Vdd Vdd - 0.5	V V	
$CMRR_{OA}$	Common Mode Rejection Ratio	60	–	–	dB	
G_{OLOA}	Open Loop Gain	80	–	–	dB	
$V_{OHIGHOA}$	High Output Voltage Swing (Internal Signals)	Vdd - 0.01	–	–	V	
V_{OLOWOA}	Low Output Voltage Swing (Internal Signals)	–	–	0.1	V	
I_{SOA}	Supply Current (including associated AGND buffer) Power = Low, Opamp Bias = Low Power = Low, Opamp Bias = High Power = Medium, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = Low Power = High, Opamp Bias = High	 – – – – – –	 150 300 600 1200 2400 4600	 200 400 800 1600 3200 6400	 µA µA µA µA µA µA	
$PSRR_{OA}$	Supply Voltage Rejection Ratio	67	80	–	dB	Vss ≤ VIN ≤ (Vdd - 2.25) or (Vdd - 1.25V) ≤ VIN ≤ Vdd.

10.3.4 DC Low Power Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 10-7. DC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{REFLPC}	Low Power Comparator (LPC) Reference Voltage Range	0.2	–	Vdd - 1	V	
I_{SLPC}	LPC Supply Current	–	10	40	µA	
V_{OSLPC}	LPC Voltage Offset	–	2.5	30	mV	

Table 10-9. 5V DC Analog Reference Specifications (continued)

Symbol	Description	Min	Typ	Max	Units
–	RefHi = 2 x Bandgap	2.50	2.60	2.70	V
–	RefHi = 3.2 x Bandgap	4.02	4.16	4.29	V
–	RefLo = Bandgap	BG - 0.082	BG + 0.023	BG + 0.129	V
–	RefLo = 2 x Bandgap - P2[6] (P2[6] = 1.3V)	2 x BG - P2[6] - 0.084	2 x BG - P2[6] + 0.025	2 x BG - P2[6] + 0.134	V
–	RefLo = P2[4] – Bandgap (P2[4] = Vdd/2)	P2[4] - BG - 0.056	P2[4] - BG + 0.026	P2[4] - BG + 0.107	V
–	RefLo = P2[4]-P2[6] (P2[4] = Vdd/2, P2[6] = 1.3V)	P2[4] - P2[6] - 0.057	P2[4] - P2[6] + 0.026	P2[4] - P2[6] + 0.110	V

10.3.7 DC Analog PSoC Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 10-10. DC Analog PSoC Block Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{CT}	Resistor Unit Value (Continuous Time)	–	12.2	–	kΩ	
C_{SC}	Capacitor Unit Value (Switch Cap)	–	80	–	fF	

10.3.8 DC POR and LVD Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C = TA = 85°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 10-11. DC POR and LVD Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
VPPOR2R	Vdd Value for PPOR Trip (positive ramp) PORLEV[1:0] = 10b	–	4.55	–	V	
VPPOR2	Vdd Value for PPOR Trip (negative ramp) PORLEV[1:0] = 10b	–	4.55	–	V	
VPH2	PPOR Hysteresis PORLEV[1:0] = 10b	–	0	–	mV	
VLVD6 VLVD7	Vdd Value for LVD Trip VM[2:0] = 110b VM[2:0] = 111b	4.63 4.72	4.73 4.81	4.82 4.91	V V	

10.3.9 DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 10-12. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
I_{DDP}	Supply Current During Programming or Verify	–	10	30	mA	
V_{ILP}	Input Low Voltage During Programming or Verify	–	–	0.8	V	
V_{IHP}	Input High Voltage During Programming or Verify	2.2	–	–	V	
I_{ILP}	Input Current when Applying V_{ILP} to P1[0] or P1[1] During Programming or Verify	–	–	0.2	mA	Driving internal pull down resistor
I_{IHP}	Input Current when Applying V_{IHP} to P1[0] or P1[1] During Programming or Verify	–	–	1.5	mA	Driving internal pull down resistor
V_{OLV}	Output Low Voltage During Programming or Verify	–	–	Vss + 0.75	V	
V_{OHV}	Output High Voltage During Programming or Verify	Vdd - 1.0	–	Vdd	V	
$Flash_{ENPB}$	Flash Endurance (per block)	50,000	–	–	–	Erase/write cycles per block
$Flash_{ENT}$	Flash Endurance (total)[5]	1,800,000	–	–	–	Erase/write cycles
$Flash_{DR}$	Flash Data Retention	10	–	–	Years	

10.4 AC Electrical Characteristics

10.4.1 AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

Note See the individual user module data sheets for information on maximum frequencies for user modules.

Table 10-13. AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{IMO24}	Internal Main Oscillator Frequency for 24 MHz	23.4	24	24.6	MHz	Trimmed for 5V operation using factory trim values. SLIMO Mode = 0.
F_{IMO6}	Internal Main Oscillator Frequency for 6 MHz	5.5	6	6.5[6]	MHz	Trimmed for 5V operation using factory trim values. SLIMO Mode = 1.
F_{CPU1}	CPU Frequency (5V Nominal)	0.93	24	24.6[6]	MHz	
F_{48M}	Digital PSoC Block Frequency	0	48	49.2[6, 7]	MHz	Refer to the AC Digital Block Specifications below.
F_{32K1}	Internal Low Speed Oscillator Frequency	15	32	64	kHz	
F_{32K2}	External Crystal Oscillator	–	32.768	–	kHz	Accuracy is capacitor and crystal dependent. 50% duty cycle.

Notes
5. A maximum of 36 x 50,000 block endurance cycles is allowed. This may be balanced between operations on 36x1 blocks of 50,000 maximum cycles each, 36x2 blocks of 25,000 maximum cycles each, or 36x4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36x50,000 and that no single block ever sees more than 50,000 cycles). For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 at http://www.cypress.com under Application Notes for more information.
6. Accuracy derived from Internal Main Oscillator with appropriate trim for Vdd range.
7. See the individual user module data sheets for information on maximum frequencies for user modules.

Table 10-13. AC Chip-Level Specifications (continued)

Symbol	Description	Min	Typ	Max	Units	Notes
F_{32K_U}	Internal Low Speed Oscillator (ILO) Untrimmed Frequency	5	–	–	kHz	After a reset and before the m8c starts to run, the ILO is not trimmed. See the System Resets section of the PSoC Technical Reference Manual for details on timing this.
F_{PLL}	PLL Frequency	–	23.986	–	MHz	A multiple (x732) of crystal frequency.
Jitter24M2	24 MHz Period Jitter (PLL)	–	–	600	ps	
$T_{PLLSLEW}$	PLL Lock Time	0.5	–	10	ms	
$T_{PLLSLEWLOW}$	PLL Lock Time for Low Gain Setting	0.5	–	50	ms	
T_{OS}	External Crystal Oscillator Startup to 1%	–	250	500	ms	
T_{OSACC}	External Crystal Oscillator Startup to 100 ppm	–	300	600	ms	The crystal oscillator frequency is within 100 ppm of its final value by the end of the T_{OSACC} period. Correct operation assumes a properly loaded 1 µW maximum drive level 32.768 kHz crystal. -40°C ≤ T_A ≤ 85°C.
Jitter32k	32 kHz Period Jitter	–	100		ns	
T_{XRST}	External Reset Pulse Width	10	–	–	µs	
DC24M	24 MHz Duty Cycle	40	50	60	%	
DC_{ILO}	Internal Low Speed Oscillator Duty Cycle	20	50	80	%	
Step24M	24 MHz Trim Step Size	–	50	–	kHz	
Fout48M	48 MHz Output Frequency	46.8	48.0	49.2	MHz	Trimmed using factory trim values.
Jitter24M1	24 MHz Period Jitter (IMO)	–	600		ps	
F_{MAX}	Maximum frequency of signal on row input or row output.	–	–	12.3	MHz	
SR_{POWER_UP}	Power Supply Slew Rate	–	–	250	V/ms	Vdd slew rate during power up.
$T_{POWERUP}$	Time from end of POR to CPU executing code	–	16	100	ms	Power up from 0V. See the System Resets section of the PSoC Technical Reference Manual.

Figure 10-1. PLL Lock Timing Diagram

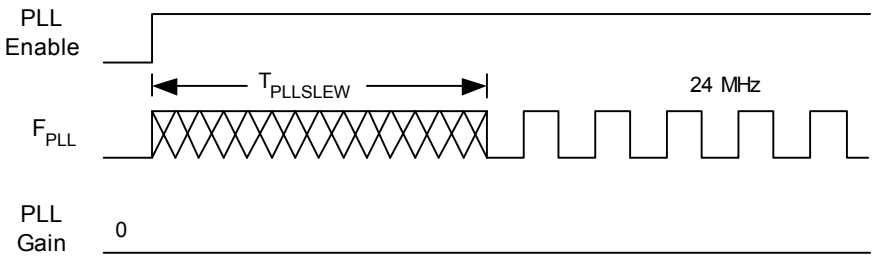
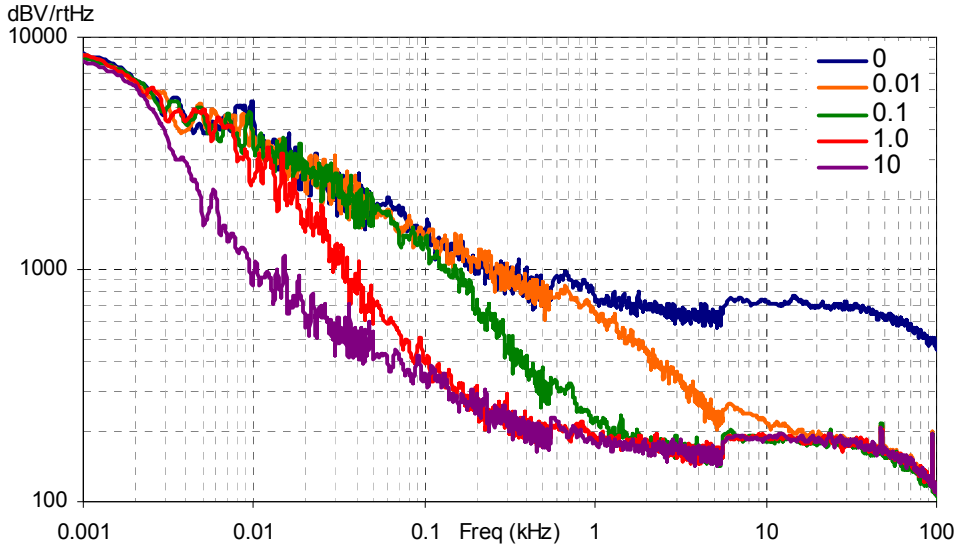
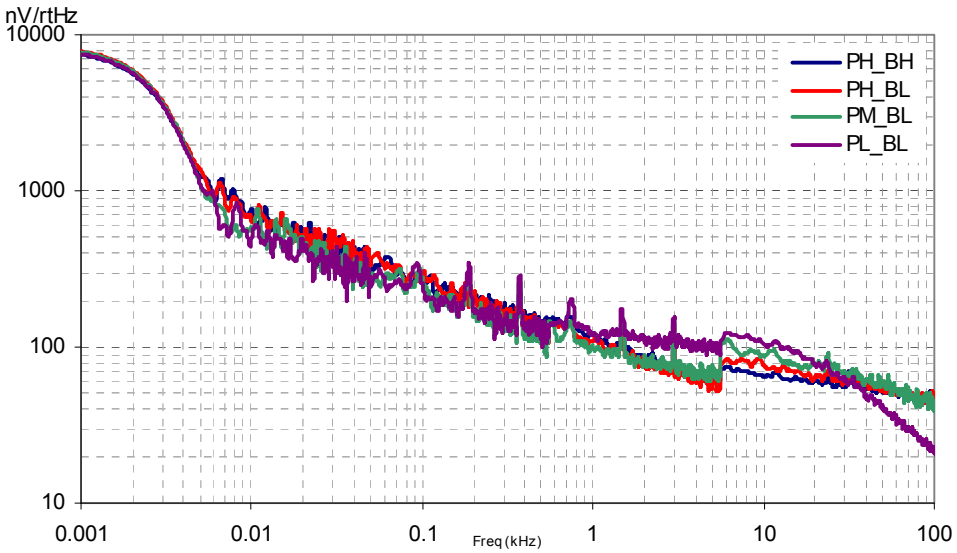


Figure 10-7. Typical AGND Noise with P2[4] Bypass



At low frequencies, the opamp noise is proportional to 1/f, power independent, and determined by device geometry. At high frequencies, increased power level reduces the noise spectrum level.

Figure 10-8. Typical Opamp Noise



10.4.4 AC Low Power Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 10-16. AC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{RLPC}	LPC response time	–	–	50	µs	≥ 50 mV overdrive comparator reference set within V_{REFLPC}.

10.4.5 AC Digital Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 10-17. AC Digital Block Specifications

Function	Description	Min	Typ	Max	Units	Notes
All Functions	Maximum Block Clocking Frequency			49.2	MHz	
Timer	Capture Pulse Width	50[9]	–	–	ns	
	Maximum Frequency, No Capture	–	–	49.2	MHz	
	Maximum Frequency, With Capture	–	–	24.6	MHz	
Counter	Enable Pulse Width	50[9]	–	–	ns	
	Maximum Frequency, No Enable Input	–	–	49.2	MHz	
	Maximum Frequency, Enable Input	–	–	24.6	MHz	
Dead Band	Kill Pulse Width:					
	Asynchronous Restart Mode	20	–	–	ns	
	Synchronous Restart Mode	50[9]	–	–	ns	
	Disable Mode	50[9]	–	–	ns	
	Maximum Frequency	–	–	49.2	MHz	
CRCPRS (PRS Mode)	Maximum Input Clock Frequency	–	–	49.2	MHz	
CRCPRS (CRC Mode)	Maximum Input Clock Frequency	–	–	24.6	MHz	
SPIM	Maximum Input Clock Frequency	–	–	8.2	MHz	Maximum data rate at 4.1 MHz due to 2 x over clocking.
SPIS	Maximum Input Clock Frequency	–	–	4.1	MHz	
	Width of SS_ Negated Between Transmissions	50[8]	–	–	ns	
Transmitter	Maximum Input Clock Frequency Vdd ≥ 4.75V, 2 Stop Bits	– –	– –	24.6 49.2	MHz MHz	Maximum data rate at 3.08 MHz due to 8 x over clocking. Maximum data rate at 6.15 MHz due to 8 x over clocking.
Receiver	Maximum Input Clock Frequency Vdd ≥ 4.75V, 2 Stop Bits	– –	– –	24.6 49.2	MHz MHz	Maximum data rate at 3.08 MHz due to 8 x over clocking. Maximum data rate at 6.15 MHz due to 8 x over clocking.

Note
8. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).

11. Packaging Information

This section illustrates the packaging specifications for the CY8CLED16P01 PLC device, along with the thermal impedances for each package, and the typical package capacitance on crystal pins.

Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the document titled *PSoC Emulator Pod Dimensions* at http://www.cypress.com/design/MR10161.

11.1 Packaging Dimensions

Figure 11-1. 28-Pin (210-Mil) SSOP

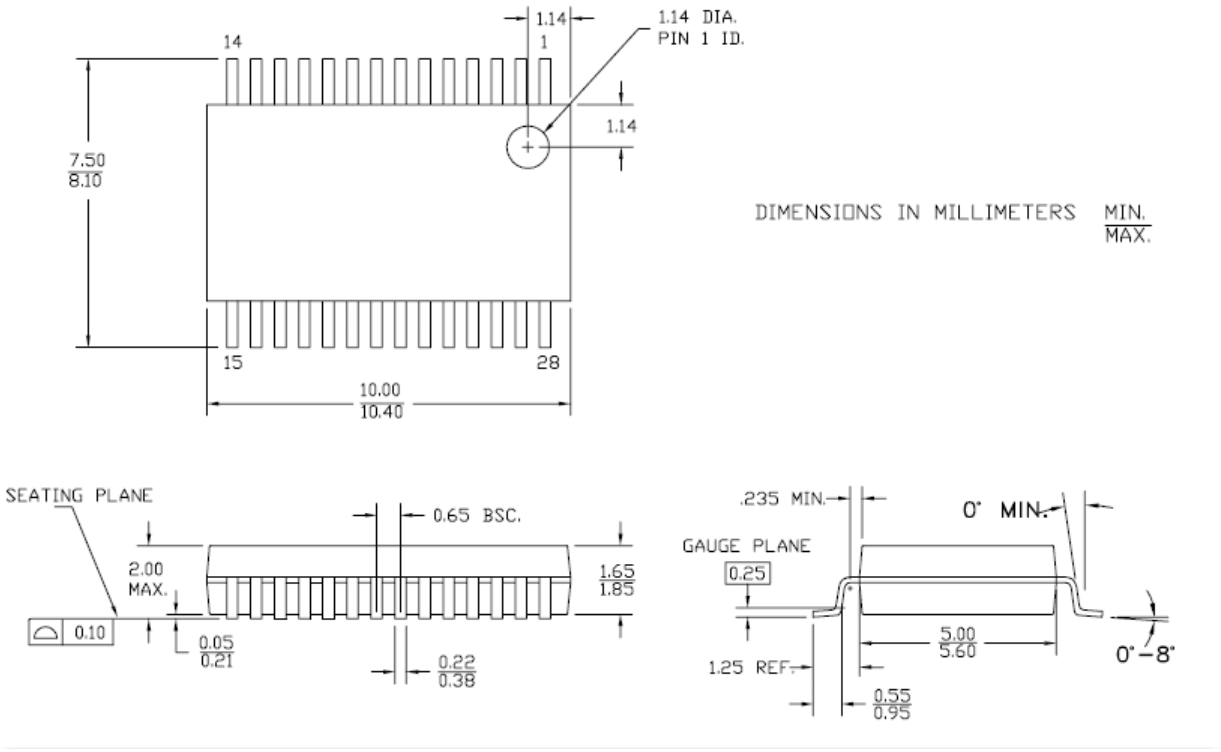


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Figure 11-3. 48-Pin QFN 7x7x 0.90 MM (Sawn Type)

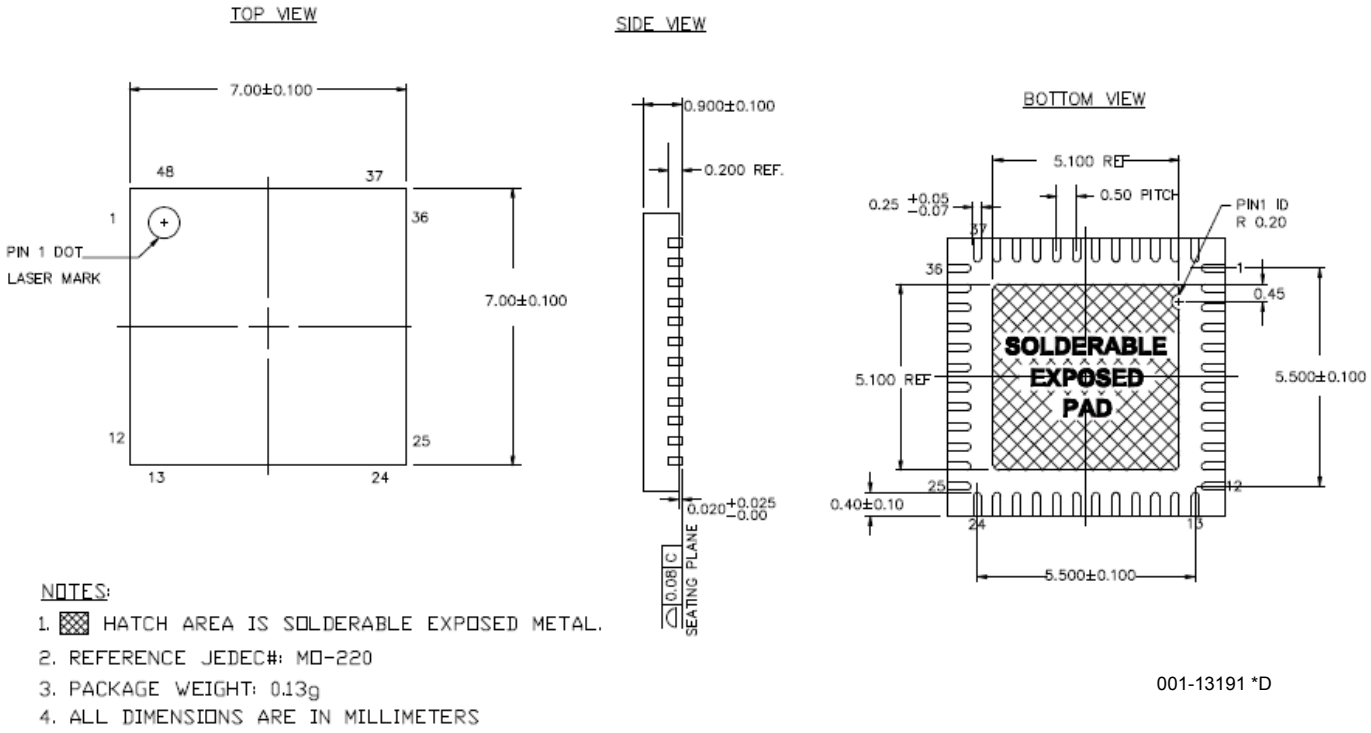
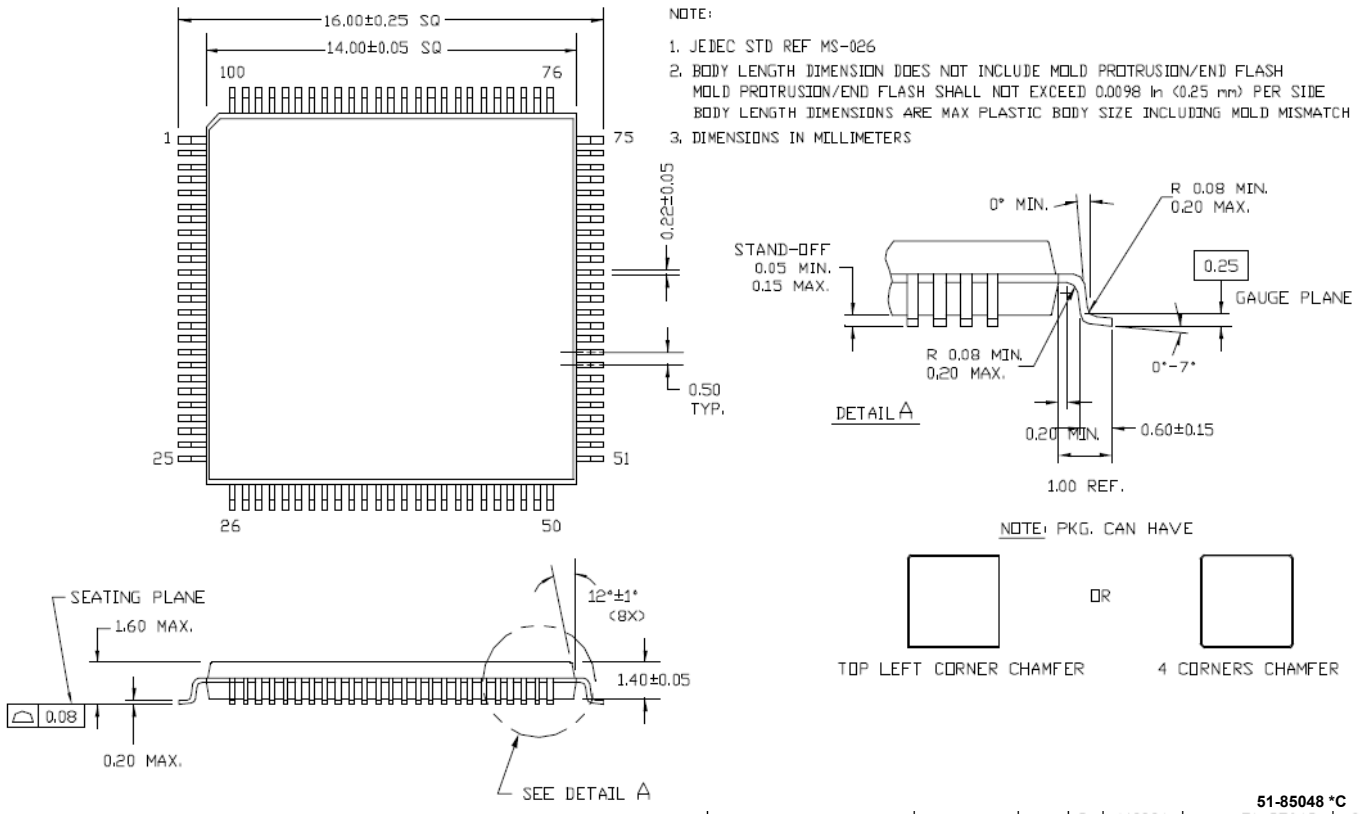


Figure 11-4. 100-Pin TQFP



11.1 Thermal Impedances

Table 11-1. Thermal Impedances per Package

Package	Typical θ_{JA}[11]
28 SSOP	94°C/W
48 QFN[12]	28°C/W
100 TQFP	50°C/W

11.2 Capacitance on Crystal Pins

Table 11-2. Typical Package Capacitance on Crystal Pins

Package	Package Capacitance
28 SSOP	2.8 pF
48 QFN	1.8 pF
100 TQFP	3.1 pF

11.3 Solder Reflow Peak Temperature

Following is the minimum solder reflow peak temperature to achieve good solderability.

Table 11-3. Solder Reflow Peak Temperature

Package	Minimum Peak Temperature[13]	Maximum Peak Temperature
28 SSOP	240°C	260°C
48 QFN	220°C	260°C
100 TQFP	220°C	260°C

Notes
11. $T_J = T_A + POWER \times \theta_{JA}$
12. To achieve the thermal impedance specified for the QFN package, the center thermal pad should be soldered to the PCB ground plane.
13. Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are 220 ± 5°C with Sn-Pb or 245 ± 5°C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.

15. Document History Page

Document Title: CY8CLED16P01 Powerline Communication Solution Document Number: 001-49263				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2575716	GHH/PYRS	10/01/08	New Datasheet
*A	2731927	GHH/HMT/ DSG	07/06/09	Added - Configurable baud rates and FSK Frequencies - PLC Pod Kits for development purposes Modified - Pin information for all packages
*B	2748537	GHH	See ECN	Added Sections on ‘Getting Started’ and ‘Document Conventions’ Modified the following Electrical Parameters - FIMO6 Min: Changed from 5.75 MHz to 5.5 MHz - FIMO6 Max: Changed from 6.35 MHz to 6.5 MHz - SPIS (Maximum input clock frequency): Changed from 4.1 ns to 4.1 MHz - TWRITE (Flash Block Write Time): Changed from 40 ms to 10 ms
*C	2752799	GHH	08/17/09	Posting to external web.
*D	2759000	GHH	09/02/2009	Fixed typos in the data sheet. Updated Figure 1-2. on page 2 and Figure 3-1. on page 10.
*E	2778970	FRE	10/05/2009	Added a table for DC POR and LVD Specifications Updated DC GPIO, AC Chip-Level, and AC Programming Specifications as follows: - Modified FIMO6, TWRITE, and Power Up IMO to Switch specifications - Added IOH, IOL, DCILO, F32K_U, TPOWERUP, TERASEALL, and SRPOWER_UP specifications Added 48-Pin QFN (Sawn) package diagram and CY8CLED16P01-48LTXI and CY8CLED16P01-48LTXIT part details in the Ordering Information table Updated section 5 and Tables 10-1, 10-2, and 10-3 to state the requirement to use the external crystal for PLC protocol timing Table 10-1 and Figure 10-1: Changed pins 9 and 25 from NC to RSVD Table 10-2 and Figure 10-2: Changed pins 7 and 39 from NC to RSVD Table 10-3 and Figure 10-3: Changed pins 14 and 77 from NC to RSVD Tables 10-1, 10-2, 10-3: Added explanation to Connect a 0.1 uF capacitor between XTAL_Stability and VSS. Fixed minor typos