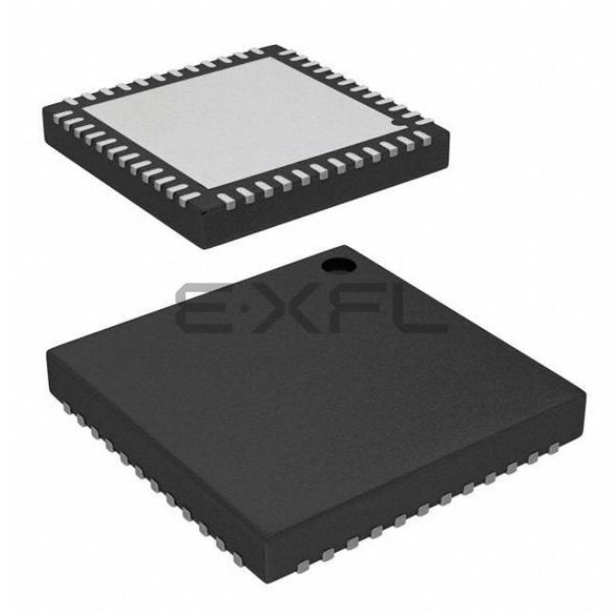

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Details	
Product Status	Obsolete
Applications	Powerline Communication
Core Processor	M8C
Program Memory Type	FLASH (32KB)
Controller Series	CY8CLED
RAM Size	2K x 8
Interface	I²C, IrDA, SPI, UART/USART
Number of I/O	44
Voltage - Supply	4.75V ~ 5.25V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8cled16p01-48lfxi

1. PLC Functional Overview

The CY8CLED16P01 is an integrated Powerline Communication (PLC) chip with the Powerline Modem PHY and Network Protocol Stack running on the same device. Apart from the PLC core, the CY8CLED16P01 also offers Cypress's revolutionary PSoC technology that enables system designers to integrate multiple functions on the same chip.

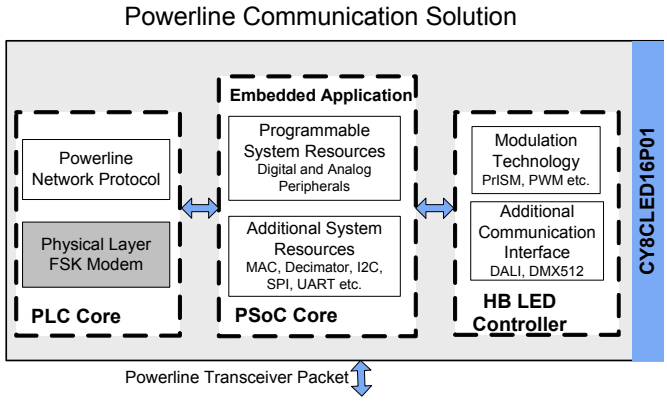
1.1 Robust Communication using Cypress's PLC Solution

Powerlines are available everywhere in the world and are a widely available communication medium for PLC technology. The pervasiveness of powerlines also makes it difficult to predict the characteristics and operation of PLC products. Because of the variable quality of powerlines around the world, implementing robust communication has been an engineering challenge for years. The Cypress PLC solution enables secure and reliable communications. Cypress PLC features that enable robust communication over powerlines include:

- Integrated Powerline PHY modem with optimized filters and amplifiers to work with lossy high voltage and low voltage powerlines.
- Powerline optimized network protocol that supports bidirectional communication with acknowledgement-based signaling. In case of data packet loss due to bursty noise on the powerline, the transmitter has the capability to retransmit data.
- The Powerline Network Protocol also supports an 8-bit CRC for error detection and data packet retransmission.
- A Carrier Sense Multiple Access (CSMA) scheme is built into the network protocol that minimizes collisions between packet transmissions on the powerline and supports multiple masters and reliable communication on a bigger network.

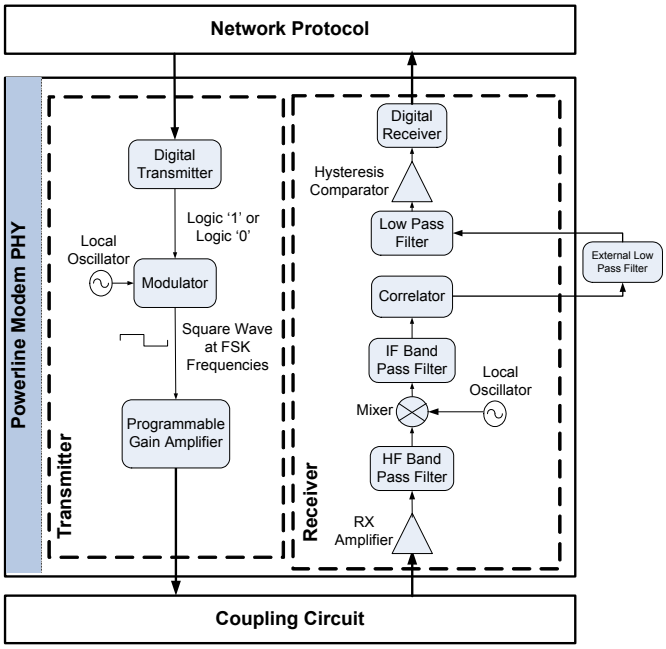
1.2 Powerline Modem PHY

Figure 1-1. Physical Layer FSK Modem



The physical layer of the Cypress PLC solution is implemented using an FSK modem that enables half duplex communication on any high voltage and low voltage powerline. This modem supports raw data rates up to 2400 bps. A block diagram is shown in Figure 1-2.

Figure 1-2. Physical Layer FSK Modem Block Diagram



1.2.1 Transmitter Section

Digital data from the network layer is serialized by the digital transmitter and fed as input to the modulator. The modulator divides the local oscillator frequency by a definite factor depending on whether the input data is high level logic '1' or low level logic '0'. It then generates a square wave at 133.3 kHz (logic '0') or 131.8 kHz (logic '1'), which is fed to the Programmable Gain Amplifier to generate FSK modulated signals. This enables tunable amplification of the signal depending on the noise in the channel. The logic '1' frequency can also be configured as 130.4 kHz for wider FSK deviation.

1.2.2 Receiver Section

The incoming FSK signal from the powerline is input to a high frequency (HF) band pass filter that filters out-of-band frequency components and outputs a filtered signal within the desired spectrum of 125 kHz to 140 kHz for further demodulation. The mixer block multiplies the filtered FSK signals with a locally generated signal to produce heterodyned frequencies.

The intermediate frequency (IF) band pass filters further remove out-of-band noise as required for further demodulation. This signal is fed to the correlator, which produces a DC component (consisting of logic '1' and '0') and a higher frequency component.

The output of the correlator is fed to a low pass filter (LPF) that outputs only the demodulated digital data at 2400 baud and suppresses all other higher frequency components generated in the correlation process. The output of the LPF is digitized by the hysteresis comparator. This eliminates the effects of correlator delay and false logic triggers due to noise. The digital receiver deserializes this data and outputs to the network layer for interpretation.

1.2.3 Coupling Circuit Reference Design

The coupling circuit couples low voltage signals from the CY8CLED16P01 to the powerline. The topology of this circuit is determined by the voltage on the powerline and design constraints mandated by powerline usage regulations.

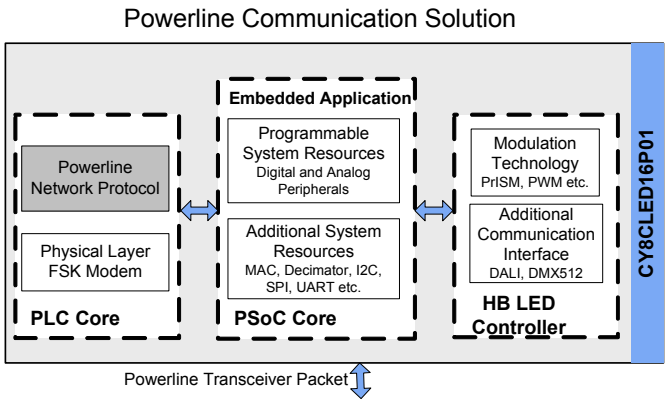
Cypress provides reference designs for a range of powerline voltages including 110V/240V AC and 12V/24V AC/DC. The CY8CLED16P01 is capable of data communication over other AC/DC Powerlines as well with the appropriate external coupling circuit. The 110V AC and 240V AC designs are compliant to the following powerline usage regulations:

- FCC Part 15 for North America
- EN 50065-1:2001 for Europe

1.3 Network Protocol

Cypress's powerline optimized network protocol performs the functions of the data link, network, and transport layers in an ISO/OSI-equivalent model.

Figure 1-3. Powerline Network Protocol



The network protocol implemented on the CY8CLED16P01 supports the following features:

- Bidirectional half duplex communication
- Master-slave or peer-to-peer network topologies
- Multiple masters on powerline network
- 8-bit logical addressing supports up to 256 powerline nodes
- 16-bit extended logical addressing supports up to 65536 powerline nodes
- 64-bit physical addressing supports up to 2^{64} powerline nodes
- Individual, broadcast or group mode addressing
- Carrier Sense Multiple Access (CSMA)
- Full control over transmission parameters
  - Acknowledged
  - Unacknowledged
  - Repeated Transmit

1.3.1 CSMA and Timing Parameters

- CSMA – The protocol provides the random selection of a period between 85 and 115 ms (out of seven possible values in this range). Within this period, the Band-In-Use (BIU) detector must indicate that the line is not in use, before attempting a transmission.
- BIU – A Band-In-Use detector, as defined under CENELEC EN 50065-1, is active whenever a signal that exceeds 86 dBμVrms anywhere in the range 131.5 kHz to 133.5 kHz is present for at least 4 ms. This threshold can be configured for different end-system applications not requiring CENELEC compliance.The modem tries to retransmit after every 85 to 115 ms when the band is in use. The transmitter times out after 1.1 seconds to 3 seconds (depending on the noise on the Powerline) and generates an interrupt to indicate that the transmitter was unable to acquire the powerline.

1.3.2 Powerline Transceiver Packet

The powerline network protocol defines a Powerline Transceiver (PLT) packet structure, which is used for data transfers between nodes across the powerline. Packet formation and data transmission across the powerline network is implemented internally in the CY8CLED16P01.

A PLT packet is divided into a variable length header (minimum 6 bytes to maximum 20 bytes, depending on address type), variable length payload (minimum 0 bytes to maximum 31 bytes), and a packet CRC byte.

This packet (preceded by a one byte preamble "0xAB") is then transmitted by the powerline modem PHY and the external coupling circuit across the powerline.

The format of the PLT packet is shown in the following table.

Table 1-1. Powerline Transceiver (PLT) Packet Structure

Byte Offset	Bit Offset							
	7	6	5	4	3	2	1	0
0x00	SA Type	DA Type		Service Type	RSVD	RSVD	Response	RSVD
0x01	Destination Address (8-Bit Logical, 16-Bit Extended Logical or 64-Bit Physical)							
0x02	Source Address (8-Bit Logical, 16-Bit Extended Logical or 64-Bit Physical)							
0x03	Command							
0x04	RSVD			Payload Length				
0x05	Seq Num				Powerline Packet Header CRC			
0x06	Payload (0 to 31 Bytes)							
	Powerline Transceiver Packet CRC							

1.3.3 Packet Header

The packet header contains the first 6 bytes of the packet when 1-byte logical addressing is used. When 8-byte physical addressing is used, the source and destination addresses each contain 8 bytes. In this case, the header can consist of a maximum of 20 bytes. Unused fields marked RSVD are for future expansion and are transmitted as bit 0. Table 1-2 describes the PLT packet header fields in detail.

Table 1-2. Powerline Transceiver (PLT) Packet Header

Field Name	No. of Bits	Tag	Description
SA Type	1	Source Address Type	0 – Logical Addressing 1 – Physical Addressing
DA Type	2	Destination Address Type	00 – Logical Addressing 01 – Group Addressing 10 – Physical Addressing 11 – Invalid
Service Type	1		0 – Unacknowledged Messaging 1 – Acknowledged Messaging
Response	1	Response	0 - Not an acknowledgement or response packet 1 - Acknowledgement or response packet
Seq Num	4	Sequence Number	4-bit unique identifier for each packet between source and destination.
Header CRC	4		4-bit CRC value. This enables the receiver to suspend receiving the rest of the packet if its header is corrupted

1.3.4 Payload

The packet payload has a length of 0 to 31 bytes. Payload content is user defined and can be read or written through I^2C.

1.3.5 Packet CRC

The last byte of the packet is an 8-bit CRC value used to check packet data integrity. This CRC calculation includes the header and payload portions of the packet and is in addition to the powerline packet header CRC.

1.3.6 Sequence Numbering

The sequence number is increased for every new unique packet transmitted. If in acknowledged mode and an acknowledgment is not received for a given packet, that packet will be re-transmitted (if TX_Retry > 0) with the same sequence number. If in unacknowledged mode, the packet will be transmitted (TX_Retry + 1) times with the same sequence number.

If the receiver receives consecutive packets from the same source address with the same sequence number and packet CRC, it does not notify the host of the reception of the duplicate packet. If in acknowledged mode, it still sends an acknowledgment so that the transmitter knows that the packet was received.

1.3.7 Addressing

The CY8CLED16P01 has three modes of addressing:

- Logical addressing: Every CY8CLED16P01 node can have either a 8-bit logical address or a 16-bit logical address. The logical address of the PLC Node is set by the local application or by a remote node on the Powerline.
- Physical addressing: Every CY8CLED16P01 has a unique 64-bit physical address.
- Group addressing: This is explained in the next section.

1.3.8 Group Membership

Group membership enables the user to multicast messages to select groups. The CY8CLED16P01 supports two types of group addressing:

- Single Group Membership – The network protocol supports up to 256 different groups on the network in this mode. In this mode, each PLC node can only be part of a single group. For example, multiple PLC nodes can be part of Group 131.
- Multiple Group Membership – The network protocol supports eight different groups in this mode and each PLC node can be a part of multiple groups. For example, a single PLC node can be a part of Group 3, Group 4, and Group 7 at the same time.

Both of these membership modes can also be used together for group membership. For example, a single PLC node can be a part of Group 131 and also multiple groups such as Group 3, Group 4, and Group 7.

The group membership ID for broadcasting messages to all nodes in the network is 0x00.

The service type is always set to Unacknowledgment Mode in Group Addressing Mode. This is to avoid acknowledgment flooding on the powerline during multicast.

1.3.9 Remote Commands

In addition to sending normal data over the Powerline, the CY8CPLC10 can also send (and request) control information to (and from) another node on the network. The type of remote command to transmit is set by the TX_CommandID register and when received, is stored in the RX_CommandID register.

When a control command (Command ID = 0x01 - 0x08 and 0x0C - 0x0F) is received, the protocol will automatically process the packet (if Lock_Configuration is '0'), respond to the initiator, and notify the host of the successful transmission and reception.

When the send data command (ID 0x09) or request for data command (ID 0x0A) is received, the protocol will reply with an acknowledgment packet (if TX_Service_Type = '1'), and notify the host of the new received data. If the initiator doesn't receive the acknowledgment packet within 500ms, it will notify the host of the no acknowledgment received condition.

When a response command (ID 0x0B) is received by the initiator within 1.5s of sending the request for data command, the protocol will notify the host of the successful transmission and reception. If the response command is not received by the initiator within 1.5s, it will notify the host of the no response received condition.

The host is notified by updating the appropriate values in the INT_Status register (including Status_Value_Change).

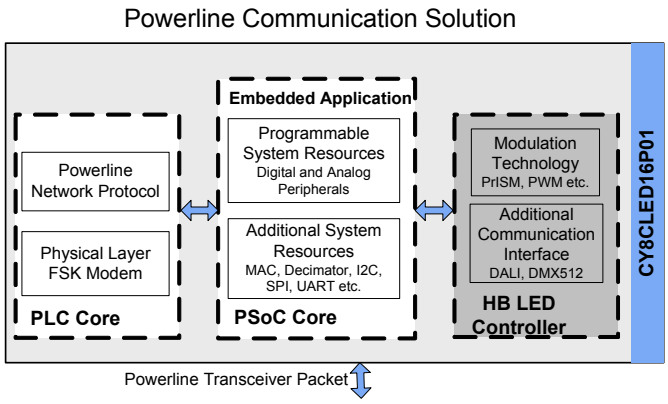
The command IDs 0x30-0xff can be used for custom commands that would be processed by the external host (e.g. set an LED color, get a temperature/voltage reading). The available remote commands are described in Table 1-3 on page 5 with the respective Command IDs.

Table 1-3. Remote Commands

Cmd ID	Command Name	Description	Payload (TX Data)	Response (RX Data)
0x01	SetRemote_TXEnable	Sets the TX Enable bit in the PLC Mode Register. Rest of the PLC Mode register is unaffected	0 - Disable Remote TX 1 - Enable Remote TX	If Remote Lock Config = 0, Response = 00 (Success) If Remote Lock Config = 1, Response = 01 (Denied)
0x03	SetRemote_ExtendedAddr	Set the Addressing to Extended Addressing Mode	0 - Disable Extended Addressing 1 - Enable Extended Addressing	If Remote Lock Config = 0, Response = 00 (Success) If Remote Lock Config = 1, Response = 01 (Denied)
0x04	SetRemote_LogicalAddr	Assigns the specified logical address to the remote PLC node	If Ext Address = 0, Payload = 8-bit Logical Address If Ext Address = 1, Payload = 16-bit Logical Address	If Remote Lock Config = 0, Response = 00 (Success) If Remote Lock Config = 1, Response = 01 (Denied)
0x05	GetRemote_LogicalAddr	Get the Logical Address of the remote PLC node	None	If Remote TX Enable = 0, Response = None If Remote TX Enable = 1, {If Ext Address = 0, Response = 8-bit Logical Address If Ext Address = 1, Response = 16-bit Logical Address}
0x06	GetRemote_PhysicalAddr	Get the Physical Address of the remote PLC node	None	If Remote TX Enable = 0, Response = None If Remote TX Enable = 1, Response = 64-bit Physical Address
0x07	GetRemote_State	Request PLC_Mode Register content from a Remote PLC node	None	If Remote TX Enable = 0, Response = None If Remote TX Enable = 1, Response = Remote PLC Mode register
0x08	GetRemote_Version	Get the Version Number of the Remote Node	None	If TX Enable = 0, Response = None If TX Enable = 1, Response = Remote Version register
0x09	SendRemote_Data	Transmit data to a Remote Node.	Payload = Local TX Data	If Local Service Type = 0, Response = None If Local Service Type = 1, Response = Ack
0x0A	RequestRemote_Data	Request data from a Remote Node	Payload = Local TX Data	If Local Service Type = 1, Response = Ack Then, the remote node host must send a ResponseRemote_Data command. The response must be completely transmitted within 1.5s of receiving the request. Otherwise, the requesting node will time out.
0x0B	ResponseRemote_Data	Transmit response data to a Remote Node.	Payload = Local TX Data	None
0x0C	SetRemote_BIU	Enables/Disables BIU functionality at the remote node	0 - Enable Remote BIU 1 - Disable Remote BIU	If Remote Lock Config = 0, Response = 00 (Success) If Remote Lock Config = 1, Response = 01 (Denied)

2. High Brightness (HB) LED Controller

Figure 2-1. CY8CLED16P01: HB LED Controller



The HB LED Controller is based on Cypress's EZ-Color™ technology. EZ-Color offers the ideal control solution for high brightness (HB) LED applications requiring intelligent dimming control. EZ-Color devices combine the power and flexibility of PSoC (Programmable System-on-Chip) with Cypress's PrISM™ (Precise Illumination Signal Modulation) modulation technology providing lighting designers a fully customizable and integrated lighting solution platform.

The CY8CLED16P01 supports up to 16 independent LED channels with up to 32 bits of resolution per channel, giving lighting designers the flexibility to choose the LED array size and color quality. PSoC Designer software, with lighting-specific user modules, significantly cuts development time and simplifies implementation of fixed color points through temperature and LED binning compensation. EZ-Color's virtually limitless analog and digital customization enable simple integration of features in addition to intelligent lighting, such as battery charging, image stabilization, and motor control during the development process. These features, along with Cypress's best-in-class quality and design support, make EZ-Color the ideal choice for intelligent HB LED control applications.

The list of functions that EZ-Color devices implement are:

- LED Dimming Modulation
- Pulse Density Modulation Techniques
  - DMX512
  - DALI
- Digital Communication for Lighting
- LED Temperature Compensation
- 3- and 4-Channel Color Mixing
  - Including LED Binning Compensation
- Optical Feedback Algorithms

2.1 LED Dimming Modulation

The LED Dimming modulators are an important part of any HB LED application. All EZ-Color controllers are capable of three primary types of LED dimming modulations. These are:

- Pulse Width Modulation (PWM)
- Precise Illumination Signal Modulation (PrISM)
- Delta Sigma Modulated PWM (DSPWM)

PWM is among the most commonly used and conventional methods of modulation. It is straightforward to use and effective in practice. There are two additional techniques of modulation supported by EZ-Color that are superior to using the PWM alone:

- PrISM is a modulation technique that is developed and patented by Cypress. It results in reduced EMI as compared to the PWM technique while still providing adequate dimming control for LEDs.
- The Delta Sigma Modulated PWM technique provides higher resolution while using the same hardware resources as a conventional PWM.

LED dimming modulators use digital block resources. Digital blocks are configurable 8-bit digital peripherals. There are two types of digital blocks in the CY8CLED16P01: basic and communication. Usually, there are equal numbers of each. Any communication functions must be implemented using communication blocks but basic, noncommunication functions are implemented using either kind of block.

PWM and DSPWM modulators can have a dimming resolution of up to 16 bits. A PrISM modulator can theoretically have a dimming resolution of up to 32 bits, but the maximum recommended resolution for these modulators is 13 bits. This is because the output signal of a PrISM modulator has a frequency output range that increases with the resolution of the modulator. This increase in frequency output range is undesirable as it goes beyond the switching frequency of the current driver. Therefore, a resolution of 13 bits or lower is recommended for a PrISM modulator. Refer to application note AN47372, *PrISM Technology for LED Dimming* on http://www.cypress.com, for details.

To determine the number of digital blocks used by one PWM or PrISM modulator, use Equation 1. Note that a partial digital block cannot be used, so the result must always be rounded up. In Equation 1, n is the dimming resolution of the modulator. The resolution of dimming is determined by the color accuracy needed for the end application.

$$DigBlocks_{PWM,PRISM} = \frac{n}{8} \qquad \text{Equation 1}$$

Equations 2 and 3 are used to determine how many digital blocks are needed by a DSPWM. The total dimming resolution of a DSPWM modulator is the total of the hardware PWM modulation resolution and extra resolution added by Delta Sigma modulation in the software. Equation 3 shows that the number of digital blocks needed is only determined by the hardware resolution.

$$DigBlocks_{DSPWM} = \frac{n_{HW}}{8} \quad \text{Equation 2}$$

$$n_{Total} = n_{SW} + n_{HW} \quad \text{Equation 3}$$

These equations show that more dimming resolution is achieved with a DSPWM modulator than with a PWM or PrISM modulator. A DSPWM modulator requires more code space and execution time to use.

Equations 1, 2, and 3 determine the number of digital blocks required by one modulator. The total number of blocks for all modulators is determined by adding up the digital blocks needed by each modulator used in the device.

The CY8CLED16P01 device has a variety of LED dimming configurations. Because it has 16 digital blocks, it can implement eight 16-bit PWM modulators, eight 12-bit PrISM modulators, or sixteen 12-bit DSPWM modulators (assuming the software resolution is 4 bits). As another example, it can implement four 10-bit PrISM modulators and still have 8 digital blocks left over to implement other digital functions.

The CY8CLED16P01 is a one-device solution for powerline communication and HB LED control. For an application that runs powerline communication and HB LED control simultaneously, the CY8CLED16P01 can implement four 16-bit PWM modulators, four 12-bit PrISM modulators, or eight 12-bit DSPWM modulators (assuming the software resolution is 4 bits).

2.2 Color Mixing Algorithm

Code algorithms to implement color mixing functionality work well with EZ-Color controllers. Color mixing algorithms convert a set of color coordinates that specify a color into the appropriate 8-bit dimming values for the LED dimming modulators. This enables the EZ-Color controller to be communicated on a higher level and maintain desired color and brightness levels.

The basic 3-channel color mixing firmware performing 8-bit LED dimming requires three 8-bit dimming blocks. The discussion on LED dimming modulation implies that it consumes three digital blocks. The addition of a simple temperature compensation algorithm using a thermistor consumes an additional digital block and analog block (for the ADC).

If the dimming resolution is increased, the number of digital blocks needed should be calculated accordingly.

2.3 LED Temperature Compensation

Many HB LED systems need to measure analog signals. One or more thermistors are often present to measure temperatures of the system and the LEDs. The CY8CLED16P01 measures an analog signal with an analog-to-digital converter (ADC). The device can implement a variety of flexible ADC implementations. The ADCs cover a wide range of resolutions and techniques and use varied number of digital and analog block resources. For help in selecting from this multitude of ADCs, refer to application note AN2239, *Analog – ADC Selection* on http://www.cypress.com. When designing with an EZ-Color device, the number of digital and analog blocks used by an ADC must be factored into the total number of digital and analog blocks that are used.

In a typical case, such as the 3-channel color mixing firmware IP developed by Cypress, the simple 8-bit incremental ADC is used. This module occupies one digital and one switched capacitor analog block.

Analog blocks come in two types: continuous time and switched capacitor blocks. The former enables continuous time functions such as comparators and programmable gain amplifiers. The switched capacitor blocks enable functions such as ADCs and filters.

Temperature sensors with an I^2C interface can also be used instead of raw thermistors, thereby eliminating the need for ADCs and complicated processing.

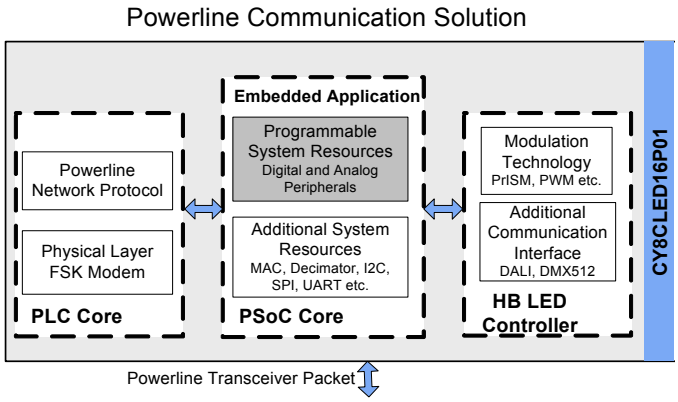
2.4 ColorLock Algorithm

ColorLock functionality uses feedback from an optical sensor in the system to adjust the LED dimming modulators correctly to “lock on” to a target color. This is similar to the concept of temperature compensation because it compensates for change in color. Instead of indirectly measuring change in color through temperature, it senses actual change in color and compensates for it.

The ColorLock algorithm implemented by Cypress requires the use of 10 digital blocks. Due to a 9-bit PrISM implementation, 6 digital blocks are used for dimming as in Equation 1. A 16-bit PWM and two 8-bit timers are also used to form the frame generator, pulse counter, and debounce counter.

3.1 Programmable System Resources

Figure 3-2. Programmable System Resources



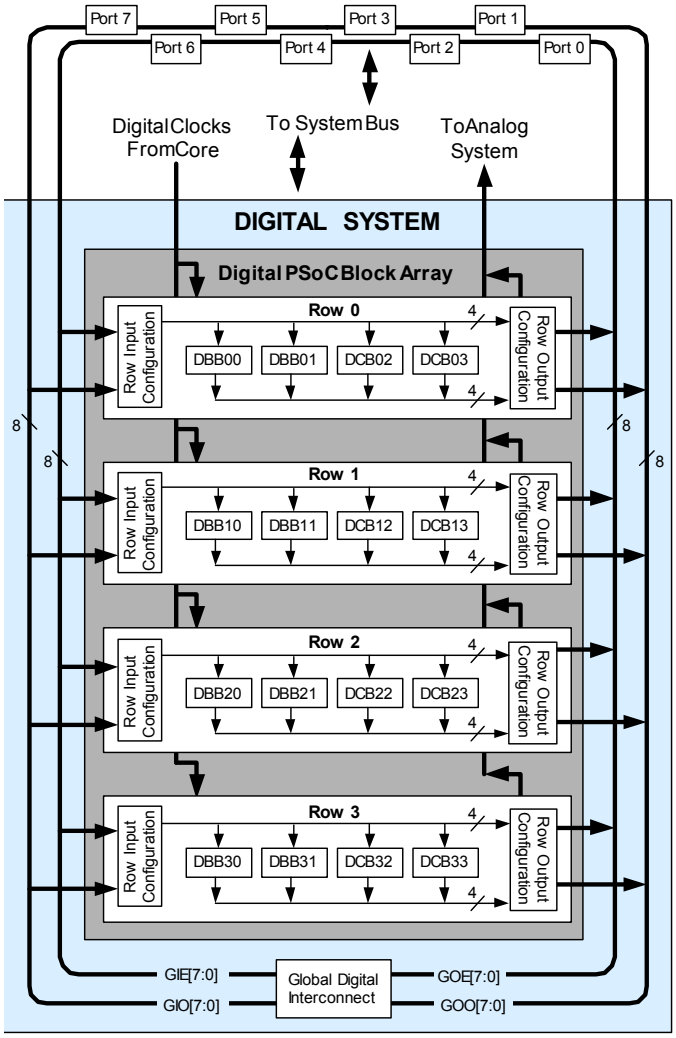
3.1.1 The Digital System

The digital system contains 16 digital PSoC blocks. Each block is an 8-bit resource that can be used alone, or combined with other blocks to form 8-, 16-, 24-, and 32-bit peripherals called user module references. Digital peripheral configurations include:

- PWMs (8 to 32 bit)
- PWMs with Dead Band (8 to 32 bit)
- Counters (8 to 32 bit)
- Timers (8 to 32 bit)
- UART 8 bit with selectable parity (up to four)
- SPI master and slave (up to four each)
- I^2C slave and multi-master (one available as a System Resource)
- Cyclical Redundancy Checker and Generator (8 to 32 bit)
- IrDA (up to 4)
- Pseudo Random Sequence Generators (8 to 32 bit)

The digital blocks can be connected to any GPIO through a series of global buses that can route any signal to any pin. The buses also enable signal multiplexing and perform logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

Figure 3-3. Digital System Block Diagram



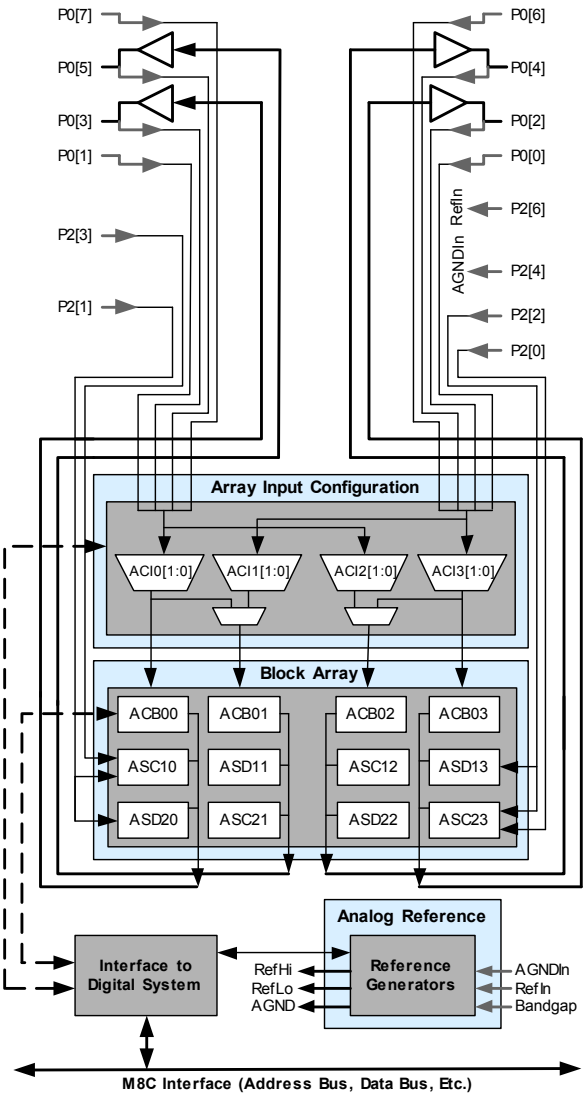
3.1.2 The Analog System

The analog system contains 12 configurable blocks, each containing an opamp circuit, enabling the creation of complex analog signal flows. Analog peripherals are very flexible and can be customized to support specific application requirements. Some of the more common PSoC analog functions (most available as user modules) are:

- Analog-to-digital converters (up to 4, with 6- to 14-bit resolution, selectable as Incremental, Delta Sigma, and SAR)
- Filters (2, 4, 6, or 8 pole band pass, low pass, and notch)
- Amplifiers (up to 4, with selectable gain to 48x)
- Instrumentation amplifiers (up to 2, with selectable gain to 93x)
- Comparators (up to 4, with 16 selectable thresholds)
- DACs (up to 4, with 6- to 9-bit resolution)
- Multiplying DACs (up to 4, with 6- to 9-bit resolution)
- High current output drivers (4 with 40 mA drive as a Core Resource)
- 1.3V reference (as a System Resource)
- DTMF Dialer
- Modulators
- Correlators
- Peak detectors
- Many other topologies possible

Analog blocks are provided in columns of three, which includes one CT (continuous time) and two SC (switched capacitor) blocks, as shown in the Figure 3-4. on page 12.

Figure 3-4. Analog System Block Diagram



7. Document Conventions

7.1 Acronyms Used

This table lists the acronyms used in this data sheet.

Table 7-1. Acronyms

Acronym	Description
AC	alternating current
ADC	analog-to-digital converter
API	application programming interface
CPU	central processing unit
CT	continuous time
DAC	digital-to-analog converter
DC	direct current
EEPROM	electrically erasable programmable read-only memory
FSR	full scale range
GPIO	general purpose IO
ICE	in-circuit emulator
IDE	integrated development environment
IO	input/output
ISSP	in-system serial programming
IPOR	imprecise power on reset
LSb	least-significant bit
LVD	low voltage detect
MSb	most-significant bit
PC	program counter
PGA	programmable gain amplifier
POR	power on reset
PPOR	precision power on reset
PSoC®	Programmable System-on-Chip
PWM	pulse width modulator
ROM	read only memory
SC	switched capacitor
SRAM	static random access memory

7.2 Units of Measure

A units of measure table is located in the section Electrical Specifications on page 25.

7.3 Numeric Naming

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexadecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (for example, 01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’, ‘b’, or 0x are decimal.

8. Pin Information

The CY8CLED16P01 PLC device is available in a variety of packages which are listed and illustrated in the following tables. Every port pin (labeled with a “P”) is capable of Digital I/O. However, Vss, Vdd, and XRES are not capable of Digital I/O.

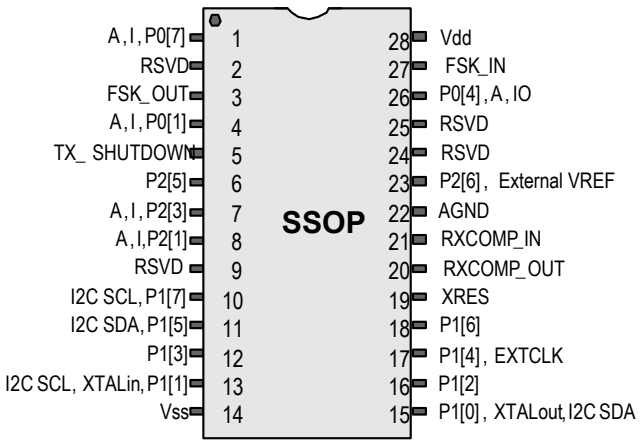
8.1 28-Pin Part Pinout

Table 8-1. 28-Pin Part Pinout (SSOP)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	IO	I	P0[7]	Analog Column Mux Input
2	Reserved		RSVD	Reserved
3		O	FSK_OUT	Analog FSK Output
4	IO	I	P0[1]	Analog Column Mux Input
5	O		TX_SHUT DOWN	Output to disable PLC transmit circuitry in receive mode Logic ‘0’ - When the Modem is trans-mitting Logic ‘1’ - When the Modem is not transmitting
6	IO		P2[5]	
7	IO	I	P2[3]	Direct switched capacitor block input
8	IO	I	P2[1]	Direct switched capacitor block input
9	Reserved		RSVD	Reserved
10	IO		P1[7]	I2C Serial Clock (SCL)
11	IO		P1[5]	I2C Serial Data (SDA)
12	IO		P1[3]	XTAL_STABILITY. Connect a 0.1 uF capacitor between the pin and VSS.
13	IO		P1[1]	Crystal (XTALin)[2], ISSP-SCLK[1], I2C SCL
14	Power		Vss	Ground connection.
15	IO		P1[0]	Crystal (XTALout)[2], ISSP-SDATA[1], I2C SDA
16	IO		P1[2]	
17	IO		P1[4]	Optional External Clock Input (EXTCLK)[2]
18	IO		P1[6]	
19	Input		XRES	Active high external reset with internal pull down
20		O	RXCOMP_ OUT	Analog Output to external Low Pass Filter Circuitry
21		I	RXCOMP_ IN	Analog Input from the external Low Pass Filter Circuitry
22	Analog Ground		AGND	Analog Ground
23	IO		P2[6]	External Voltage Reference (VREF)
24	Reserved		RSVD	Reserved
25	Reserved		RSVD	Reserved
26	IO	IO	P0[4]	Analog column mux input and column output
27		I	FSK_IN	Analog FSK Input
28	Power		Vdd	Supply Voltage

LEGEND: A = Analog, I = Input, O = Output, and RSVD = Reserved (should be left unconnected).

Figure 8-1. CY8CLED16P01 28-Pin PLC Device



Notes
1. These are the ISSP pins, which are not High Z at POR (Power On Reset). See the *PSoC Technical Reference Manual* for details.
2. When using the PLT user module, the external crystal is always required for protocol timing. For the FSK modem, either the PLL Mode should be enabled or the external 24MHz on P1[4] should be selected. The IMO should not be used.

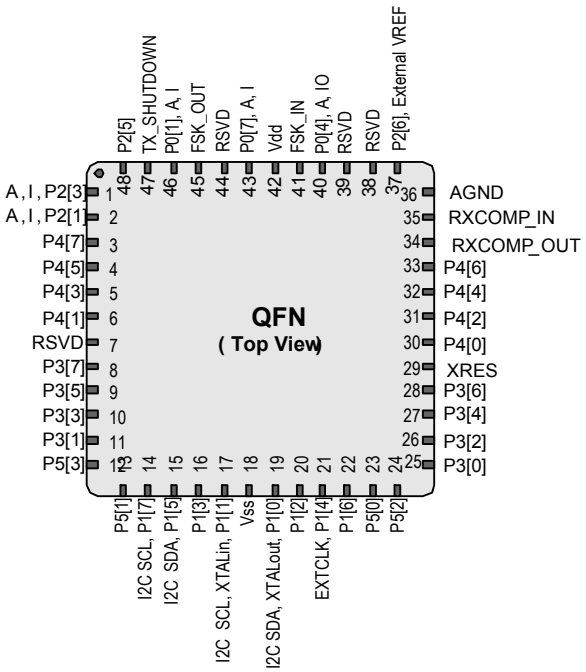
8.1 48-Pin Part Pinout

Table 8-2. 48-Pin Part Pinout (QFN)[3]

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	IO	I	P2[3]	Direct switched capacitor block input
2	IO	I	P2[1]	Direct switched capacitor block input
3	IO		P4[7]	
4	IO		P4[5]	
5	IO		P4[3]	
6	IO		P4[1]	
7	Reserved		RSVD	Reserved
8	IO		P3[7]	
9	IO		P3[5]	
10	IO		P3[3]	
11	IO		P3[1]	
12	IO		P5[3]	
13	IO		P5[1]	
14	IO		P1[7]	I2C Serial Clock (SCL)
15	IO		P1[5]	I2C Serial Data (SDA)
16	IO		P1[3]	XTAL_STABILITY. Connect a 0.1 uF capacitor between the pin and VSS.
17	IO		P1[1]	Crystal (XTALin)[2], I2C Serial Clock (SCL), ISSP-SCLK[1]
18	Power		Vss	Ground connection.
19	IO		P1[0]	Crystal (XTALout)[2], I2C Serial Data (SDA), ISSP-SDATA[1]
20	IO		P1[2]	
21	IO		P1[4]	Optional External Clock Input (EXTCLK)[2]
22	IO		P1[6]	
23	IO		P5[0]	
24	IO		P5[2]	
25	IO		P3[0]	
26	IO		P3[2]	
27	IO		P3[4]	
28	IO		P3[6]	
29	Input		XRES	Active high external reset with internal pull down
30	IO		P4[0]	
31	IO		P4[2]	
32	IO		P4[4]	
33	IO		P4[6]	
34		O	RXCOMP_OUT	Analog Output to external Low Pass Filter Circuitry
35		I	RXCOMP_IN	Analog Input from external Low Pass Filter Circuitry
36	Analog Ground		AGND	Analog Ground
37	IO		P2[6]	External Voltage Reference (VREF)
38	Reserved		RSVD	Reserved
39	Reserved		RSVD	Reserved
40	IO	IO	P0[4]	Analog column mux input and column output
41		I	FSK_IN	Analog FSK Input
42	Power		Vdd	Supply Voltage
43	IO	I	P0[7]	Analog column mux input
44	Reserved		RSVD	Reserved
45		O	FSK_OUT]	Analog FSK Output
46	IO	I	P0[1]	Analog column mux input
47	O		TX_SHUTDOWN	Output to disable transmit circuitry in receive mode Logic '0' - When the Modem is transmitting Logic '1' - When the Modem is not transmitting
48	IO		P2[5]	

LEGEND: A = Analog, I = Input, O = Output, and RSVD = Reserved (should be left unconnected).

Figure 8-2. CY8CLED16P01 48-Pin PLC Device



Note
3. The QFN package has a center pad that must be connected to ground (Vss).

Table 9-1. Register Map Bank 0 Table: User Space (continued)

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
DCB02DR2	2A	RW		6A		MUL1_DH	AA	R	MUL0_DH	EA	R
DCB02CR0	2B	#		6B		MUL1_DL	AB	R	MUL0_DL	EB	R
DCB03DR0	2C	#	TMP_DR0	6C	RW	ACC1_DR1	AC	RW	ACC0_DR1	EC	RW
DCB03DR1	2D	W	TMP_DR1	6D	RW	ACC1_DR0	AD	RW	ACC0_DR0	ED	RW
DCB03DR2	2E	RW	TMP_DR2	6E	RW	ACC1_DR3	AE	RW	ACC0_DR3	EE	RW
DCB03CR0	2F	#	TMP_DR3	6F	RW	ACC1_DR2	AF	RW	ACC0_DR2	EF	RW
DBB10DR0	30	#	ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
DBB10DR1	31	W	ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
DBB10DR2	32	RW	ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
DBB10CR0	33	#	ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
DBB11DR0	34	#	ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
DBB11DR1	35	W	ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
DBB11DR2	36	RW	ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
DBB11CR0	37	#	ACB01CR2	77	RW		B7		CPU_F	F7	RL
DCB12DR0	38	#	ACB02CR3	78	RW	RDI1RI	B8	RW		F8	
DCB12DR1	39	W	ACB02CR0	79	RW	RDI1SYN	B9	RW		F9	
DCB12DR2	3A	RW	ACB02CR1	7A	RW	RDI1IS	BA	RW		FA	
DCB12CR0	3B	#	ACB02CR2	7B	RW	RDI1LT0	BB	RW		FB	
DCB13DR0	3C	#	ACB03CR3	7C	RW	RDI1LT1	BC	RW		FC	
DCB13DR1	3D	W	ACB03CR0	7D	RW	RDI1RO0	BD	RW		FD	
DCB13DR2	3E	RW	ACB03CR1	7E	RW	RDI1RO1	BE	RW	CPU_SCR1	FE	#
DCB13CR0	3F	#	ACB03CR2	7F	RW		BF		CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed. # Access is bit specific.

Table 9-2. Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW	DBB20FN	40	RW	ASC10CR0	80	RW	RDI2RI	C0	RW
PRT0DM1	01	RW	DBB20IN	41	RW	ASC10CR1	81	RW	RDI2SYN	C1	RW
PRT0IC0	02	RW	DBB20OU	42	RW	ASC10CR2	82	RW	RDI2IS	C2	RW
PRT0IC1	03	RW		43		ASC10CR3	83	RW	RDI2LT0	C3	RW
PRT1DM0	04	RW	DBB21FN	44	RW	ASD11CR0	84	RW	RDI2LT1	C4	RW
PRT1DM1	05	RW	DBB21IN	45	RW	ASD11CR1	85	RW	RDI2RO0	C5	RW
PRT1IC0	06	RW	DBB21OU	46	RW	ASD11CR2	86	RW	RDI2RO1	C6	RW
PRT1IC1	07	RW		47		ASD11CR3	87	RW		C7	
PRT2DM0	08	RW	DCB22FN	48	RW	ASC12CR0	88	RW	RDI3RI	C8	RW
PRT2DM1	09	RW	DCB22IN	49	RW	ASC12CR1	89	RW	RDI3SYN	C9	RW
PRT2IC0	0A	RW	DCB22OU	4A	RW	ASC12CR2	8A	RW	RDI3IS	CA	RW
PRT2IC1	0B	RW		4B		ASC12CR3	8B	RW	RDI3LT0	CB	RW
PRT3DM0	0C	RW	DCB23FN	4C	RW	ASD13CR0	8C	RW	RDI3LT1	CC	RW
PRT3DM1	0D	RW	DCB23IN	4D	RW	ASD13CR1	8D	RW	RDI3RO0	CD	RW
PRT3IC0	0E	RW	DCB23OU	4E	RW	ASD13CR2	8E	RW	RDI3RO1	CE	RW
PRT3IC1	0F	RW		4F		ASD13CR3	8F	RW		CF	
PRT4DM0	10	RW	DBB30FN	50	RW	ASD20CR0	90	RW	GDI_O_IN	D0	RW
PRT4DM1	11	RW	DBB30IN	51	RW	ASD20CR1	91	RW	GDI_E_IN	D1	RW
PRT4IC0	12	RW	DBB30OU	52	RW	ASD20CR2	92	RW	GDI_O_OU	D2	RW
PRT4IC1	13	RW		53		ASD20CR3	93	RW	GDI_E_OU	D3	RW
PRT5DM0	14	RW	DBB31FN	54	RW	ASC21CR0	94	RW		D4	
PRT5DM1	15	RW	DBB31IN	55	RW	ASC21CR1	95	RW		D5	
PRT5IC0	16	RW	DBB31OU	56	RW	ASC21CR2	96	RW		D6	
PRT5IC1	17	RW		57		ASC21CR3	97	RW		D7	
PRT6DM0	18	RW	DCB32FN	58	RW	ASD22CR0	98	RW		D8	
PRT6DM1	19	RW	DCB32IN	59	RW	ASD22CR1	99	RW		D9	
PRT6IC0	1A	RW	DCB32OU	5A	RW	ASD22CR2	9A	RW		DA	
PRT6IC1	1B	RW		5B		ASD22CR3	9B	RW		DB	
PRT7DM0	1C	RW	DCB33FN	5C	RW	ASC23CR0	9C	RW		DC	
PRT7DM1	1D	RW	DCB33IN	5D	RW	ASC23CR1	9D	RW	OSC_GO_EN	DD	RW
PRT7IC0	1E	RW	DCB33OU	5E	RW	ASC23CR2	9E	RW	OSC_CR4	DE	RW
PRT7IC1	1F	RW		5F		ASC23CR3	9F	RW	OSC_CR3	DF	RW
DBB00FN	20	RW	CLK_CR0	60	RW		A0		OSC_CR0	E0	RW
DBB00IN	21	RW	CLK_CR1	61	RW		A1		OSC_CR1	E1	RW
DBB00OU	22	RW	ABF_CR0	62	RW		A2		OSC_CR2	E2	RW
	23		AMD_CR0	63	RW		A3		VLT_CR	E3	RW
DBB01FN	24	RW		64			A4		VLT_CMP	E4	R

Blank fields are Reserved and should not be accessed. # Access is bit specific.

10.3.3 DC Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

The Operational Amplifier is a component of both the Analog Continuous Time PSoC blocks and the Analog Switched Capacitor PSoC blocks. The guaranteed specifications are measured in the Analog Continuous Time PSoC block. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 10-6. 5V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input Offset Voltage (Absolute Value) Power = Low, Opamp Bias = High Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 – – –	 1.6 1.3 1.2	 10 8 7.5	 mV mV mV	
TCV_{OSOA}	Average Input Offset Voltage Drift	–	7.0	35.0	µV/°C	
I_{EBOA}	Input Leakage Current (Port 0 Analog Pins)	–	200	–	pA	Gross tested to 1 µA.
C_{INOA}	Input Capacitance (Port 0 Analog Pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25°C.
V_{CMOA}	Common Mode Voltage Range. All cases, except highest. Power = High, Opamp Bias = High	0.0 0.5	– –	Vdd Vdd - 0.5	V V	
$CMRR_{OA}$	Common Mode Rejection Ratio	60	–	–	dB	
G_{OLOA}	Open Loop Gain	80	–	–	dB	
$V_{OHIGHOA}$	High Output Voltage Swing (Internal Signals)	Vdd - 0.01	–	–	V	
V_{OLOWOA}	Low Output Voltage Swing (Internal Signals)	–	–	0.1	V	
I_{SOA}	Supply Current (including associated AGND buffer) Power = Low, Opamp Bias = Low Power = Low, Opamp Bias = High Power = Medium, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = Low Power = High, Opamp Bias = High	 – – – – – –	 150 300 600 1200 2400 4600	 200 400 800 1600 3200 6400	 µA µA µA µA µA µA	
$PSRR_{OA}$	Supply Voltage Rejection Ratio	67	80	–	dB	Vss ≤ VIN ≤ (Vdd - 2.25) or (Vdd - 1.25V) ≤ VIN ≤ Vdd.

10.3.4 DC Low Power Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 10-7. DC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{REFLPC}	Low Power Comparator (LPC) Reference Voltage Range	0.2	–	Vdd - 1	V	
I_{SLPC}	LPC Supply Current	–	10	40	µA	
V_{OSLPC}	LPC Voltage Offset	–	2.5	30	mV	

Table 10-9. 5V DC Analog Reference Specifications (continued)

Symbol	Description	Min	Typ	Max	Units
–	RefHi = 2 x Bandgap	2.50	2.60	2.70	V
–	RefHi = 3.2 x Bandgap	4.02	4.16	4.29	V
–	RefLo = Bandgap	BG - 0.082	BG + 0.023	BG + 0.129	V
–	RefLo = 2 x Bandgap - P2[6] (P2[6] = 1.3V)	2 x BG - P2[6] - 0.084	2 x BG - P2[6] + 0.025	2 x BG - P2[6] + 0.134	V
–	RefLo = P2[4] – Bandgap (P2[4] = Vdd/2)	P2[4] - BG - 0.056	P2[4] - BG + 0.026	P2[4] - BG + 0.107	V
–	RefLo = P2[4]-P2[6] (P2[4] = Vdd/2, P2[6] = 1.3V)	P2[4] - P2[6] - 0.057	P2[4] - P2[6] + 0.026	P2[4] - P2[6] + 0.110	V

10.3.7 DC Analog PSoC Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 10-10. DC Analog PSoC Block Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{CT}	Resistor Unit Value (Continuous Time)	–	12.2	–	kΩ	
C_{SC}	Capacitor Unit Value (Switch Cap)	–	80	–	fF	

10.3.8 DC POR and LVD Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C = TA = 85°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 10-11. DC POR and LVD Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
VPPOR2R	Vdd Value for PPOR Trip (positive ramp) PORLEV[1:0] = 10b	–	4.55	–	V	
VPPOR2	Vdd Value for PPOR Trip (negative ramp) PORLEV[1:0] = 10b	–	4.55	–	V	
VPH2	PPOR Hysteresis PORLEV[1:0] = 10b	–	0	–	mV	
VLVD6 VLVD7	Vdd Value for LVD Trip VM[2:0] = 110b VM[2:0] = 111b	4.63 4.72	4.73 4.81	4.82 4.91	V V	

10.3.9 DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 10-12. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
I_{DDP}	Supply Current During Programming or Verify	–	10	30	mA	
V_{ILP}	Input Low Voltage During Programming or Verify	–	–	0.8	V	
V_{IHP}	Input High Voltage During Programming or Verify	2.2	–	–	V	
I_{ILP}	Input Current when Applying V_{ILP} to P1[0] or P1[1] During Programming or Verify	–	–	0.2	mA	Driving internal pull down resistor
I_{IHP}	Input Current when Applying V_{IHP} to P1[0] or P1[1] During Programming or Verify	–	–	1.5	mA	Driving internal pull down resistor
V_{OLV}	Output Low Voltage During Programming or Verify	–	–	Vss + 0.75	V	
V_{OHV}	Output High Voltage During Programming or Verify	Vdd - 1.0	–	Vdd	V	
$Flash_{ENPB}$	Flash Endurance (per block)	50,000	–	–	–	Erase/write cycles per block
$Flash_{ENT}$	Flash Endurance (total)[5]	1,800,000	–	–	–	Erase/write cycles
$Flash_{DR}$	Flash Data Retention	10	–	–	Years	

10.4 AC Electrical Characteristics

10.4.1 AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

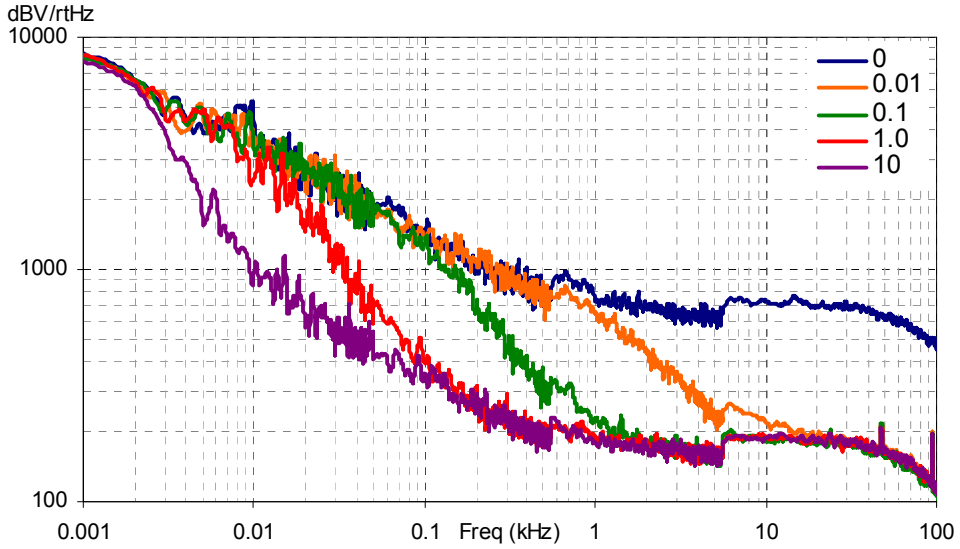
Note See the individual user module data sheets for information on maximum frequencies for user modules.

Table 10-13. AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{IMO24}	Internal Main Oscillator Frequency for 24 MHz	23.4	24	24.6	MHz	Trimmed for 5V operation using factory trim values. SLIMO Mode = 0.
F_{IMO6}	Internal Main Oscillator Frequency for 6 MHz	5.5	6	6.5[6]	MHz	Trimmed for 5V operation using factory trim values. SLIMO Mode = 1.
F_{CPU1}	CPU Frequency (5V Nominal)	0.93	24	24.6[6]	MHz	
F_{48M}	Digital PSoC Block Frequency	0	48	49.2[6, 7]	MHz	Refer to the AC Digital Block Specifications below.
F_{32K1}	Internal Low Speed Oscillator Frequency	15	32	64	kHz	
F_{32K2}	External Crystal Oscillator	–	32.768	–	kHz	Accuracy is capacitor and crystal dependent. 50% duty cycle.

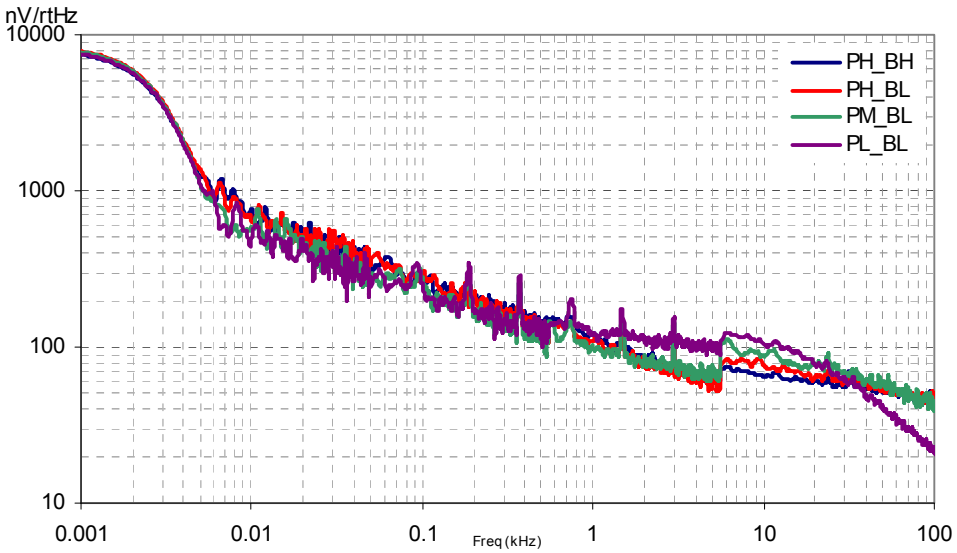
Notes
5. A maximum of 36 x 50,000 block endurance cycles is allowed. This may be balanced between operations on 36x1 blocks of 50,000 maximum cycles each, 36x2 blocks of 25,000 maximum cycles each, or 36x4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36x50,000 and that no single block ever sees more than 50,000 cycles). For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 at http://www.cypress.com under Application Notes for more information.
6. Accuracy derived from Internal Main Oscillator with appropriate trim for Vdd range.
7. See the individual user module data sheets for information on maximum frequencies for user modules.

Figure 10-7. Typical AGND Noise with P2[4] Bypass



At low frequencies, the opamp noise is proportional to 1/f, power independent, and determined by device geometry. At high frequencies, increased power level reduces the noise spectrum level.

Figure 10-8. Typical Opamp Noise



10.4.4 AC Low Power Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 10-16. AC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{RLPC}	LPC response time	–	–	50	µs	≥ 50 mV overdrive comparator reference set within V_{REFLPC}.

Table 10-20. AC Programming Specifications (continued)

Symbol	Description	Min	Typ	Max	Units	Notes
T_{DSCLK}	Data Out Delay from Falling Edge of SCLK	–	–	45	ns	
$T_{ERASEALL}$	Flash Erase Time (Bulk)	–	80	–	ms	Erase all Blocks and protection fields at once
$T_{PROGRAM\_HOT}$	Flash Block Erase + Flash Block Write Time	–	–	100[9]	ms	0°C <= Tj <= 100°C
$T_{PROGRAM\_COLD}$	Flash Block Erase + Flash Block Write Time	–	–	200[9]	ms	-40°C <= Tj <= 0°C

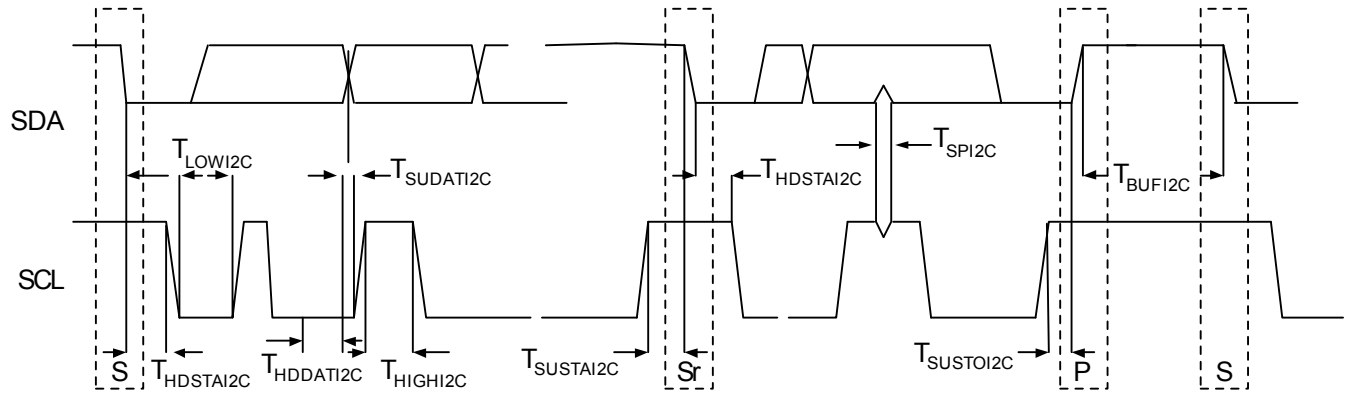
10.4.9 AC I²C Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 10-21. AC Characteristics of the I²C SDA and SCL Pins

Symbol	Description	Standard Mode		Fast Mode		Units	Notes
		Min	Max	Min	Max		
F_{SCLI2C}	SCL Clock Frequency	0	100	0	400	kHz	
$T_{HDSTAI2C}$	Hold Time (repeated) START Condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	µs	
T_{LOWI2C}	LOW Period of the SCL Clock	4.7	–	1.3	–	µs	
$T_{HIGHI2C}$	HIGH Period of the SCL Clock	4.0	–	0.6	–	µs	
$T_{SUSTAI2C}$	Setup Time for a Repeated START Condition	4.7	–	0.6	–	µs	
$T_{HDDATI2C}$	Data Hold Time	0	–	0	–	µs	
$T_{SUDATI2C}$	Data Setup Time	250	–	100[10]	–	ns	
$T_{SUSTOI2C}$	Setup Time for STOP Condition	4.0	–	0.6	–	µs	
T_{BUFI2C}	Bus Free Time Between a STOP and START Condition	4.7	–	1.3	–	µs	
T_{SPI2C}	Pulse Width of spikes are suppressed by the input filter	–	–	0	50	ns	

Figure 10-9. Definition for Timing for Fast/Standard Mode on the I²C Bus Packaging Dimensions



Notes

9. For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 at http://www.cypress.com for more information.
10. A Fast-Mode I2C-bus device can be used in a Standard-Mode I2C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If this device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the Standard-Mode I2C-bus specification) before the SCL line is released.

11.1 Thermal Impedances

Table 11-1. Thermal Impedances per Package

Package	Typical θ_{JA}[11]
28 SSOP	94°C/W
48 QFN[12]	28°C/W
100 TQFP	50°C/W

11.2 Capacitance on Crystal Pins

Table 11-2. Typical Package Capacitance on Crystal Pins

Package	Package Capacitance
28 SSOP	2.8 pF
48 QFN	1.8 pF
100 TQFP	3.1 pF

11.3 Solder Reflow Peak Temperature

Following is the minimum solder reflow peak temperature to achieve good solderability.

Table 11-3. Solder Reflow Peak Temperature

Package	Minimum Peak Temperature[13]	Maximum Peak Temperature
28 SSOP	240°C	260°C
48 QFN	220°C	260°C
100 TQFP	220°C	260°C

Notes
11. $T_J = T_A + POWER \times \theta_{JA}$
12. To achieve the thermal impedance specified for the QFN package, the center thermal pad should be soldered to the PCB ground plane.
13. Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are 220 ± 5°C with Sn-Pb or 245 ± 5°C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.

12. Development Tool Selection

12.1 Software

12.1.1 PSoC Designer™

At the core of the PSoC development software suite is PSoC Designer. Utilized by thousands of PSoC developers, this robust software has been facilitating PSoC designs for years. PSoC Designer is available free of charge at http://www.cypress.com. PSoC Designer comes with a free C compiler.

12.1.2 PSoC Programmer

PSoC Programmer is a very flexible programming application. It is used on the bench in development and is also suitable for factory programming. PSoC Programmer works either in a standalone configuration or operates directly from PSoC Designer. PSoC Programmer software is compatible with both PSoC ICE Cube In-Circuit Emulator and PSoC MiniProg. PSoC programmer is available free of charge at http://www.cypress.com/psocprogrammer.

12.2 Development Kits

All development kits are sold at the Cypress Online Store.

12.2.1 CY3276-Programmable HV PLC + EZ-Color™ Development Kit

The CY3276 is used for prototyping and development on the CY8CLED16P01 with PSoC Designer. This kit supports in-circuit emulation. The software interface enables users to run, halt, and single-step the processor and view the content of specific memory locations. PSoC Designer also supports the advanced emulation features. The hardware contains the high voltage coupling circuit for 110 VAC to 240 VAC powerline, which is compliant with the CENELEC/FCC standards. This board also has an onboard switch mode power supply. The kit includes:

- One High Voltage (110 to 230VAC) PLC Board. Cypress recommends that a user purchases two CY3276 kits to set up a two-node PLC subsystem for evaluation and development.
- LED Daughter Card
- CY8CLED16P01-OCD (100 TQFP)
- Software CD
- Supporting Literature
- MiniProg1

12.2.2 CY3277-Programmable LV PLC + EZ-Color Development Kit

The CY3277-PLC is used for prototyping and development on the CY8CLED16P01 with PSoC Designer. This kit supports in-circuit emulation. The software interface enables users to run, halt, and single-step the processor and view the content of specific memory locations. PSoC Designer also supports advanced emulation features. The hardware contains the low voltage coupling circuit for 12-24V AC/DC powerline. The kit includes:

- One Low Voltage (12 to 24V AC/DC) PLC Board. Cypress recommends that a user purchases two CY3275 kits to set up a two-node PLC subsystem for evaluation and development
- LED Daughter Card
- CY8CLED16P01-OCD (100 TQFP)
- Software CD
- Supporting Literature
- MiniProg1

12.2.3 CY3250-PLC Pod Kits

The CY3250-PLC Pod Kits are essential for development purposes as they provide the users a medium to emulate and debug their designs. The pod kits are available for all the available footprints. The details are:

- CY3250-LED16P01NQ – One SSOP Pod (CY8CLED16P01-OCD), Two 28-SSOP Feet, One 3250-Flex Cable, One 28-SSOP Foot Mask
- CY3250-LED16P01QFN – One QFN Pod (CY8CLED16P01-OCD), Two 48-QFN Feet, One 3250-Flex Cable
- CY3250-LED16P01NQ-POD – Two SSOP Pods (CY8CLED16P01-OCD)
- CY3250-LED16P01QFN-POD – Two QFN Pods (CY8CLED16P01-OCD)

12.2.4 CY3215-DK Basic Development Kit

The CY3215-DK is used for prototyping and development with PSoC Designer. This kit can be used in conjunction with the PLC kits to support in-circuit emulation. The software interface enables users to run, halt, and single step the processor and view the content of specific memory locations. PSoC Designer also supports the advanced emulation features. The kit includes:

- PSoC Designer Software CD
- ICE-Cube In-Circuit Emulator
- ICE Flex-Pod for CY8C29x66 Family
- Cat-5 Adapter
- Mini-Eval Programming Board
- 110 ~ 240V Power Supply, Euro-Plug Adapter
- iMAGEcraft C Compiler (Registration Required)
- ISSP Cable
- USB 2.0 Cable and Blue Cat-5 Cable
- 2 CY8C29466-24PXI 28-PDIP Chip Samples

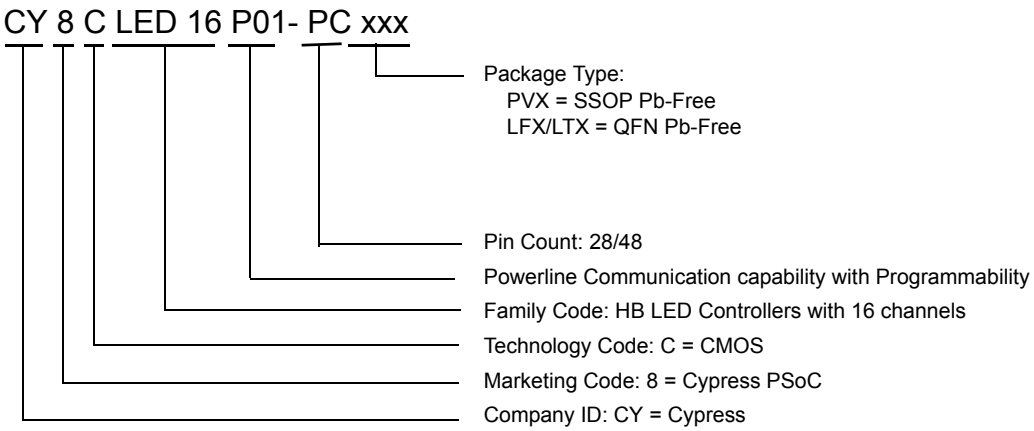
13. Ordering Information

The following table lists the CY8CLED16P01 PLC device family key package features and ordering codes.

Table 13-1. CY8CLED16P01 PLC Device Key Features and Ordering Information

Package	Ordering Code	Flash (Bytes)	RAM (Bytes)	Temperature Range	Digital PSoC Blocks	Analog PSoC Blocks	Digital IO Pins	Analog Inputs	Analog Outputs	XRES Pin
28-Pin (210 Mil) SSOP	CY8CLED16P01-28PVXI	32K	2K	-40°C to +85°C	16	12	24	12	4	Yes
28-Pin (210 Mil) SSOP (Tape and Reel)	CY8CLED16P01-28PVXIT	32K	2K	-40°C to +85°C	16	12	24	12	4	Yes
48-Pin QFN	CY8CLED16P01-48LFXI	32K	2K	-40°C to +85°C	16	12	44	12	4	Yes
48-Pin QFN (Sawn)	CY8CLED16P01-48LTXI	32K	2K	-40°C to +85°C	16	12	44	12	4	Yes
48-Pin QFN (Sawn) (Tape and Reel)	CY8CLED16P01-48LTXIT	32K	2K	-40°C to +85°C	16	12	44	12	4	Yes
100-Pin OCD TQFP[14]	CY8CLED16P01-OCD	32K	2K	-40°C to +85°C	16	12	64	12	4	Yes

14. Ordering Code Definitions



Note
14. This part may be used for in-circuit debugging. It is not available for production.