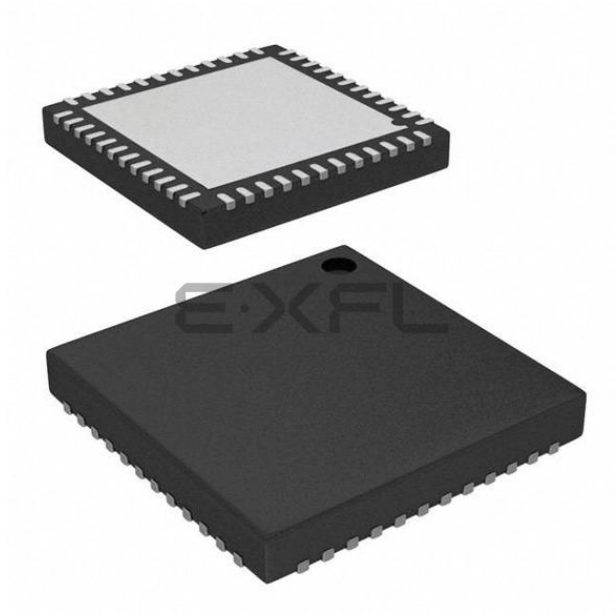

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Details	
Product Status	Obsolete
Applications	Powerline Communication
Core Processor	M8C
Program Memory Type	FLASH (32KB)
Controller Series	CY8CLED
RAM Size	2K x 8
Interface	I²C, IrDA, SPI, UART/USART
Number of I/O	44
Voltage - Supply	4.75V ~ 5.25V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8cled16p01-48ltxit

1. PLC Functional Overview

The CY8CLED16P01 is an integrated Powerline Communication (PLC) chip with the Powerline Modem PHY and Network Protocol Stack running on the same device. Apart from the PLC core, the CY8CLED16P01 also offers Cypress's revolutionary PSoC technology that enables system designers to integrate multiple functions on the same chip.

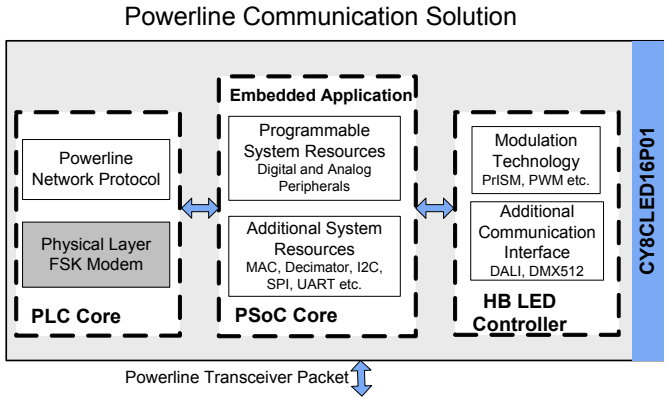
1.1 Robust Communication using Cypress's PLC Solution

Powerlines are available everywhere in the world and are a widely available communication medium for PLC technology. The pervasiveness of powerlines also makes it difficult to predict the characteristics and operation of PLC products. Because of the variable quality of powerlines around the world, implementing robust communication has been an engineering challenge for years. The Cypress PLC solution enables secure and reliable communications. Cypress PLC features that enable robust communication over powerlines include:

- Integrated Powerline PHY modem with optimized filters and amplifiers to work with lossy high voltage and low voltage powerlines.
- Powerline optimized network protocol that supports bidirectional communication with acknowledgement-based signaling. In case of data packet loss due to bursty noise on the powerline, the transmitter has the capability to retransmit data.
- The Powerline Network Protocol also supports an 8-bit CRC for error detection and data packet retransmission.
- A Carrier Sense Multiple Access (CSMA) scheme is built into the network protocol that minimizes collisions between packet transmissions on the powerline and supports multiple masters and reliable communication on a bigger network.

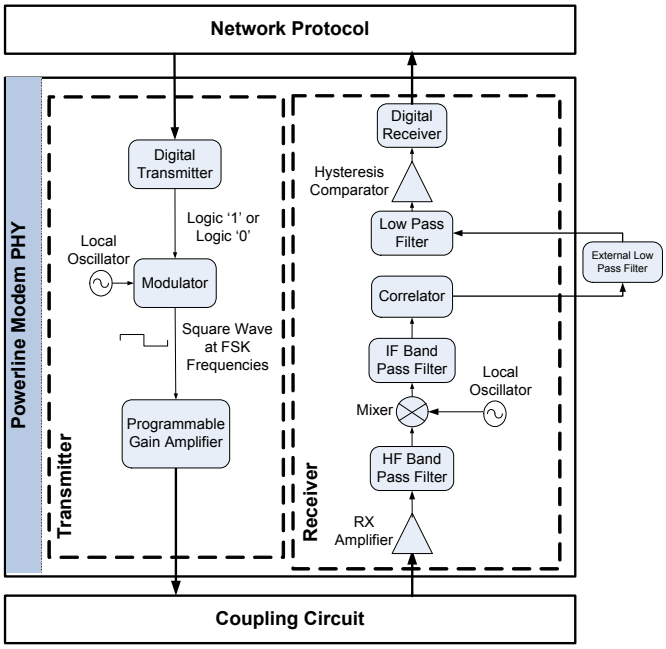
1.2 Powerline Modem PHY

Figure 1-1. Physical Layer FSK Modem



The physical layer of the Cypress PLC solution is implemented using an FSK modem that enables half duplex communication on any high voltage and low voltage powerline. This modem supports raw data rates up to 2400 bps. A block diagram is shown in Figure 1-2.

Figure 1-2. Physical Layer FSK Modem Block Diagram



1.2.1 Transmitter Section

Digital data from the network layer is serialized by the digital transmitter and fed as input to the modulator. The modulator divides the local oscillator frequency by a definite factor depending on whether the input data is high level logic '1' or low level logic '0'. It then generates a square wave at 133.3 kHz (logic '0') or 131.8 kHz (logic '1'), which is fed to the Programmable Gain Amplifier to generate FSK modulated signals. This enables tunable amplification of the signal depending on the noise in the channel. The logic '1' frequency can also be configured as 130.4 kHz for wider FSK deviation.

1.2.2 Receiver Section

The incoming FSK signal from the powerline is input to a high frequency (HF) band pass filter that filters out-of-band frequency components and outputs a filtered signal within the desired spectrum of 125 kHz to 140 kHz for further demodulation. The mixer block multiplies the filtered FSK signals with a locally generated signal to produce heterodyned frequencies.

The intermediate frequency (IF) band pass filters further remove out-of-band noise as required for further demodulation. This signal is fed to the correlator, which produces a DC component (consisting of logic '1' and '0') and a higher frequency component.

The output of the correlator is fed to a low pass filter (LPF) that outputs only the demodulated digital data at 2400 baud and suppresses all other higher frequency components generated in the correlation process. The output of the LPF is digitized by the hysteresis comparator. This eliminates the effects of correlator delay and false logic triggers due to noise. The digital receiver deserializes this data and outputs to the network layer for interpretation.

1.3.3 Packet Header

The packet header contains the first 6 bytes of the packet when 1-byte logical addressing is used. When 8-byte physical addressing is used, the source and destination addresses each contain 8 bytes. In this case, the header can consist of a maximum of 20 bytes. Unused fields marked RSVD are for future expansion and are transmitted as bit 0. Table 1-2 describes the PLT packet header fields in detail.

Table 1-2. Powerline Transceiver (PLT) Packet Header

Field Name	No. of Bits	Tag	Description
SA Type	1	Source Address Type	0 – Logical Addressing 1 – Physical Addressing
DA Type	2	Destination Address Type	00 – Logical Addressing 01 – Group Addressing 10 – Physical Addressing 11 – Invalid
Service Type	1		0 – Unacknowledged Messaging 1 – Acknowledged Messaging
Response	1	Response	0 - Not an acknowledgement or response packet 1 - Acknowledgement or response packet
Seq Num	4	Sequence Number	4-bit unique identifier for each packet between source and destination.
Header CRC	4		4-bit CRC value. This enables the receiver to suspend receiving the rest of the packet if its header is corrupted

1.3.4 Payload

The packet payload has a length of 0 to 31 bytes. Payload content is user defined and can be read or written through I^2C.

1.3.5 Packet CRC

The last byte of the packet is an 8-bit CRC value used to check packet data integrity. This CRC calculation includes the header and payload portions of the packet and is in addition to the powerline packet header CRC.

1.3.6 Sequence Numbering

The sequence number is increased for every new unique packet transmitted. If in acknowledged mode and an acknowledgment is not received for a given packet, that packet will be re-transmitted (if TX_Retry > 0) with the same sequence number. If in unacknowledged mode, the packet will be transmitted (TX_Retry + 1) times with the same sequence number.

If the receiver receives consecutive packets from the same source address with the same sequence number and packet CRC, it does not notify the host of the reception of the duplicate packet. If in acknowledged mode, it still sends an acknowledgment so that the transmitter knows that the packet was received.

1.3.7 Addressing

The CY8CLED16P01 has three modes of addressing:

- Logical addressing: Every CY8CLED16P01 node can have either a 8-bit logical address or a 16-bit logical address. The logical address of the PLC Node is set by the local application or by a remote node on the Powerline.
- Physical addressing: Every CY8CLED16P01 has a unique 64-bit physical address.
- Group addressing: This is explained in the next section.

1.3.8 Group Membership

Group membership enables the user to multicast messages to select groups. The CY8CLED16P01 supports two types of group addressing:

- Single Group Membership – The network protocol supports up to 256 different groups on the network in this mode. In this mode, each PLC node can only be part of a single group. For example, multiple PLC nodes can be part of Group 131.
- Multiple Group Membership – The network protocol supports eight different groups in this mode and each PLC node can be a part of multiple groups. For example, a single PLC node can be a part of Group 3, Group 4, and Group 7 at the same time.

Both of these membership modes can also be used together for group membership. For example, a single PLC node can be a part of Group 131 and also multiple groups such as Group 3, Group 4, and Group 7.

The group membership ID for broadcasting messages to all nodes in the network is 0x00.

The service type is always set to Unacknowledgment Mode in Group Addressing Mode. This is to avoid acknowledgment flooding on the powerline during multicast.

1.3.9 Remote Commands

In addition to sending normal data over the Powerline, the CY8CPLC10 can also send (and request) control information to (and from) another node on the network. The type of remote command to transmit is set by the TX_CommandID register and when received, is stored in the RX_CommandID register.

When a control command (Command ID = 0x01 - 0x08 and 0x0C - 0x0F) is received, the protocol will automatically process the packet (if Lock_Configuration is '0'), respond to the initiator, and notify the host of the successful transmission and reception.

When the send data command (ID 0x09) or request for data command (ID 0x0A) is received, the protocol will reply with an acknowledgment packet (if TX_Service_Type = '1'), and notify the host of the new received data. If the initiator doesn't receive the acknowledgment packet within 500ms, it will notify the host of the no acknowledgment received condition.

When a response command (ID 0x0B) is received by the initiator within 1.5s of sending the request for data command, the protocol will notify the host of the successful transmission and reception. If the response command is not received by the initiator within 1.5s, it will notify the host of the no response received condition.

The host is notified by updating the appropriate values in the INT_Status register (including Status_Value_Change).

The command IDs 0x30-0xff can be used for custom commands that would be processed by the external host (e.g. set an LED color, get a temperature/voltage reading). The available remote commands are described in Table 1-3 on page 5 with the respective Command IDs.

Table 1-3. Remote Commands (continued)

Cmd ID	Command Name	Description	Payload (TX Data)	Response (RX Data)
0x0D	SetRemote_ThresholdValue	Sets the Threshold Value at the Remote node	3-bit Remote Threshold Value	If Remote Lock Config = 0, Response = 00 (Success) If Remote Lock Config = 1, Response = 01 (Denied)
0x0E	SetRemote_GroupMembership	Sets the Group Membership of the Remote node	Byte0 - Remote SIngle Group Membership Address Byte1- Remote Multiple Group Membership Address	If Remote Lock Config = 0, Response = 00 (Success) If Remote Lock Config = 1, Response = 01 (Denied)
0x0F	GetRemote_GroupMembership	Gets the Group Membership of the Remote node	None	If Remote TX Enable = 0, Response = None If Remote TX Enable = 1, Response = Byte0 - Remote SIngle Group Membership Address Byte1- Remote Multiple Group Membership Address
0x10 - 0x2F	Reserved			
0x30 - 0xFF	User Defined Command Set			

Equations 2 and 3 are used to determine how many digital blocks are needed by a DSPWM. The total dimming resolution of a DSPWM modulator is the total of the hardware PWM modulation resolution and extra resolution added by Delta Sigma modulation in the software. Equation 3 shows that the number of digital blocks needed is only determined by the hardware resolution.

$$DigBlocks_{DSPWM} = \frac{n_{HW}}{8} \quad \text{Equation 2}$$

$$n_{Total} = n_{SW} + n_{HW} \quad \text{Equation 3}$$

These equations show that more dimming resolution is achieved with a DSPWM modulator than with a PWM or PrISM modulator. A DSPWM modulator requires more code space and execution time to use.

Equations 1, 2, and 3 determine the number of digital blocks required by one modulator. The total number of blocks for all modulators is determined by adding up the digital blocks needed by each modulator used in the device.

The CY8CLED16P01 device has a variety of LED dimming configurations. Because it has 16 digital blocks, it can implement eight 16-bit PWM modulators, eight 12-bit PrISM modulators, or sixteen 12-bit DSPWM modulators (assuming the software resolution is 4 bits). As another example, it can implement four 10-bit PrISM modulators and still have 8 digital blocks left over to implement other digital functions.

The CY8CLED16P01 is a one-device solution for powerline communication and HB LED control. For an application that runs powerline communication and HB LED control simultaneously, the CY8CLED16P01 can implement four 16-bit PWM modulators, four 12-bit PrISM modulators, or eight 12-bit DSPWM modulators (assuming the software resolution is 4 bits).

2.2 Color Mixing Algorithm

Code algorithms to implement color mixing functionality work well with EZ-Color controllers. Color mixing algorithms convert a set of color coordinates that specify a color into the appropriate 8-bit dimming values for the LED dimming modulators. This enables the EZ-Color controller to be communicated on a higher level and maintain desired color and brightness levels.

The basic 3-channel color mixing firmware performing 8-bit LED dimming requires three 8-bit dimming blocks. The discussion on LED dimming modulation implies that it consumes three digital blocks. The addition of a simple temperature compensation algorithm using a thermistor consumes an additional digital block and analog block (for the ADC).

If the dimming resolution is increased, the number of digital blocks needed should be calculated accordingly.

2.3 LED Temperature Compensation

Many HB LED systems need to measure analog signals. One or more thermistors are often present to measure temperatures of the system and the LEDs. The CY8CLED16P01 measures an analog signal with an analog-to-digital converter (ADC). The device can implement a variety of flexible ADC implementations. The ADCs cover a wide range of resolutions and techniques and use varied number of digital and analog block resources. For help in selecting from this multitude of ADCs, refer to application note AN2239, *Analog – ADC Selection* on http://www.cypress.com. When designing with an EZ-Color device, the number of digital and analog blocks used by an ADC must be factored into the total number of digital and analog blocks that are used.

In a typical case, such as the 3-channel color mixing firmware IP developed by Cypress, the simple 8-bit incremental ADC is used. This module occupies one digital and one switched capacitor analog block.

Analog blocks come in two types: continuous time and switched capacitor blocks. The former enables continuous time functions such as comparators and programmable gain amplifiers. The switched capacitor blocks enable functions such as ADCs and filters.

Temperature sensors with an I^2C interface can also be used instead of raw thermistors, thereby eliminating the need for ADCs and complicated processing.

2.4 ColorLock Algorithm

ColorLock functionality uses feedback from an optical sensor in the system to adjust the LED dimming modulators correctly to “lock on” to a target color. This is similar to the concept of temperature compensation because it compensates for change in color. Instead of indirectly measuring change in color through temperature, it senses actual change in color and compensates for it.

The ColorLock algorithm implemented by Cypress requires the use of 10 digital blocks. Due to a 9-bit PrISM implementation, 6 digital blocks are used for dimming as in Equation 1. A 16-bit PWM and two 8-bit timers are also used to form the frame generator, pulse counter, and debounce counter.

2.5 Digital Communication

Most HB LED-based lighting systems require some form of digital communication to send and receive data to and from the light fixtures to control them. The CY8CLED16P01 is a one-device solution for HB LED lighting control and powerline communication. However, the CY8CLED16P01 supports several other data communication protocols, apart from powerline communication. These are listed in Table 2-1. Some of the hardware is dedicated for a protocol and does not use any digital blocks. Some protocols use digital blocks to implement the communication.

A DMX512 protocol receiver can be implemented using two digital blocks. This is a standard protocol that is common in stage and concert lighting systems. The receiver has a software programmable address and programmable number of channels that it can control. A typical DMX512 receiver implementation (developed by Cypress) controlling three LED channels consumes five digital blocks (three for the LED modulators).

Table 2-1. Digital Communication Resource Usage

Data Protocol	Digital Blocks	Communication Digital Blocks
DMX512 (Receiver)	2	1
DALI (Slave)	3	0
I^2C Master or Slave	0	0
Half Duplex UART	1	1
SPI Master or Slave	1	1

DALI is another lighting communication protocol that is common for large commercial buildings. The DALI slave can be implemented in EZ-Color consuming six digital blocks (three for the DALI slave and three to modulate 3 LED channels). The three blocks used to implement DALI need not be communication blocks as the Manchester encoding is performed in the software.

Apart from these specific lighting communication protocols, the industry standard communication protocols such as I^2C, UART, and SPI can be implemented in any of the devices in the family. As examples, SPI can be used to interface to external WUSB devices, while I^2C can be used to interface to external microcontrollers.

Table 2-1 also shows the number of digital block resources that each type of communication block consumes.

2.6 Other Functions

The CY8CLED16P01 is capable of functions other than those previously discussed. Most functions that can be implemented with a standard microcontroller can be also implemented with the CY8CLED16P01.

Similar to regular PSoC devices, the CY8CLED16P01 also has dynamic reconfiguration ability. This is a technique that enables the device's digital and analog resources to be reused for different functions that may not be available simultaneously. For instance, consider the application to remotely control LED color/intensity (with current feedback) over powerlines using the CY8CLED16P01 for both PLC and LED color control. The PLC functionality and the current feedback do not necessarily need to happen at the same time. Therefore, the digital and analog blocks that implement the PLC functionality can dynamically reconfigure into resources that implement current feedback. By doing this, the CY8CLED16P01 device gets more functionality out of a fixed number of resources than would otherwise be possible. The only constraint on this technique is the amount of Flash and SRAM size required for the code to implement these functions. For more details on dynamic reconfiguration, refer to application note AN2104, *PSoC Dynamic Reconfiguration*.

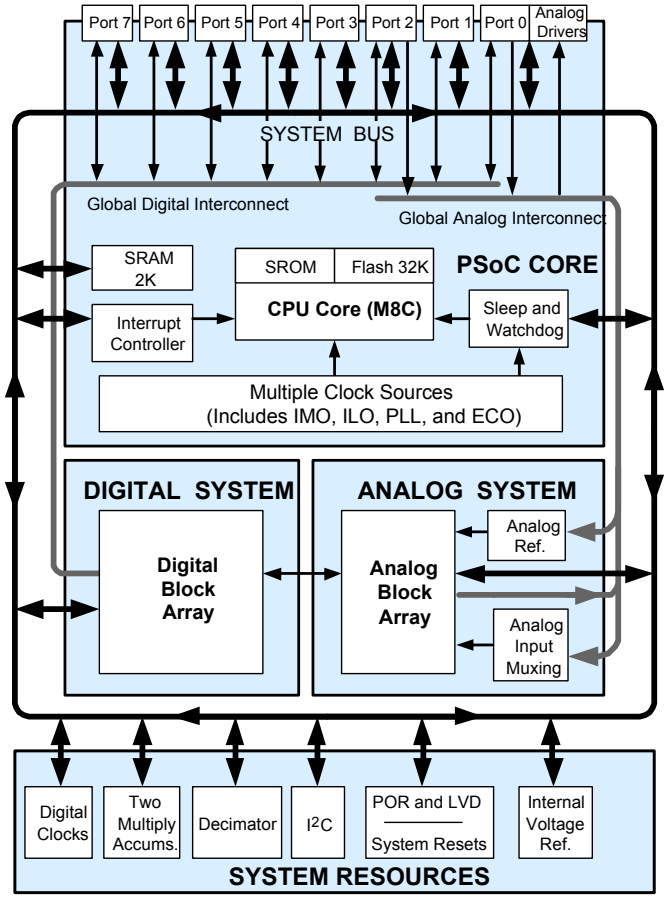
3. PSoC Core

The CY8CLED16P01 is based on the Cypress PSoC® 1 architecture. The PSoC platform consists of many *Programmable System-on-chip Controller* devices. These devices are designed to replace multiple traditional MCU-based system components with one, low cost single-chip programmable device. PSoC devices include configurable blocks of analog and digital logic, and programmable interconnects. This architecture enables the user to create customized peripheral configurations that match the requirements of each individual application. Additionally, a fast CPU, Flash program memory, SRAM data memory, and configurable I/Os are included in a range of convenient pinouts and packages.

The PSoC architecture, as shown in Figure 3-1., consists of four main areas: PSoC Core, Digital System, Analog System, and System Resources. Configurable global busing enables all the device resources to be combined into a complete custom system. The CY8CLED16P01 family can have up to five I/O ports that connect to the global digital and analog interconnects, providing access to 16 digital blocks and 12 analog blocks.

The PSoC Core is a powerful engine that supports a rich feature set. The core includes a CPU, memory, clocks, and configurable GPIO (General Purpose I/O).

Figure 3-1. PSoC Architecture



The M8C CPU core is a powerful processor with speeds up to 24 MHz, providing a 4 MIPS 8-bit Harvard architecture microprocessor. The CPU uses an interrupt controller with 25 vectors, to simplify programming of realtime embedded events. Program execution is timed and protected using the included Sleep and Watchdog timers (WDT).

Memory encompasses 32 KB of Flash for program storage, 2 KB of SRAM for data storage, and up to 2 KB of EEPROM emulated using Flash. Program Flash uses four protection levels on blocks of 64 bytes, enabling customized software IP protection.

The PSoC device incorporates flexible internal clock generators, including a 24 MHz IMO (internal main oscillator) accurate to 2.5 percent over temperature and voltage. The 24 MHz IMO can also be doubled to 48 MHz for the digital system use. A low power 32 kHz ILO (internal low speed oscillator) is provided for the sleep timer and WDT. If crystal accuracy is desired, the ECO (32.768 kHz external crystal oscillator) is available for use as a Real Time Clock (RTC) and can optionally generate a crystal-accurate 24 MHz system clock using a PLL. When operating the Powerline Transceiver (PLT) user module, the ECO must be selected to ensure accurate protocol timing. The clocks, together with programmable clock dividers (as a System Resource), provide the flexibility to integrate almost any timing requirement into the PSoC device.

PSoC GPIOs provide connection to the CPU, digital, and analog resources of the device. Each pin's drive mode may be selected from eight options, enabling great flexibility in external interfacing. Every pin also has the capability to generate a system interrupt on high level, low level, and change from last read.

8. Pin Information

The CY8CLED16P01 PLC device is available in a variety of packages which are listed and illustrated in the following tables. Every port pin (labeled with a “P”) is capable of Digital I/O. However, Vss, Vdd, and XRES are not capable of Digital I/O.

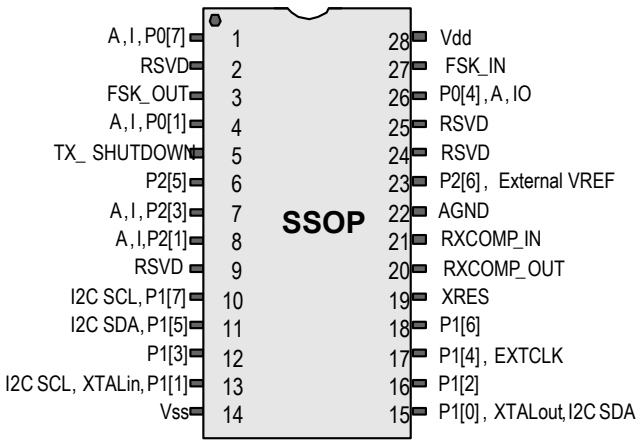
8.1 28-Pin Part Pinout

Table 8-1. 28-Pin Part Pinout (SSOP)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	IO	I	P0[7]	Analog Column Mux Input
2	Reserved		RSVD	Reserved
3		O	FSK_OUT	Analog FSK Output
4	IO	I	P0[1]	Analog Column Mux Input
5	O		TX_SHUT DOWN	Output to disable PLC transmit circuitry in receive mode Logic ‘0’ - When the Modem is trans-mitting Logic ‘1’ - When the Modem is not transmitting
6	IO		P2[5]	
7	IO	I	P2[3]	Direct switched capacitor block input
8	IO	I	P2[1]	Direct switched capacitor block input
9	Reserved		RSVD	Reserved
10	IO		P1[7]	I2C Serial Clock (SCL)
11	IO		P1[5]	I2C Serial Data (SDA)
12	IO		P1[3]	XTAL_STABILITY. Connect a 0.1 uF capacitor between the pin and VSS.
13	IO		P1[1]	Crystal (XTALin)[2], ISSP-SCLK[1], I2C SCL
14	Power		Vss	Ground connection.
15	IO		P1[0]	Crystal (XTALout)[2], ISSP-SDATA[1], I2C SDA
16	IO		P1[2]	
17	IO		P1[4]	Optional External Clock Input (EXTCLK)[2]
18	IO		P1[6]	
19	Input		XRES	Active high external reset with internal pull down
20		O	RXCOMP_ OUT	Analog Output to external Low Pass Filter Circuitry
21		I	RXCOMP_ IN	Analog Input from the external Low Pass Filter Circuitry
22	Analog Ground		AGND	Analog Ground
23	IO		P2[6]	External Voltage Reference (VREF)
24	Reserved		RSVD	Reserved
25	Reserved		RSVD	Reserved
26	IO	IO	P0[4]	Analog column mux input and column output
27		I	FSK_IN	Analog FSK Input
28	Power		Vdd	Supply Voltage

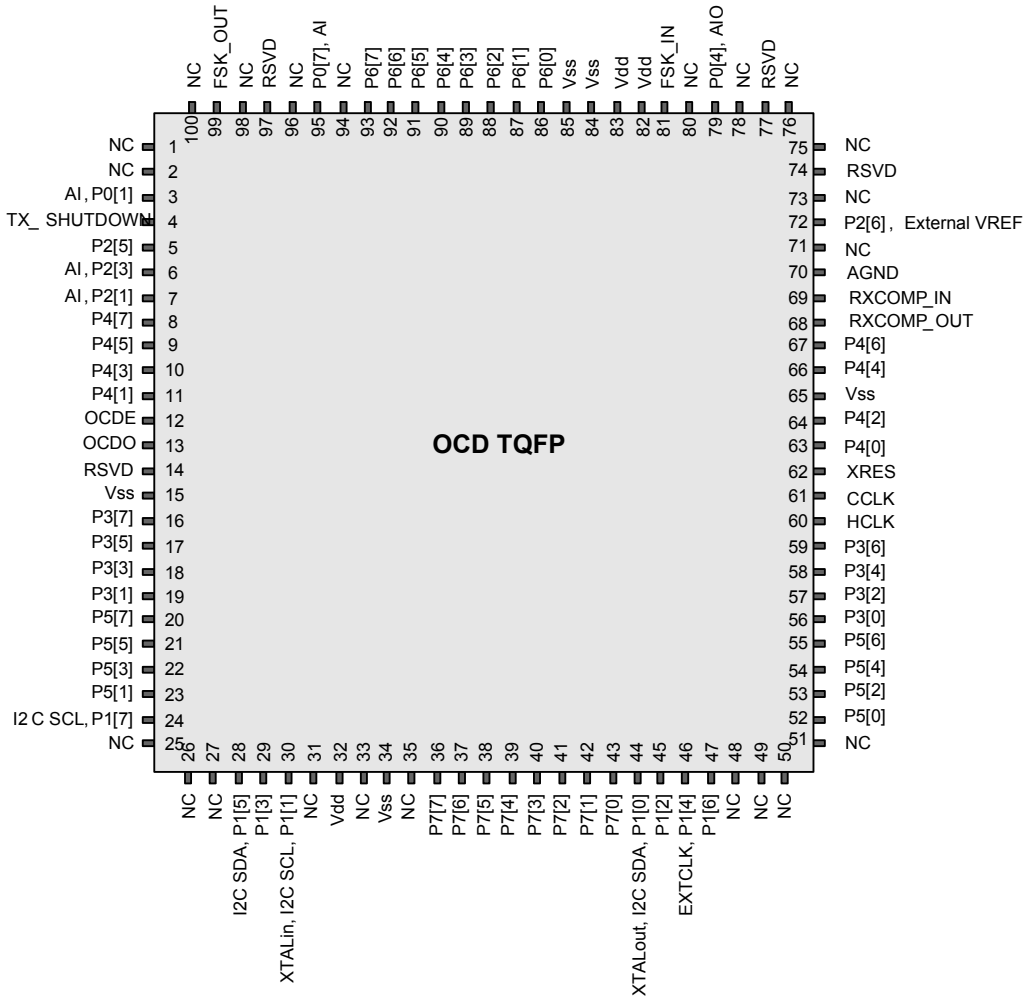
LEGEND: A = Analog, I = Input, O = Output, and RSVD = Reserved (should be left unconnected).

Figure 8-1. CY8CLED16P01 28-Pin PLC Device



Notes
1. These are the ISSP pins, which are not High Z at POR (Power On Reset). See the *PSoC Technical Reference Manual* for details.
2. When using the PLT user module, the external crystal is always required for protocol timing. For the FSK modem, either the PLL Mode should be enabled or the external 24MHz on P1[4] should be selected. The IMO should not be used.

Figure 8-3. CY8CLED16P01-OCD



Not for Production

Table 9-1. Register Map Bank 0 Table: User Space (continued)

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
DCB02DR2	2A	RW		6A		MUL1_DH	AA	R	MUL0_DH	EA	R
DCB02CR0	2B	#		6B		MUL1_DL	AB	R	MUL0_DL	EB	R
DCB03DR0	2C	#	TMP_DR0	6C	RW	ACC1_DR1	AC	RW	ACC0_DR1	EC	RW
DCB03DR1	2D	W	TMP_DR1	6D	RW	ACC1_DR0	AD	RW	ACC0_DR0	ED	RW
DCB03DR2	2E	RW	TMP_DR2	6E	RW	ACC1_DR3	AE	RW	ACC0_DR3	EE	RW
DCB03CR0	2F	#	TMP_DR3	6F	RW	ACC1_DR2	AF	RW	ACC0_DR2	EF	RW
DBB10DR0	30	#	ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
DBB10DR1	31	W	ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
DBB10DR2	32	RW	ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
DBB10CR0	33	#	ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
DBB11DR0	34	#	ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
DBB11DR1	35	W	ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
DBB11DR2	36	RW	ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
DBB11CR0	37	#	ACB01CR2	77	RW		B7		CPU_F	F7	RL
DCB12DR0	38	#	ACB02CR3	78	RW	RDI1RI	B8	RW		F8	
DCB12DR1	39	W	ACB02CR0	79	RW	RDI1SYN	B9	RW		F9	
DCB12DR2	3A	RW	ACB02CR1	7A	RW	RDI1IS	BA	RW		FA	
DCB12CR0	3B	#	ACB02CR2	7B	RW	RDI1LT0	BB	RW		FB	
DCB13DR0	3C	#	ACB03CR3	7C	RW	RDI1LT1	BC	RW		FC	
DCB13DR1	3D	W	ACB03CR0	7D	RW	RDI1RO0	BD	RW		FD	
DCB13DR2	3E	RW	ACB03CR1	7E	RW	RDI1RO1	BE	RW	CPU_SCR1	FE	#
DCB13CR0	3F	#	ACB03CR2	7F	RW		BF		CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed. # Access is bit specific.

Table 9-2. Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW	DBB20FN	40	RW	ASC10CR0	80	RW	RDI2RI	C0	RW
PRT0DM1	01	RW	DBB20IN	41	RW	ASC10CR1	81	RW	RDI2SYN	C1	RW
PRT0IC0	02	RW	DBB20OU	42	RW	ASC10CR2	82	RW	RDI2IS	C2	RW
PRT0IC1	03	RW		43		ASC10CR3	83	RW	RDI2LT0	C3	RW
PRT1DM0	04	RW	DBB21FN	44	RW	ASD11CR0	84	RW	RDI2LT1	C4	RW
PRT1DM1	05	RW	DBB21IN	45	RW	ASD11CR1	85	RW	RDI2RO0	C5	RW
PRT1IC0	06	RW	DBB21OU	46	RW	ASD11CR2	86	RW	RDI2RO1	C6	RW
PRT1IC1	07	RW		47		ASD11CR3	87	RW		C7	
PRT2DM0	08	RW	DCB22FN	48	RW	ASC12CR0	88	RW	RDI3RI	C8	RW
PRT2DM1	09	RW	DCB22IN	49	RW	ASC12CR1	89	RW	RDI3SYN	C9	RW
PRT2IC0	0A	RW	DCB22OU	4A	RW	ASC12CR2	8A	RW	RDI3IS	CA	RW
PRT2IC1	0B	RW		4B		ASC12CR3	8B	RW	RDI3LT0	CB	RW
PRT3DM0	0C	RW	DCB23FN	4C	RW	ASD13CR0	8C	RW	RDI3LT1	CC	RW
PRT3DM1	0D	RW	DCB23IN	4D	RW	ASD13CR1	8D	RW	RDI3RO0	CD	RW
PRT3IC0	0E	RW	DCB23OU	4E	RW	ASD13CR2	8E	RW	RDI3RO1	CE	RW
PRT3IC1	0F	RW		4F		ASD13CR3	8F	RW		CF	
PRT4DM0	10	RW	DBB30FN	50	RW	ASD20CR0	90	RW	GDI_O_IN	D0	RW
PRT4DM1	11	RW	DBB30IN	51	RW	ASD20CR1	91	RW	GDI_E_IN	D1	RW
PRT4IC0	12	RW	DBB30OU	52	RW	ASD20CR2	92	RW	GDI_O_OU	D2	RW
PRT4IC1	13	RW		53		ASD20CR3	93	RW	GDI_E_OU	D3	RW
PRT5DM0	14	RW	DBB31FN	54	RW	ASC21CR0	94	RW		D4	
PRT5DM1	15	RW	DBB31IN	55	RW	ASC21CR1	95	RW		D5	
PRT5IC0	16	RW	DBB31OU	56	RW	ASC21CR2	96	RW		D6	
PRT5IC1	17	RW		57		ASC21CR3	97	RW		D7	
PRT6DM0	18	RW	DCB32FN	58	RW	ASD22CR0	98	RW		D8	
PRT6DM1	19	RW	DCB32IN	59	RW	ASD22CR1	99	RW		D9	
PRT6IC0	1A	RW	DCB32OU	5A	RW	ASD22CR2	9A	RW		DA	
PRT6IC1	1B	RW		5B		ASD22CR3	9B	RW		DB	
PRT7DM0	1C	RW	DCB33FN	5C	RW	ASC23CR0	9C	RW		DC	
PRT7DM1	1D	RW	DCB33IN	5D	RW	ASC23CR1	9D	RW	OSC_GO_EN	DD	RW
PRT7IC0	1E	RW	DCB33OU	5E	RW	ASC23CR2	9E	RW	OSC_CR4	DE	RW
PRT7IC1	1F	RW		5F		ASC23CR3	9F	RW	OSC_CR3	DF	RW
DBB00FN	20	RW	CLK_CR0	60	RW		A0		OSC_CR0	E0	RW
DBB00IN	21	RW	CLK_CR1	61	RW		A1		OSC_CR1	E1	RW
DBB00OU	22	RW	ABF_CR0	62	RW		A2		OSC_CR2	E2	RW
	23		AMD_CR0	63	RW		A3		VLT_CR	E3	RW
DBB01FN	24	RW		64			A4		VLT_CMP	E4	R

Blank fields are Reserved and should not be accessed. # Access is bit specific.

10. Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8CLED16P01 device. For the most up to date electrical specifications, confirm that you have the most recent data sheet by going to the web at http://www.cypress.com.

Specifications are valid for -40°C ≤ T_A ≤ 85°C and T_J ≤ 100°C, except where noted.

The following table lists the units of measure that are used in this section.

Table 10-1. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
°C	degrees Celsius	µW	microwatts
dB	decibels	mA	milliamperes
fF	femtofarads	ms	milliseconds
Hz	hertz	mV	millivolts
KB	1024 bytes	nA	nanoamperes
Kbit	1024 bits	ns	nanoseconds
kHz	kilohertz	nV	nanovolts
kΩ	kilohms	Ω	ohms
MHz	megahertz	pA	picoamperes
MΩ	megaohms	pF	picofarads
µA	microamperes	pp	peak-to-peak
µF	microfarads	ppm	parts per million
µH	microhenrys	ps	picoseconds
µs	microseconds	sps	samples per second
µV	microvolts	σ	sigma: one standard deviation
µVrms	microvolts root-mean-square	V	volts

10.1 Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 10-2. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units	Notes
T_{STG}	Storage Temperature	-55	25	+100	°C	Higher storage temperatures reduce data retention time. Recommended storage temperature is +25°C ± 25°C. Extended duration storage temperatures above 65°C degrade reliability.
T_A	Ambient Temperature with Power Applied	-40	–	+85	°C	
Vdd	Supply Voltage on Vdd Relative to Vss	-0.5	–	+6.0	V	
V_{IO}	DC Input Voltage	Vss - 0.5	–	Vdd + 0.5	V	
V_{IOZ}	DC Voltage Applied to Tri-state	Vss - 0.5	–	Vdd + 0.5	V	
I_{MIO}	Maximum Current into any Port Pin	-25	–	+50	mA	
I_{MAIO}	Maximum Current into any Port Pin Configured as Analog Driver	-50	–	+50	mA	
ESD	Electro Static Discharge Voltage	2000	–	–	V	Human Body Model ESD
LU	Latch-up Current	–	–	200	mA	

10.3.9 DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 10-12. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
I_{DDP}	Supply Current During Programming or Verify	–	10	30	mA	
V_{ILP}	Input Low Voltage During Programming or Verify	–	–	0.8	V	
V_{IHP}	Input High Voltage During Programming or Verify	2.2	–	–	V	
I_{ILP}	Input Current when Applying V_{ILP} to P1[0] or P1[1] During Programming or Verify	–	–	0.2	mA	Driving internal pull down resistor
I_{IHP}	Input Current when Applying V_{IHP} to P1[0] or P1[1] During Programming or Verify	–	–	1.5	mA	Driving internal pull down resistor
V_{OLV}	Output Low Voltage During Programming or Verify	–	–	Vss + 0.75	V	
V_{OHV}	Output High Voltage During Programming or Verify	Vdd - 1.0	–	Vdd	V	
$Flash_{ENPB}$	Flash Endurance (per block)	50,000	–	–	–	Erase/write cycles per block
$Flash_{ENT}$	Flash Endurance (total)[5]	1,800,000	–	–	–	Erase/write cycles
$Flash_{DR}$	Flash Data Retention	10	–	–	Years	

10.4 AC Electrical Characteristics

10.4.1 AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

Note See the individual user module data sheets for information on maximum frequencies for user modules.

Table 10-13. AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{IMO24}	Internal Main Oscillator Frequency for 24 MHz	23.4	24	24.6	MHz	Trimmed for 5V operation using factory trim values. SLIMO Mode = 0.
F_{IMO6}	Internal Main Oscillator Frequency for 6 MHz	5.5	6	6.5[6]	MHz	Trimmed for 5V operation using factory trim values. SLIMO Mode = 1.
F_{CPU1}	CPU Frequency (5V Nominal)	0.93	24	24.6[6]	MHz	
F_{48M}	Digital PSoC Block Frequency	0	48	49.2[6, 7]	MHz	Refer to the AC Digital Block Specifications below.
F_{32K1}	Internal Low Speed Oscillator Frequency	15	32	64	kHz	
F_{32K2}	External Crystal Oscillator	–	32.768	–	kHz	Accuracy is capacitor and crystal dependent. 50% duty cycle.

Notes
5. A maximum of 36 x 50,000 block endurance cycles is allowed. This may be balanced between operations on 36x1 blocks of 50,000 maximum cycles each, 36x2 blocks of 25,000 maximum cycles each, or 36x4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36x50,000 and that no single block ever sees more than 50,000 cycles). For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 at http://www.cypress.com under Application Notes for more information.
6. Accuracy derived from Internal Main Oscillator with appropriate trim for Vdd range.
7. See the individual user module data sheets for information on maximum frequencies for user modules.

Table 10-13. AC Chip-Level Specifications (continued)

Symbol	Description	Min	Typ	Max	Units	Notes
F_{32K_U}	Internal Low Speed Oscillator (ILO) Untrimmed Frequency	5	–	–	kHz	After a reset and before the m8c starts to run, the ILO is not trimmed. See the System Resets section of the PSoC Technical Reference Manual for details on timing this.
F_{PLL}	PLL Frequency	–	23.986	–	MHz	A multiple (x732) of crystal frequency.
Jitter24M2	24 MHz Period Jitter (PLL)	–	–	600	ps	
$T_{PLLSLEW}$	PLL Lock Time	0.5	–	10	ms	
$T_{PLLSLEWLOW}$	PLL Lock Time for Low Gain Setting	0.5	–	50	ms	
T_{OS}	External Crystal Oscillator Startup to 1%	–	250	500	ms	
T_{OSACC}	External Crystal Oscillator Startup to 100 ppm	–	300	600	ms	The crystal oscillator frequency is within 100 ppm of its final value by the end of the T_{OSACC} period. Correct operation assumes a properly loaded 1 µW maximum drive level 32.768 kHz crystal. -40°C ≤ T_A ≤ 85°C.
Jitter32k	32 kHz Period Jitter	–	100		ns	
T_{XRST}	External Reset Pulse Width	10	–	–	µs	
DC24M	24 MHz Duty Cycle	40	50	60	%	
DC_{ILO}	Internal Low Speed Oscillator Duty Cycle	20	50	80	%	
Step24M	24 MHz Trim Step Size	–	50	–	kHz	
Fout48M	48 MHz Output Frequency	46.8	48.0	49.2	MHz	Trimmed using factory trim values.
Jitter24M1	24 MHz Period Jitter (IMO)	–	600		ps	
F_{MAX}	Maximum frequency of signal on row input or row output.	–	–	12.3	MHz	
SR_{POWER_UP}	Power Supply Slew Rate	–	–	250	V/ms	Vdd slew rate during power up.
$T_{POWERUP}$	Time from end of POR to CPU executing code	–	16	100	ms	Power up from 0V. See the System Resets section of the PSoC Technical Reference Manual.

Figure 10-1. PLL Lock Timing Diagram

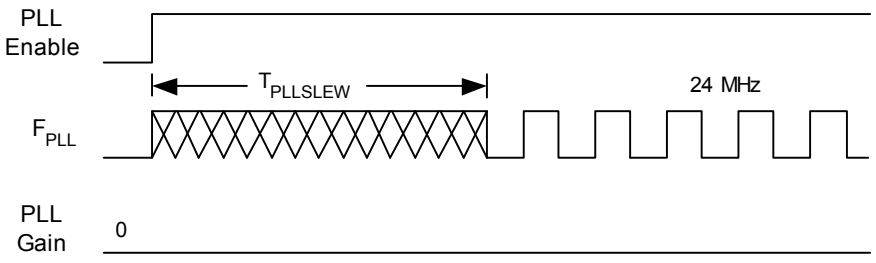


Figure 10-2. PLL Lock for Low Gain Setting Timing Diagram

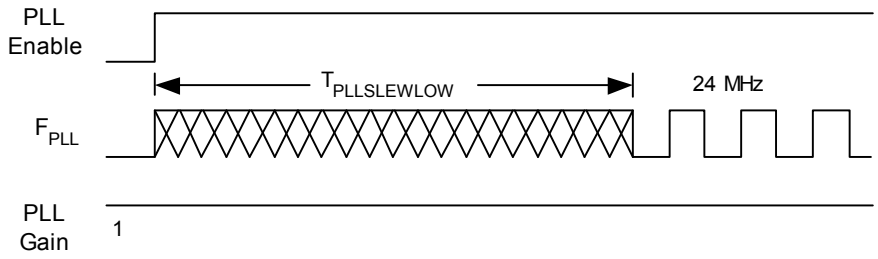


Figure 10-3. External Crystal Oscillator Startup Timing Diagram

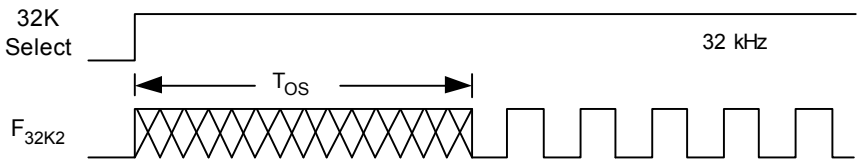


Figure 10-4. 24 MHz Period Jitter (IMO) Timing Diagram

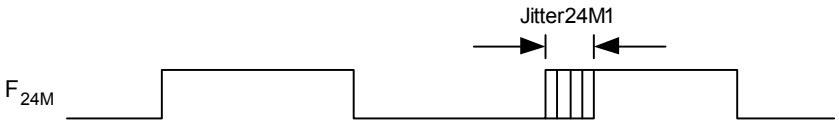
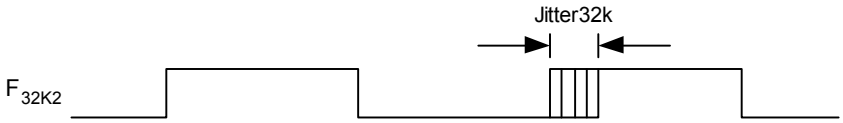


Figure 10-5. 32 kHz Period Jitter (ECO) Timing Diagram



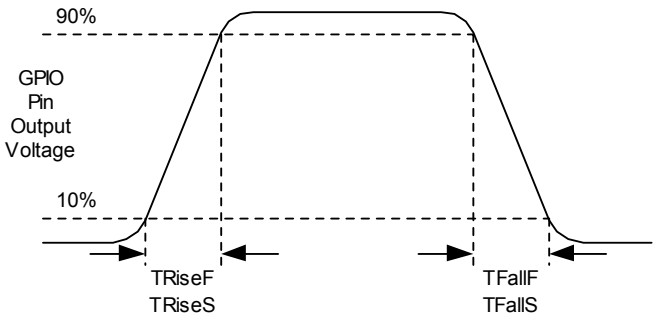
10.4.2 AC General Purpose IO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 10-14. AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO Operating Frequency	0	–	12.3	MHz	Normal Strong Mode
TRiseF	Rise Time, Normal Strong Mode, Cload = 50 pF	3	–	18	ns	10% - 90%
TFallF	Fall Time, Normal Strong Mode, Cload = 50 pF	2	–	18	ns	10% - 90%
TRiseS	Rise Time, Slow Strong Mode, Cload = 50 pF	10	27	–	ns	10% - 90%
TFallS	Fall Time, Slow Strong Mode, Cload = 50 pF	10	22	–	ns	10% - 90%

Figure 10-6. GPIO Timing Diagram



10.4.3 AC Operational Amplifier Specifications

Table 10-15 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

Settling times, slew rates, and gain bandwidth are based on the Analog Continuous Time PSoC block.

Table 10-15. 5V AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{ROA}	Rising Settling Time to 0.1% for a 1V Step (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 – – –	 – – –	 3.9 0.72 0.62	 µs µs µs	
T_{SOA}	Falling Settling Time to 0.1% for a 1V Step (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 – – –	 – – –	 5.9 0.92 0.72	 µs µs µs	
SR_{ROA}	Rising Slew Rate (20% to 80%) of a 1V Step (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 0.15 1.7 6.5	 – – –	 – – –	 V/µs V/µs V/µs	
SR_{FOA}	Falling Slew Rate (20% to 80%) of a 1V Step (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 0.01 0.5 4.0	 – – –	 – – –	 V/µs V/µs V/µs	
BW_{OA}	Gain Bandwidth Product Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 0.75 3.1 5.4	 – – –	 – – –	 MHz MHz MHz	
E_{NOA}	Noise at 1 kHz (Power = Medium, Opamp Bias = High)	–	100	–	nV/rt-Hz	

When bypassed by a capacitor on P2[4], the noise of the analog ground signal distributed to each block is reduced by a factor of up to 5 (14 dB). This is at frequencies above the corner frequency defined by the on-chip 8.1k resistance and the external capacitor.

10.4.6 AC Analog Output Buffer Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 10-18. 5V AC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{ROB}	Rising Settling Time to 0.1%, 1V Step, 100 pF Load Power = Low Power = High	 – –	 – –	 4 4	 µs µs	
T_{SOB}	Falling Settling Time to 0.1%, 1V Step, 100 pF Load Power = Low Power = High	 – –	 – –	 3.4 3.4	 µs µs	
SR_{ROB}	Rising Slew Rate (20% to 80%), 1V Step, 100 pF Load Power = Low Power = High	 0.5 0.5	 – –	 – –	 V/µs V/µs	
SR_{FOB}	Falling Slew Rate (80% to 20%), 1V Step, 100 pF Load Power = Low Power = High	 0.55 0.55	 – –	 – –	 V/µs V/µs	
BW_{OB}	Small Signal Bandwidth, 20mV_{pp}, 3 dB BW, 100 pF Load Power = Low Power = High	 0.8 0.8	 – –	 – –	 MHz MHz	
BW_{OB}	Large Signal Bandwidth, 1V_{pp}, 3 dB BW, 100 pF Load Power = Low Power = High	 300 300	 – –	 – –	 kHz kHz	

10.4.7 AC External Clock Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 10-19. 5V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency	0.093	–	24.6	MHz	
–	High Period	20.6	–	5300	ns	
–	Low Period	20.6	–	–	ns	
–	Power Up IMO to Switch	150	–	–	µs	

10.4.8 AC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 10-20. AC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{RSCLK}	Rise Time of SCLK	1	–	20	ns	
T_{FSCLK}	Fall Time of SCLK	1	–	20	ns	
T_{SSCLK}	Data Setup Time to Falling Edge of SCLK	40	–	–	ns	
T_{HSCLK}	Data Hold Time from Falling Edge of SCLK	40	–	–	ns	
F_{SCLK}	Frequency of SCLK	0	–	8	MHz	
T_{ERASEB}	Flash Erase Time (Block)	–	10	–	ms	
T_{WRITE}	Flash Block Write Time	–	40	–	ms	

Table 10-20. AC Programming Specifications (continued)

Symbol	Description	Min	Typ	Max	Units	Notes
T_{DSCLK}	Data Out Delay from Falling Edge of SCLK	–	–	45	ns	
$T_{ERASEALL}$	Flash Erase Time (Bulk)	–	80	–	ms	Erase all Blocks and protection fields at once
$T_{PROGRAM\_HOT}$	Flash Block Erase + Flash Block Write Time	–	–	100[9]	ms	0°C <= Tj <= 100°C
$T_{PROGRAM\_COLD}$	Flash Block Erase + Flash Block Write Time	–	–	200[9]	ms	-40°C <= Tj <= 0°C

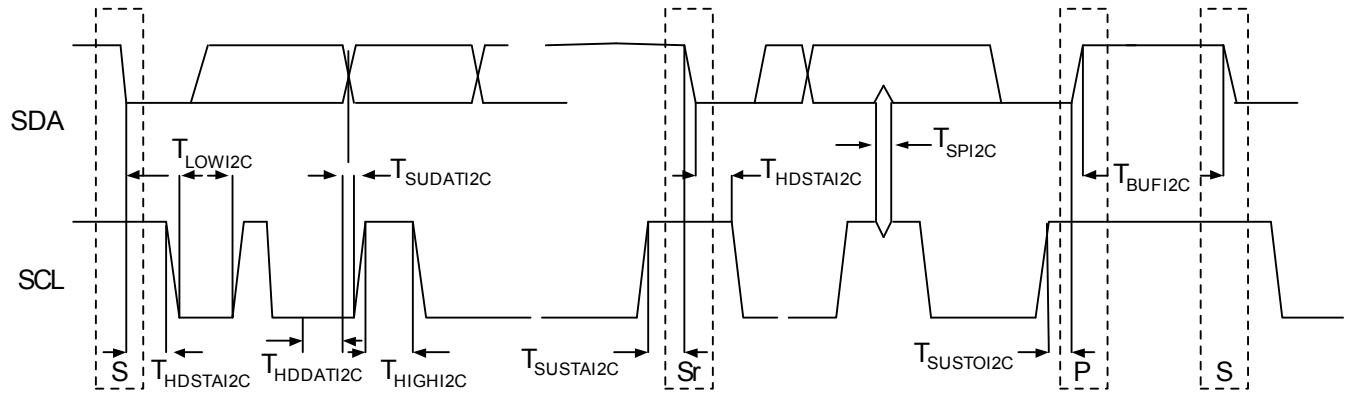
10.4.9 AC I²C Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 10-21. AC Characteristics of the I²C SDA and SCL Pins

Symbol	Description	Standard Mode		Fast Mode		Units	Notes
		Min	Max	Min	Max		
F_{SCLI2C}	SCL Clock Frequency	0	100	0	400	kHz	
$T_{HDSTAI2C}$	Hold Time (repeated) START Condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	µs	
T_{LOWI2C}	LOW Period of the SCL Clock	4.7	–	1.3	–	µs	
$T_{HIGHI2C}$	HIGH Period of the SCL Clock	4.0	–	0.6	–	µs	
$T_{SUSTAI2C}$	Setup Time for a Repeated START Condition	4.7	–	0.6	–	µs	
$T_{HDDATI2C}$	Data Hold Time	0	–	0	–	µs	
$T_{SUDATI2C}$	Data Setup Time	250	–	100[10]	–	ns	
$T_{SUSTOI2C}$	Setup Time for STOP Condition	4.0	–	0.6	–	µs	
T_{BUFI2C}	Bus Free Time Between a STOP and START Condition	4.7	–	1.3	–	µs	
T_{SPI2C}	Pulse Width of spikes are suppressed by the input filter	–	–	0	50	ns	

Figure 10-9. Definition for Timing for Fast/Standard Mode on the I²C Bus Packaging Dimensions



Notes

9. For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 at http://www.cypress.com for more information.
10. A Fast-Mode I2C-bus device can be used in a Standard-Mode I2C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If this device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the Standard-Mode I2C-bus specification) before the SCL line is released.

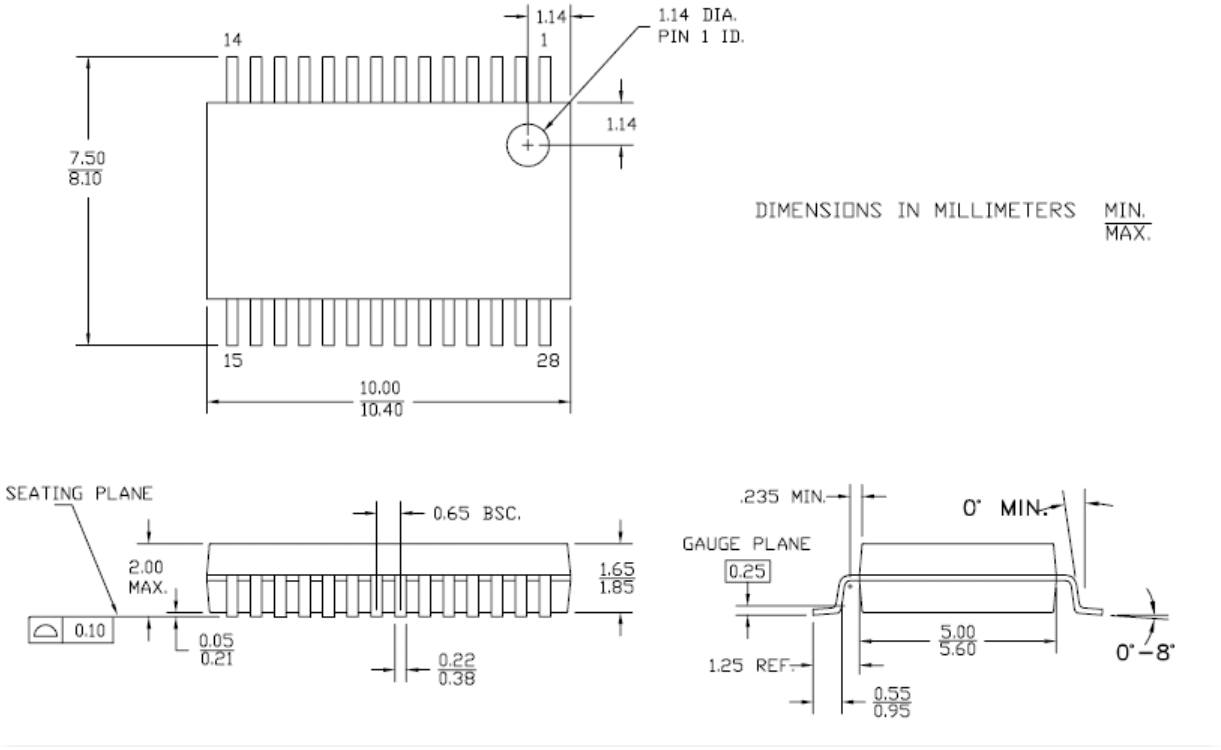
11. Packaging Information

This section illustrates the packaging specifications for the CY8CLED16P01 PLC device, along with the thermal impedances for each package, and the typical package capacitance on crystal pins.

Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the document titled *PSoC Emulator Pod Dimensions* at http://www.cypress.com/design/MR10161.

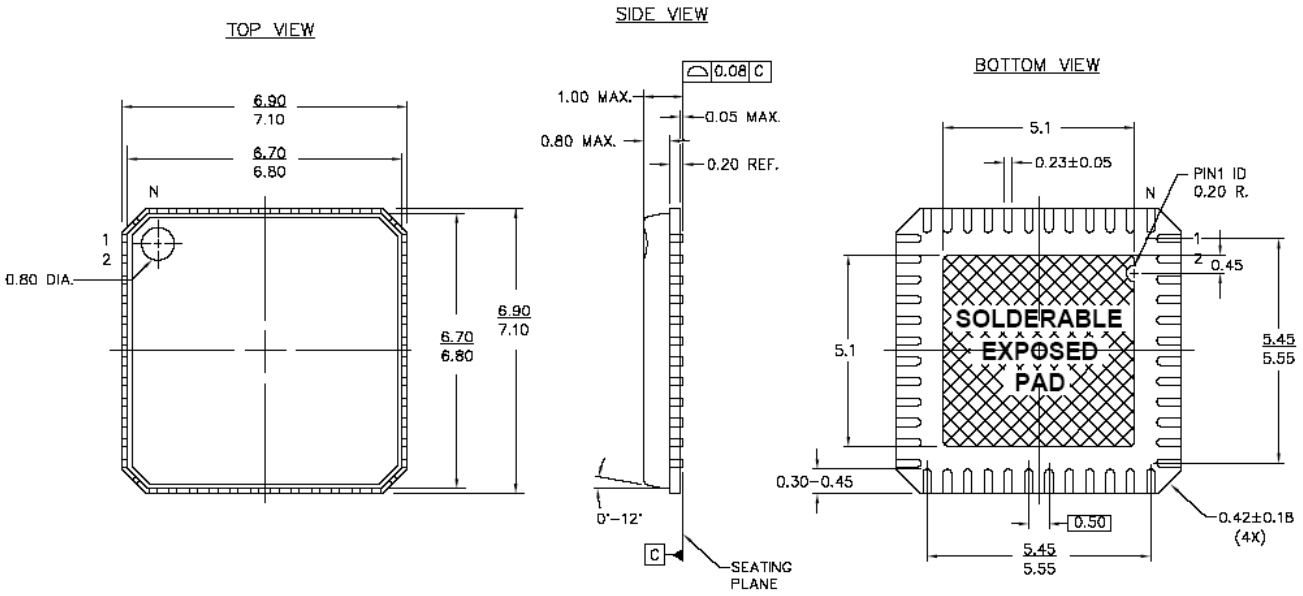
11.1 Packaging Dimensions

Figure 11-1. 28-Pin (210-Mil) SSOP



51-85079 *C

Figure 11-2. 48-Pin (7x7 mm) QFN



NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: 0.13g
4. ALL DIMENSIONS ARE IN MM [MIN/MAX]
5. PACKAGE CODE

PART #	DESCRIPTION
LF48A	STANDARD
LY48A	LEAD FREE

001-12919 *A

Important Note For information on the preferred dimensions for mounting QFN packages, see the following Application Note at http://www.amkor.com/products/notes_papers/MLFAppNote.pdf.

Important Note Pinned vias for thermal conduction are not required for the low-power PSoC devices.

12.3 Evaluation Kits

The evaluation kits do not have on-board powerline capability, but can be used with a PLC kit for evaluation purposes. All evaluation tools are sold at the Cypress Online Store.

12.3.1 CY3210-MiniProg1

The CY3210-MiniProg1 kit enables the user to program PSoC devices via the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC via a provided USB 2.0 cable. The kit includes:

- MiniProg Programming Unit
- MiniEval Socket Programming and Evaluation Board
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample
- 28-Pin CY8C27443-24PXI PDIP PSoC Device Sample
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

12.3.2 CY3210-PSoCEval1

The CY3210-PSoCEval1 kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, and plenty of bread boarding space to meet all of your evaluation needs. The kit includes:

- Evaluation Board with LCD Module
- MiniProg Programming Unit
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample (2)
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

12.3.3 CY3214-PSoCEvalUSB

The CY3214-PSoCEvalUSB evaluation kit features a development board for the CY8C24794-24LFXI PSoC device. Special features of the board include both USB and capacitive sensing development and debugging support. This evaluation board also includes an LCD module, potentiometer, LEDs, an enunciator, and plenty of bread boarding space to meet all of your evaluation needs. The kit includes:

- PSoCEvalUSB Board
- LCD Module
- MIniProg Programming Unit
- Mini USB Cable
- PSoC Designer and Example Projects CD
- Getting Started Guide
- Wire Pack

12.4 Device Programmers

All device programmers are purchased from the Cypress Online Store.

12.4.1 CY3216 Modular Programmer

The CY3216 Modular Programmer kit features a modular programmer and the MiniProg1 programming unit. The modular programmer includes three programming module cards and supports multiple Cypress products. The kit includes:

- Modular Programmer Base
- Three Programming Module Cards
- MiniProg Programming Unit
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

12.4.2 CY3207 ISSP In-System Serial Programmer (ISSP)

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production programming environment.

Note that CY3207ISSP needs special software and is not compatible with PSoC Programmer. The kit includes:

- CY3207 Programmer Unit
- PSoC ISSP Software CD
- 110 ~ 240V Power Supply, Euro-Plug Adapter
- USB 2.0 Cable

12.4.3 Third Party Tools

Several tools are specially designed by the following third party vendors to accompany PSoC devices during development and production. Specific details of each of these tools are found at http://www.cypress.com under Support.

12.4.4 Build a PSoC Emulator into Your Board

For details on emulating the circuit before going to volume production using an on-chip debug (OCD) non-production PSoC device, see Application Note AN2323 *Debugging - Build a PSoC Emulator into Your Board* at http://www.cypress.com/design/AN2323.

16. Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at www.cypress.com/go/home/order/sales.

Products

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