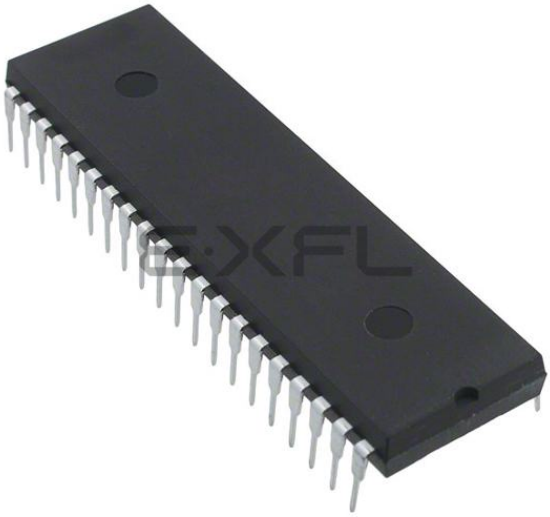

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Details	
Product Status	Last Time Buy
Core Processor	8051
Core Size	8-Bit
Speed	40MHz
Connectivity	EBI/EMI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	32
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.25K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/n78e366adg

4. PIN CONFIGURATIONS

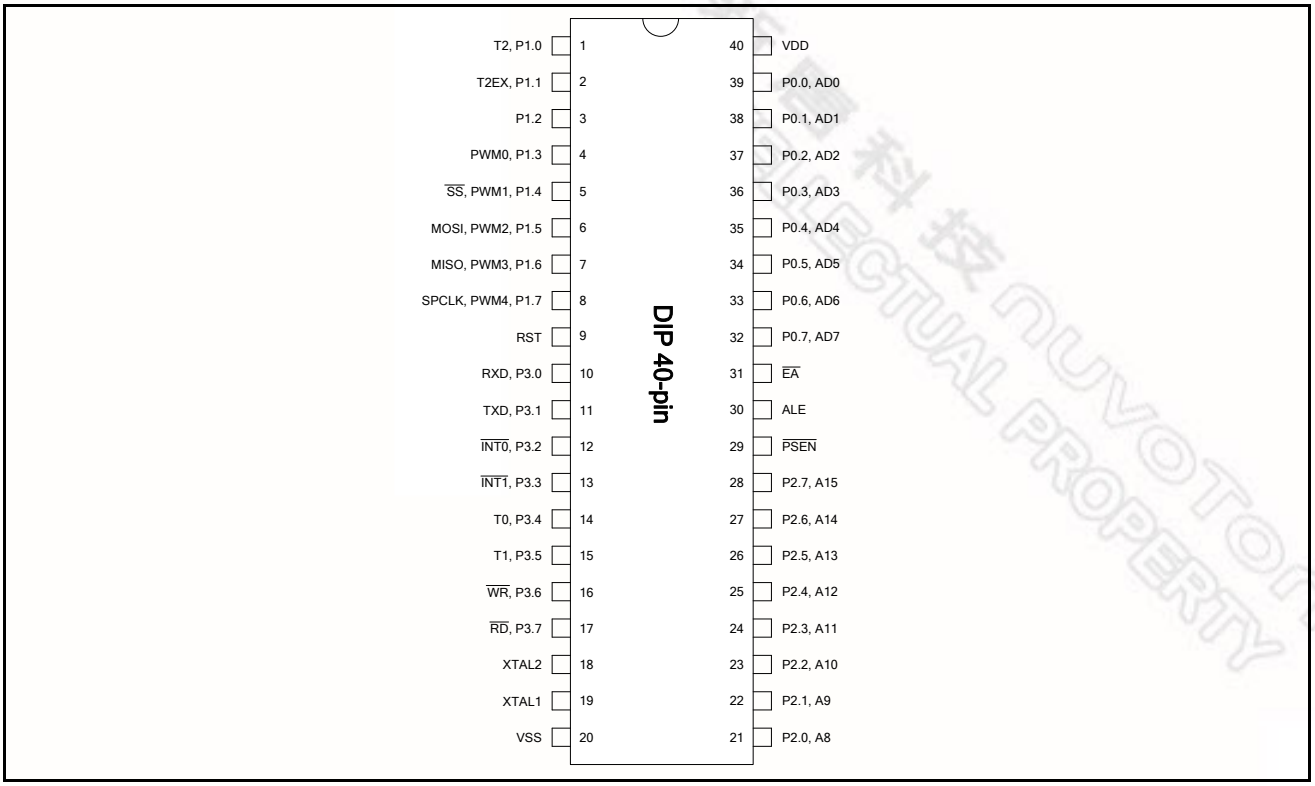

Figure 4–1. Pin Assignment of DIP 40-Pin

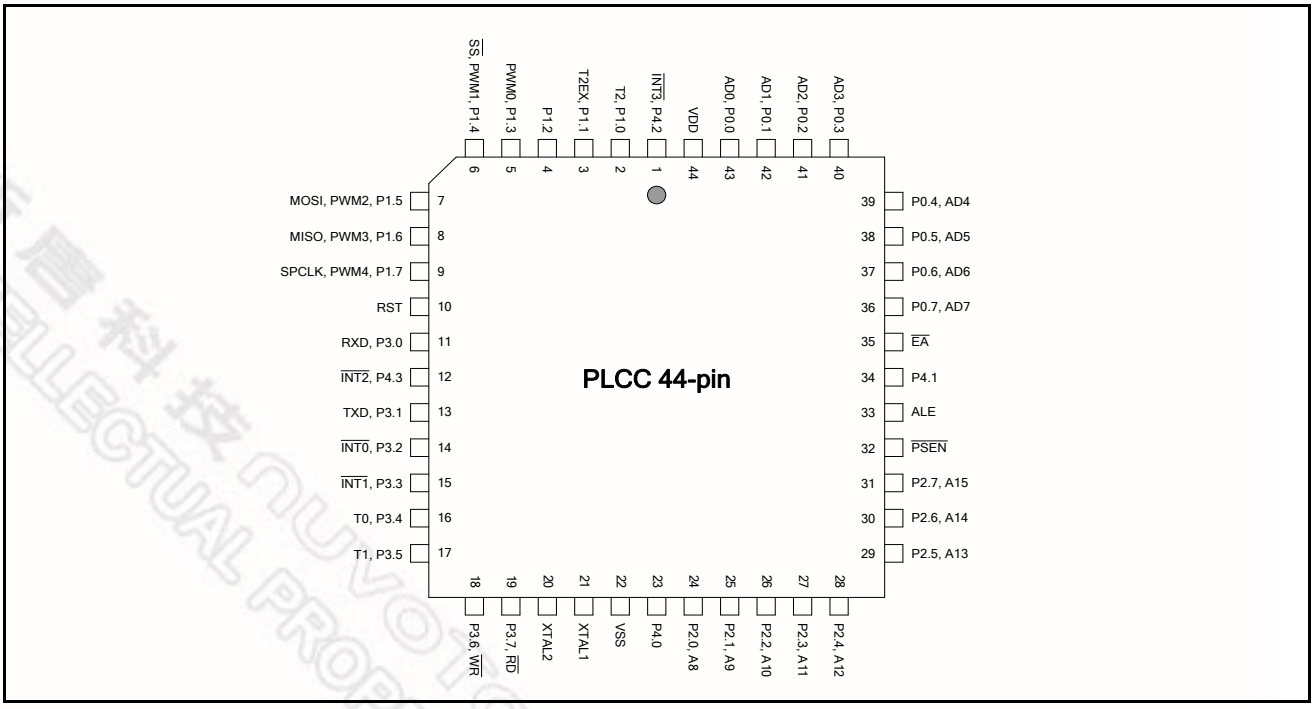

Figure 4–2. Pin Assignment of PLCC 44-Pin

The application circuit is shown below. The user is recommended follow the circuit enclosed by gray blocks to achieve the most stable and reliable operation of MCU especially in a noisy power environment for a healthy EMS immunity. If internal RC oscillator is used as the system clock, a 0.1μF capacitor should be added to gain a precise RC frequency.

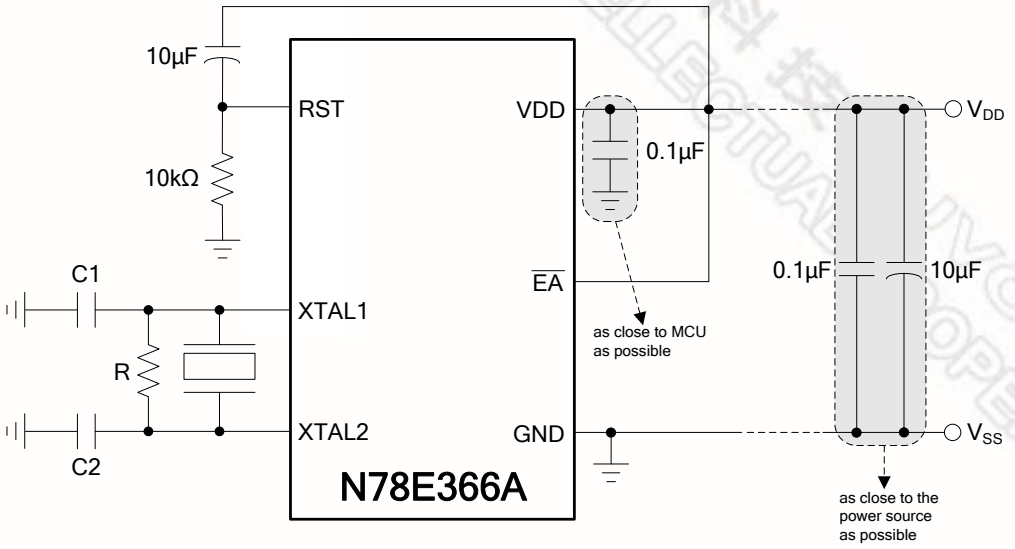

Figure 4–5. Application Circuit for Execution of Internal Program Code with External Crystal

Crystal Frequency	R	C1	C2
4MHz~33MHz	Without	Depend on crystal specifications	
33MHZ~40MHz	5kΩ~10kΩ		

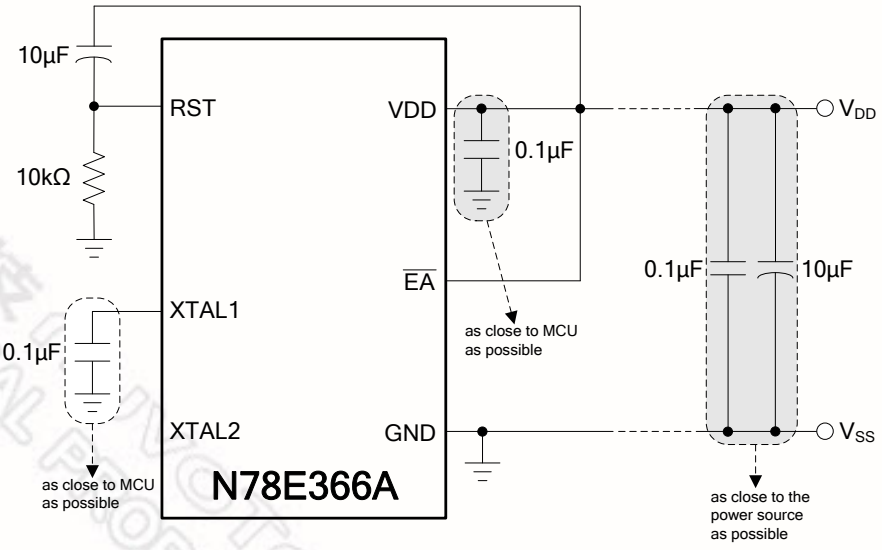

Figure 4–6. Application Circuit for Execution of Internal Program Code with Internal RC Oscillator

8. AUXILIARY RAM (XRAM)

N78E366A provides additional on-chip 1k-byte RAM called XRAM to enlarge the RAM space. It occupies the address space from 000H through 3FFH. The XRAM is enabled after all resets. The 1024 bytes of XRAM are indirectly accessed by move external instruction MOVX @DPTR or MOVX @Ri along with XRAMAH. (If XRAM is enabled, MOVX @Ri cannot be used to access external RAM anymore.) This block of XRAM shares the same logic address of 000H through 3FFH with the external RAM. A DPTR value given larger than 03FFH will map to the external RAM no matter of the value of bit XRAMEN (CHPCON.4). If the user would like to access contents within 000H to 3FFH address of the off-chip external XRAM, the XRAMEN bit should be cleared as logic 0. (Note that CHPCON is a TA writing protected SFR.) When the XRAM is accessed, the address fetching signal will not emit via P0, P2, $\overline{WR}$, and $\overline{RD}$. Note that the stack pointer cannot locate in any part of XRAM.

CHPCON – Chip Control (TA protected)

7	6	5	4	3	2	1	0
SWRST	ISPF	LDUEN	XRAMEN	-	-	BS	ISPEN
w	r/w	r/w	r/w	-	-	r/w	r/w

Address: 9FH reset value: see Table 6–2. N78E366A SFR Descriptions and Reset Values

Bit	Name	Description
4	XRAMEN	**XRAM enable.** 0 = Disable on-chip XRAM. 1 = Enable on-chip XRAM. (The default value after all resets.)

XRAMAH – XRAM Address High Byte

7	6	5	4	3	2	1	0
-	-	-	-	-	-	XRAMAH.1	XRAMAH.0
-	-	-	-	-	-	r/w	r/w

Address: A1H reset value: 0000 0000b

Bit	Name	Description
7:2	-	**Reserved.**
1:0	XRAMAH[1:0]	**XRAM address high byte.** To set the XRAM high byte address. This setting works along with MOV @Ri instructions. The demo codes are listed below.

XRAM demo code:

```
MOV     XRAMAH,#01H          ;write #5AH to XRAM with address @0123H.
MOV     R0,#23H
MOV     A,#5AH
MOVX    @R0,A

MOV     XRAMAH,#01H          ;read from XRAM with address @0123H.
MOV     R0,#23H
MOVX    A,@R0
```

9. I/O PORT STRUCTURE AND OPERATION

N78E366A has maximum five 8-bit width, bit-addressable ports P0~P4. The configuration of P1~P4 is the quasi bi-directional I/O. This type rules as both input and output. When the port outputs a logic high, it is weakly driven, allowing an external device to pull the pin low. When the pin is pulled low, it is driven strongly and able to sink a large current. In the quasi bi-directional I/O structure, there are three pull-up transistors. Each of them serves different purposes. One of these pull-ups, called the “very weak” pull-up, is turned on whenever the port latch contains a logic 1. The “very weak” pull-up sources a very small current that will pull the pin high if it is left floating.

A second pull-up, called the “weak” pull-up, is turned on when the outside port pin itself is at a logic 1 level. This pull-up provides the primary source current for a quasi bi-directional pin that is outputting a 1. If a pin that has a logic 1 on it is pulled low by an external device, the “weak” pull-up turns off, and only the “very weak” pull-up remains on. In order to pull the pin low under these conditions, the external device has to sink enough current (larger than I_{TL}) to overcome the “weak” pull-up and make the voltage on the port pin below its input threshold (lower than V_{IL}).

The third pull-up is the “strong” pull-up. This pull-up is used to speed up low-to-high transitions on a quasi bi-directional port pin when the port latch changes from a logic 0 to a logic 1. When this occurs, the strong pull-up turns on for two-peripheral-clock time in order to pull the port pin high quickly. Then it turns off and “weak: pull-up continues remaining the port pin high. The quasi bi-directional port structure is shown as below.

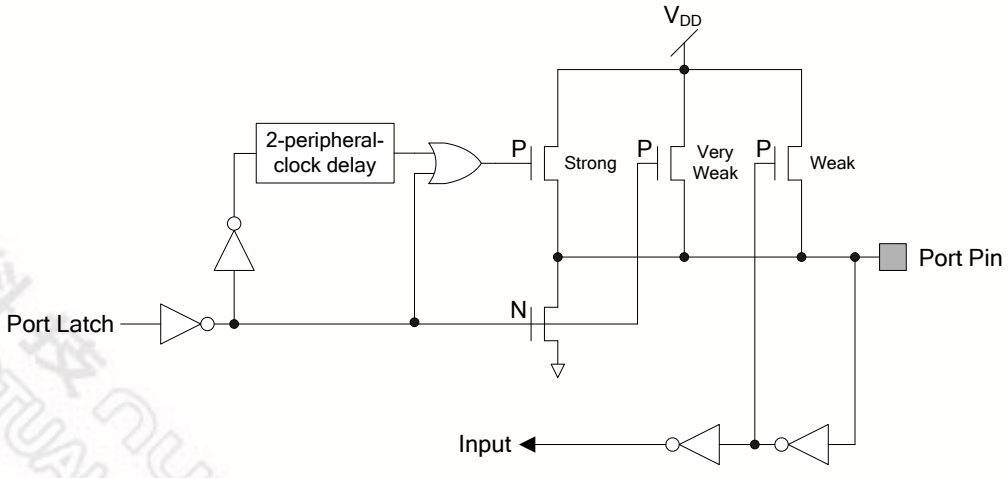

Figure 9–1. Quasi Bi-direction I/O Structure

The default configuration of P0 is open-drain structure. To serve as an I/O port the external pull-up resistor is always necessary. N78E366A also provide an internal P0 pull-up resistors for each pins. Via setting P0UP (P0OR.0) P0 will switch on its weak pull-up internally and behave the same as the quasi bi-directional I/O pins.

Bit	Name	Description
3	EXEN2	**Timer 2 external enable.** This bit enables 1-to-0 transitions on T2EX trigger. 0 = 1-to-0 transitions on T2EX is ignored. 1 = 1-to-0 transitions on T2EX will set EXF2 logic 1. If Timer 2 is configured in capture or auto-reload mode, the 1-to-0 transitions on T2EX will cause capture or reload event.
2	TR2	**Timer 2 run control.** 0 = Timer 2 is halted. Clearing this bit will halt Timer 2 and the current count will be preserved in TH2 and TL2. 1 = Timer 2 is enabled.
1	C/$\overline{T2}$	**Timer 2 Counter/Timer select.** 0 = Timer 2 is incremented by internal peripheral clocks. 1 = Timer 2 is incremented by the falling edge of the external pin T2. If Timer 2 would like to be set in clock-out mode, C/$\overline{T2}$ must be 0.
0	CP/$\overline{RL2}$	**Timer 2 Capture or Reload select.** This bit selects whether Timer 2 functions in capture or auto-reload mode. EXEN2 must be logic 1 for 1-to-0 transitions on T2EX to be recognized and used to trigger captures or reloads. If RCLK or TCLK is set, this bit is ignored and Timer 2 will function in auto-reload mode. 0 = Auto-reload on Timer 2 overflow or 1-to-0 transition on T2EX pin. 1 = Capture on 1-to-0 transition at T2EX pin.

T2MOD – Timer 2 Mode

7	6	5	4	3	2	1	0
-	-	-	-	-	-	T2OE	-
-	-	-	-	-	-	r/w	-

Address: C9H reset value: 0000 0000b

Bit	Name	Description
7:2	-	**Reserved.**
1	T2OE	**Timer 2 clock-out enable.** 0 = Disable Timer 2 clock-out function. T2 pin functions either as a standard port pin or as a counter input for Timer 2. 1 = Enable Timer 2 clock-out function. Timer 2 will drive T2 pin with a clock output if C/$\overline{T2}$ is 0.
0	-	**Reserved.**

RCAP2L – Timer 2 Reload/Capture Low Byte

7	6	5	4	3	2	1	0
RCAP2L[7:0]							
r/w							

Address: CAH reset value: 0000 0000b

Bit	Name	Description
7:0	RCAP2L[7:0]	**Timer 2 reload/capture low byte.** This register captures and stores the low byte of Timer 2 when Timer 2 is configured in capture mode. When Timer 2 is in auto-reload mode, baud rate generator mode, or clock-out mode, it holds the low byte of the reload value.

Table 10–1. Timer 2 Operating Modes

Timer 2 Mode	RCLK (T2CON.5) or TCLK (T2CON.4)	CP/$\overline{RL2}$ (T2CON.0)	T2OE (T2MOD.1)
16-bit capture[1]	0	1	0
16-bit auto-reload	0	0	0
Baud rate generator	1	X	0
Clock-out[2]	0	0	1

[1] The capture is valid while EXEN2 (T2CON.3) is a 1. Or Timer/Counter 2 behaves just like a 16-bit timer/counter.

[2] C/$\overline{T2}$ (T2CON.1) must be 0.

10.2.1 Capture Mode

The capture mode is enabled by setting the CP/$\overline{RL2}$ bit in the T2CON register to 1. In the capture mode, Timer/Counter 2 serves as a 16 bit up counter. When the counter rolls over from FFFFH to 0000H, the TF2 bit is set, which will generate an Timer 2 interrupt request. If the EXEN2 bit is set, then a negative transition of T2EX pin (alternative function of P1.1) will cause the value in the TL2 and TH2 register to be captured by the RCAP2L and RCAP2H registers. The TH2 and TL2 keeps on counting while this capture event occurs. This capture action also causes the EXF2 (T2CON.6) bit set, which will also generate an Timer 2 interrupt. If Timer 2 interrupt enabled, both TF2 and EXF2 flags will generate interrupt vectoring to the same location. The user should check which one triggers the Timer 2 interrupt in the interrupt service routine.

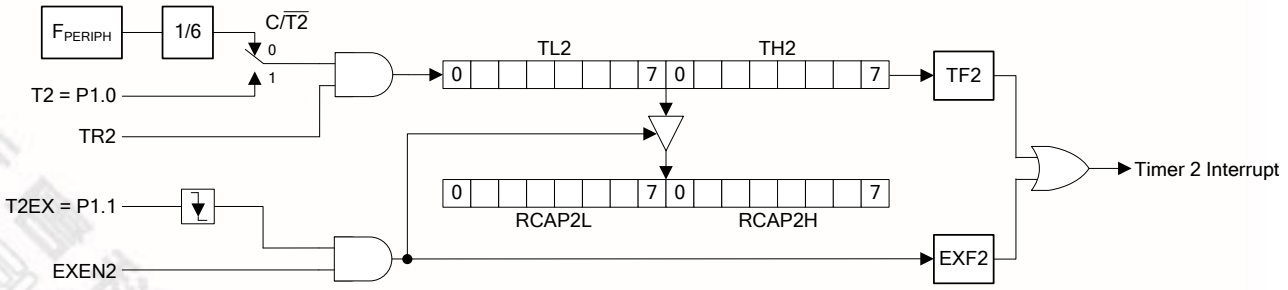

Figure 10–5. Timer/Counter 2 in Capture Mode

10.2.2 Auto-reload Mode

The auto-reload mode is enabled by clearing the CP/$\overline{RL2}$ bit in the T2CON register. In this mode, Timer/Counter 2 is a 16 bit up counter. When the counter rolls over from FFFFH, TF2 (T2CON.7) is set as 1 and a reload is generated that causes the contents of the RCAP2L and RCAP2H registers to be reloaded into the TL2 and TH2 registers respectively. If the EXEN2 bit is set, then a negative transition on T2EX pin will also cause a reload. This action also sets the EXF2 bit in T2CON.

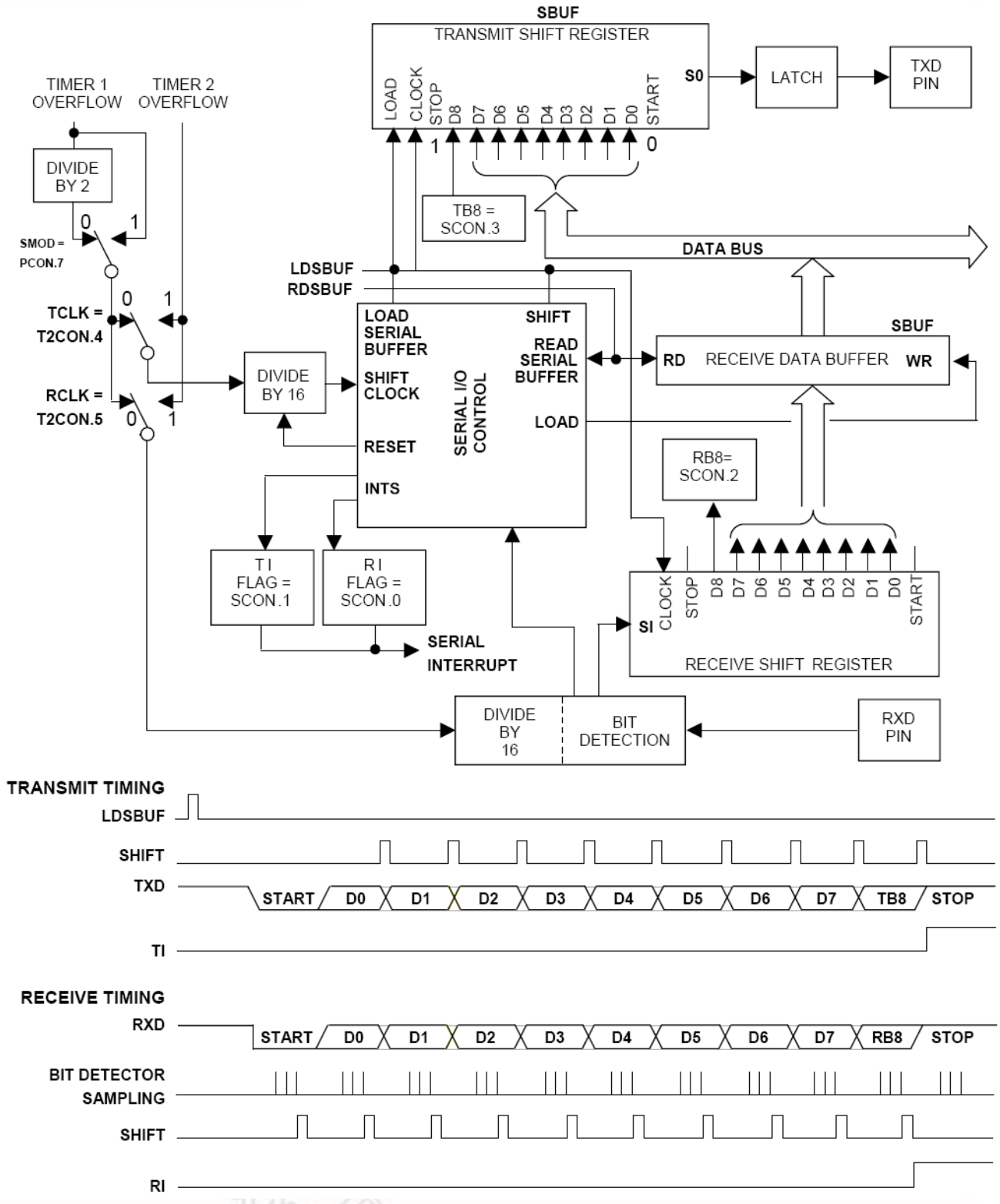

Figure 13–4. Serial Port Mode 3 Function Block and Timing Diagram

Bit	Name	Description
3	DISMODF	**Disable Mode Fault error detection.** This bit is used in combination with the SSOE (SPCR.7) bit to determine the feature of $\overline{SS}$ pin as shown in Table 14–1. Slave Select Pin Configurations. DISMODF affects only in Master mode (MSTR = 1). 0 = Mode Fault detection is not disabled. $\overline{SS}$ serves as input pin for Mode Fault detection disregard of SSOE. 1 = Mode Fault detection is disabled. The feature of $\overline{SS}$ follows SSOE bit.
2:0	-	**Reserved.**

SPDR – Serial Peripheral Data Register

7	6	5	4	3	2	1	0
SPDR[7:0]							
r/w							

Address: F5H reset value: 0000 0000b

Bit	Name	Description
7:0	SPDR[7:0]	**Serial peripheral data.** This byte is used of transmitting or receiving data on SPI bus. A write of this byte is a write to the shift register. A read of this byte is actually a read of the read data buffer. In Master mode, a write to this register initiates transmission and reception of a byte simultaneously.

14.4 Operating Modes

14.4.1 Master mode

The SPI can operate in Master mode while MSTR (SPCR.4) is set as 1. Only one Master SPI device can initiate transmissions. A transmission always begins by Master through writing to SPDR. The byte written to SPDR begins shifting out on MOSI pin under the control of SPCLK. Simultaneously, another byte shifts in from the Slave on the MISO pin. After 8-bit data transfer complete, SPIF (SPSR.7) will automatically set via hardware to indicate one byte data transfer complete. At the same time, the data received from the Slave is also transferred in SPDR. The user can clear SPIF and read data out of SPDR.

14.4.2 Slave Mode

When MSTR is 0, the SPI operates in Slave mode. The SPCLK pin becomes input and it will be clocked by another Master SPI device. The $\overline{SS}$ pin also becomes input. The Master device cannot exchange data with the Slave device until the $\overline{SS}$ pin of the Slave device is externally pulled low. Before data transmissions occurs, the $\overline{SS}$ of the Slave device must be pulled and remain low until the transmission is complete. If $\overline{SS}$ goes

This gives a repetition frequency range of 122Hz to 31.25kHz (F_{PERIPH} = 16MHz). By loading the PWMx registers with either 00H or FFH, the PWM channels will generate a constant low or high level output, respectively.

When a compare register PWMx is loaded with a new value, the associated output updated immediately. It does not have to wait until the end of the current counter period.

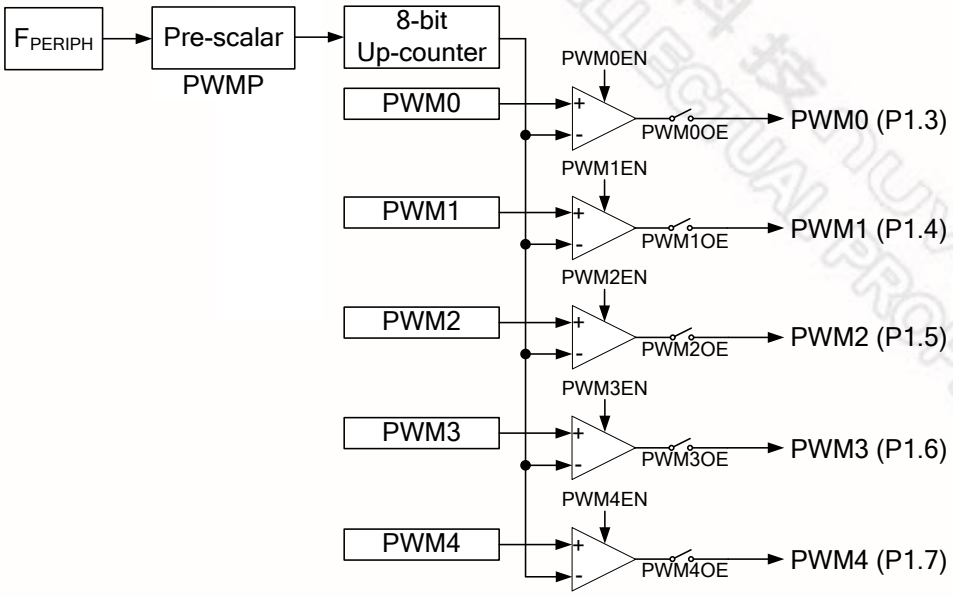

Figure 15–1. PWM Function Block

PWM demo code,

```
MOV     PWMP,#128               ;determine PWM period
MOV     PWM0,#0H                ;duty = 0%
MOV     PWM1,#40H               ;duty = 25%
MOV     PWM2,#80H               ;duty = 50%
MOV     PWM3,#0C0H              ;duty = 75%
MOV     PWM4,#0FFH              ;duty = 100%
ORL     PWMCON0,#00110011b      ;enable PWM0~3
ORL     PWMCON1,#00000001b      ;enable PWM4
ORL     PWMCON0,#11001100b      ;output enable PWM0~3
ORL     PWMCON1,#00000100b      ;output enable PWM4
```

RETI instruction, but it would not inform the Interrupt controller that the interrupt service routine is completed. RET would leave the controller still thinking that the service routine is underway, making future interrupts impossible.

17.2 Interrupt Latency

The response time for each interrupt source depends on several factors, such as the nature of the interrupt and the instruction underway. In the case of external interrupts $\overline{INT0}$ and $\overline{INT1}$, they are sampled at every machine-cycle and then their corresponding interrupt flags IE0 or IE1 will be set or reset. The value are not actually polled by the circuit until the next machine-cycle. If a request is active and all three previous conditions are met, then the hardware generated LCALL is executed. This LCALL itself takes 2 machine-cycles to be completed. Thus there is a minimum time of 3 machine-cycles between the interrupt flag being set and the interrupt service routine being executed.

A longer response time should be anticipated if any of the three conditions are not met. If a higher or equal priority is being serviced, then the interrupt latency time obviously depends on the nature of the service routine currently being executed. If the polling cycle is not the last machine-cycle of the instruction being executed, then an additional delay is introduced. The maximum response time (if no other interrupt is in service) occurs if the device is performing a write to IE, IP and then executes a MUL or DIV instruction. From the time an interrupt source is activated, the longest reaction time is 9 machine-cycles. This includes 1 machine-cycle to detect the interrupt, 2 machine-cycles to complete the IE, EIE, IP, IPH, EIP, or EIPH access, 4 machine-cycles to complete the MUL or DIV instruction and 2 machine-cycles to complete the hardware LCALL to the interrupt vector location.

Thus in a single-interrupt system the interrupt response time will always be more than 3 machine-cycles and not more than 9 machine-cycles.

```
        CJNE   A,B,Program_CONFIG_Verify_Error
        RET
Program_CONFIG_Verify_Error:
        CALL   Disable_ISP
        mov    P0,#00h
        SJMP   $
;*************************************************************
;            APROM code
;*************************************************************
AP_code:
        DB     75h, 90h, 55h              ;OPCODEs of "mov    P1,#55h"
        DB     75h,0A0h,0AAh              ;OPCODEs of "mov    P2,#0aah"
        DB     80h,0FEh                   ;OPCODEs of "sjmp   $"

        END
```

Bit	Name	Description
1	-	**Reserved.**
0	BOS	**Brown-out status.** This bit indicates the V_{DD} voltage level comparing with V_{BOD} while Brown-out circuit is enabled. It is helpful to tell a Brown-out event or power resuming event occurrence. This bit is read-only and keeps 0 if Brown-out detection is not enabled. 0 = V_{DD} voltage level is higher than V_{BOD}. 1 = V_{DD} voltage level is lower than V_{BOD}.

[1] BODEN and BORST will be directly loaded from CONFIG2 bit 7 and bit 4 after all resets.

Table 21–1. BOF Reset Value

Reset source	CBODEN (CONFIG2.7)	CBORST (CONFIG2.4)	V_{DD} stable level	BOF
Brown-out reset	1	1	> V_{BOD} always	1
Other resets	1	1	> V_{BOD} always	1
	1	0	> V_{BOD}	1
	1	0	< V_{BOD}	0
	0	X	X	0

Note that if BOF is 1 after chip reset, it is strongly recommended to initialize the user's program by clearing BOF.

PCON – Power Control

7	6	5	4	3	2	1	0
SMOD	-	-	POF	GF1	GF0	PD	IDL
r/w	-	-	r/w	r/w	r/w	r/w	r/w

Address: 87H reset value: see Table 6–2. N78E366A SFR Descriptions and Reset Values

Bit	Name	Description
4	POF	**Power-on reset flag.** This bit will be set as 1 after a power-on reset. It indicates a cold reset, a power-on reset complete. This bit remains its value after any other resets. This flag is recommended to be cleared via software.

CHPCON – Chip Control (TA protected)

7	6	5	4	3	2	1	0
SWRST	ISPF	LDUEN	XRAMEN	-	-	BS	ISPEN
w	r/w	r/w	r/w	-	-	r/w	r/w

Address: 9FH reset value: see Table 6–2. N78E366A SFR Descriptions and Reset Values

Bit	Name	Description
7	SWRST	**Software reset.** To set this bit as a logic 1 will cause a software reset. It will automatically be cleared via hardware after reset in finished.

The software demo code are listed below.

```
MOV TA,#0AAh              ;TA protection.
MOV TA,#55h               ;
ANL CHPCON,#0FDh          ;BS = 0, reset to APROM.
MOV TA,#0AAh
MOV TA,#55h
ORL CHPCON,#80h           ;Software reset
```

22.6 Boot Select

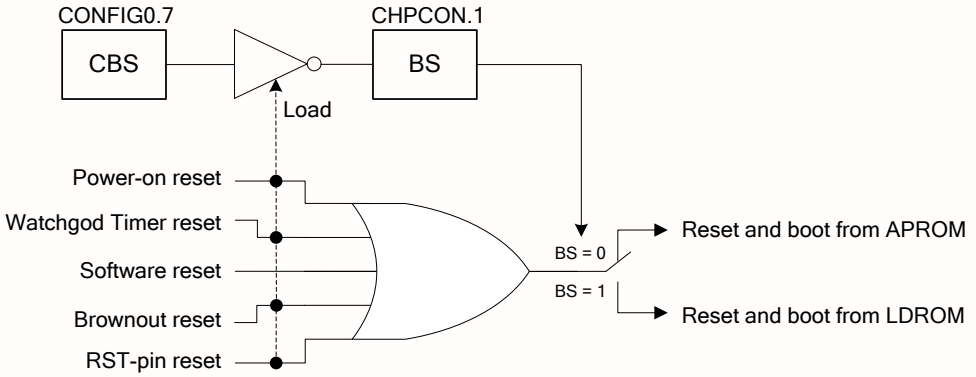

Figure 22–1. Boot Selecting Diagram

N78E366A provides users a flexible boot selection for variant application. The SFR bit BS in CHPCON.1 determines CPU booting from APROM or LDROM after any source of reset. If reset occurs and BS is 0, CPU will reboot from APPROM. Else, the CPU will reboot from LDROM.

23. AUXILIARY FEATURES

ALE is used to enable the address latch that separates the address from the data on Port 0. ALE runs at 1/6 of the Fosc in 12T mode. An ALE pulse is omitted always. The user can turn ALE signal off via setting ALEOFF to reduce EMI. ALEOFF enable will just make ALE activating during external memory access through a MOVC or MOVX instruction. ALE will stay high in other conditions.

AUXR – Auxiliary Register

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	ALEOFF
-	-	-	-	-	-	-	r/w

Address: 8EH reset value: 0000 0000b

Bit	Name	Description
7:1	-	**Reserved.**
0	ALEOFF	**ALE output off.** 0 = ALE is emitted always. 1 = ALE is off normally and active only during external memory access through a MOVX or MOVC instruction.

24. CONFIG BYTES

N78E366A has several hardware configuration bytes, called CONFIG bytes, those are used to configure the hardware options such as the security bits, system clock source, and so on. These hardware options can be re-configured through the Programmer/Writer or ISP modes. N78E366A has three CONFIG bytes those are CONFIG0, 2 and 3. Several functions which are defined by certain CONFIG bits are also available to be re-configured by certain SFR bits. Therefore, there is a need to load such CONFIG bits into respective SFR bits. Such loading will occurs after resets. (Software reset will reload all CONFIG bytes except CBS bit in CONFIG0.) These SFR bits can be continuously controlled via user's software.

Note that CONFIG bits marked as "-" should always keep unprogrammed.

CONFIG0

7	6	5	4	3	2	1	0
CBS	-	-	-	-	MOVCL	LOCK	-
r/w	-	-	-	-	r/w	r/w	-

unprogrammed value: 1111 1111b

Bit	Name	Description
7	CBS	**CONFIG boot select.** This bit defines from which block MCU boots after all resets except software reset. 1 = MCU will boot from APROM after all resets except software reset. 0 = MCU will boot from LDROM after all resets except software reset.
6:3	-	**Reserved.**
2	MOVCL	**MOVC lock enable.** This bit determines MOVC instruction is inhibited or not when reading internal Program Memory by executing on the external Program Memory. This mechanism is for data security. 1 = MOVC has no restriction. 0 = MOVC is restricted. The external Program Memory code is inhibited to read internal APROM or LDROM contents through MOVC instruction.
1	LOCK	**Chip lock enable.** 1 = Chip is unlocked. All of APROM and LDROM are not locked. Their contents can be read out through a parallel Programmer/Writer. 0 = Chip is locked. APROM and LDROM are locked. Their contents read through parallel Programmer/Writer will become FFH. Note that CONFIG bytes are always unlocked and can be read. Hence, once the chip is locked, the CONFIG bytes cannot be erased or programmed individually. The only way to disable chip lock is to use the whole chip erase mode. However, all data within APROM, LDROM, and other CONFIG bits will be erased when this procedure is executed. If the chip is locked, it does not alter the ISP function.
0	-	**Reserved.**

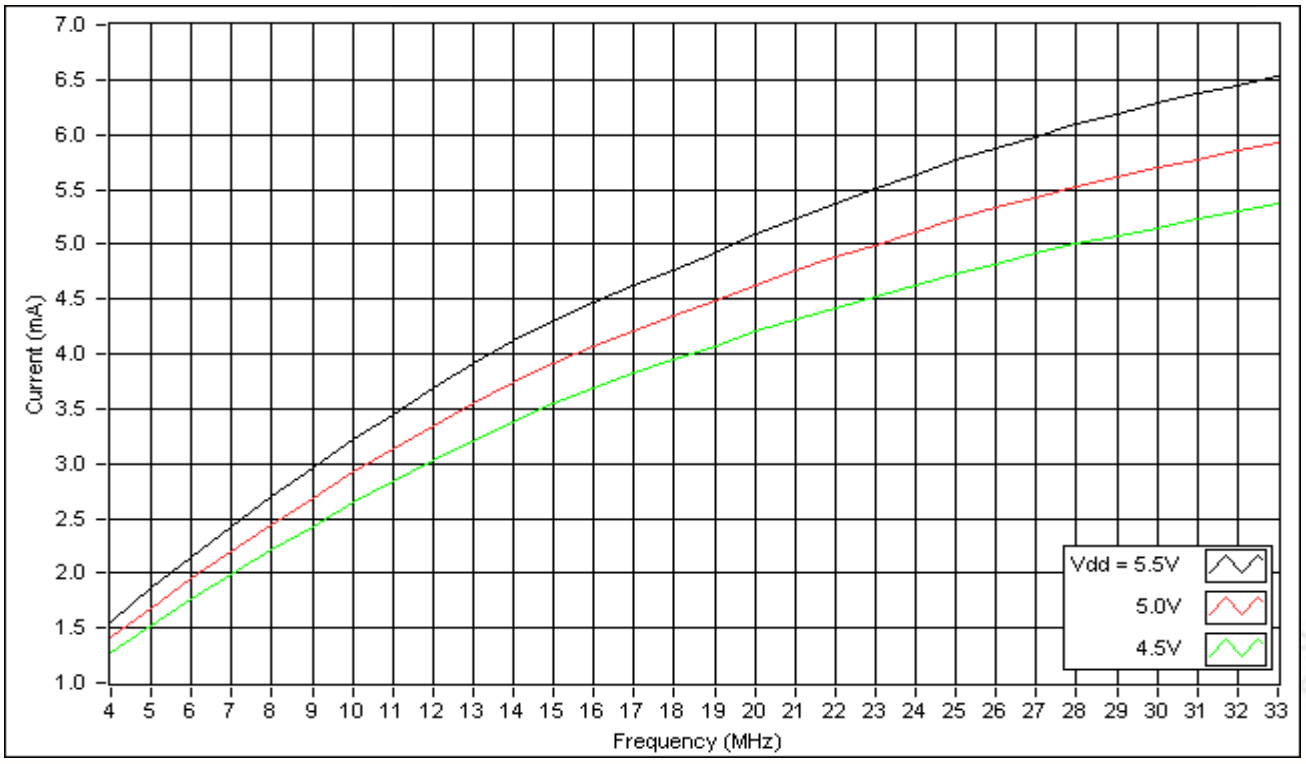

Figure 26–7. Idle Mode Current Under 6T Mode, External Clock (1)

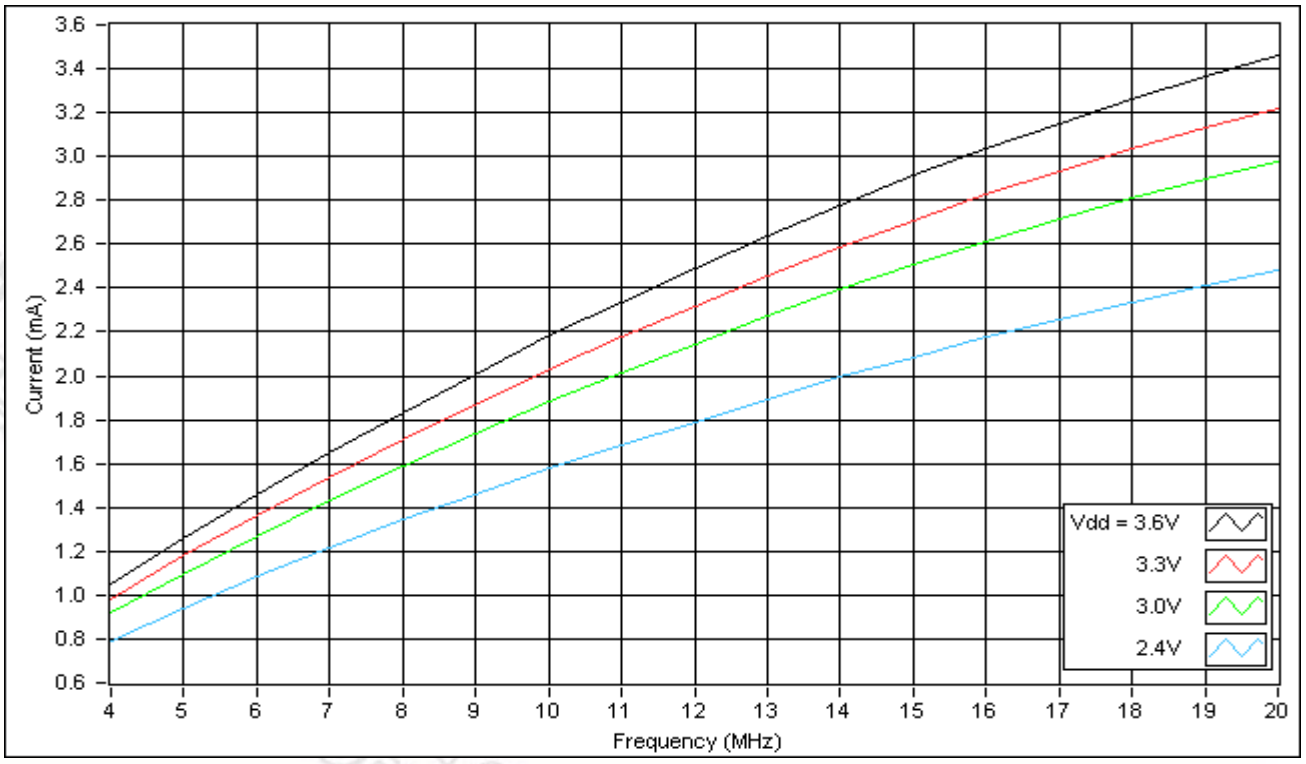

Figure 26–8. Idle Mode Current Under 6T Mode, External Clock (2)

26.3 AC Electrical Characteristics

Table 26–2. AC Characteristics

Symbol	Parameter	12T mode		6T mode		Unit
		Min.	Max.	Min.	Max.	
External Clock						
1/ t_{CLCL}	External clock input frequency	0	40	0	33	MHz
	Crystal/resonator frequency	4	40	4	33	
t_{CHCX}	High time	12		15		ns
t_{CLCX}	Low time	12		15		ns
t_{CLCH}	Rise time		8		5	ns
t_{CHCL}	Fall time		8		5	ns
Program Memory						
t_{LHLL}	ALE pulse width	2 t_{CLCL} -15		t_{CLCL} -15		ns
t_{AVLL}	Address valid to ALE low	t_{CLCL} -15		0.5 t_{CLCL} -15		ns
t_{LLAX}	Address hold after ALE low	t_{CLCL} -15		0.5 t_{CLCL} -15		ns
t_{LLIV}	ALE low to valid instruction in		4 t_{CLCL} -45		2 t_{CLCL} -45	ns
t_{LLPL}	ALE low to $\overline{PSEN}$ low	t_{CLCL} -15		0.5 t_{CLCL} -15		ns
t_{PLPH}	$\overline{PSEN}$ pulse width	3 t_{CLCL} -15		1.5 t_{CLCL} -15		ns
t_{PLIV}	$\overline{PSEN}$ low to valid instruction in		3 t_{CLCL} -50		1.5 t_{CLCL} -50	ns
t_{PXIX}	Input instruction hold after $\overline{PSEN}$	0		0		ns
t_{PXIZ}	Input instruction float after $\overline{PSEN}$		t_{CLCL} -15		0.5 t_{CLCL} -15	ns
t_{AVIV}	Address to valid instruction in		5 t_{CLCL} -60		2.5 t_{CLCL} -60	ns
t_{PLAZ}	$\overline{PSEN}$ low to address float		10		10	ns
Data Memory						
t_{RLRH}	$\overline{RD}$ pulse width	6 t_{CLCL} -30		3 t_{CLCL} -30		ns
t_{WLWH}	$\overline{WR}$ pulse width	6 t_{CLCL} -30		3 t_{CLCL} -30		ns
t_{RLDV}	$\overline{RD}$ low to valid data in		5 t_{CLCL} -50		2.5 t_{CLCL} -50	ns
t_{RHDX}	Data hold after $\overline{RD}$	0		0		ns
t_{RHDZ}	Data float after $\overline{RD}$		2 t_{CLCL} -12		t_{CLCL} -12	ns
t_{LLDV}	ALE low to valid data in		8 t_{CLCL} -50		4 t_{CLCL} -50	ns
t_{AVDV}	Address to valid data in		9 t_{CLCL} -75		4.5 t_{CLCL} -75	ns
t_{LLWL}	ALE low to $\overline{RD}$ or $\overline{WR}$ low	3 t_{CLCL} -15	3 t_{CLCL} +15	1.5 t_{CLCL} -15	1.5 t_{CLCL} +15	ns

Symbol	Parameter	12T mode		6T mode		Unit
		Min.	Max.	Min.	Max.	
t_{AVWL}	Address valid to $\overline{WR}$ low or $\overline{RD}$ low	4 t_{CLCL} -30		2 t_{CLCL} -30		ns
t_{QVWX}	Data valid to $\overline{WR}$ transition	t_{CLCL} -20		0.5 t_{CLCL} -20		ns
t_{WHQX}	Data hold after $\overline{WR}$	t_{CLCL} -15		0.5 t_{CLCL} -15		ns
t_{RLAZ}	$\overline{RD}$ low to address float		0		0	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ high to ALE high	t_{CLCL} -15	t_{CLCL} +15	0.5 t_{CLCL} -15	0.5 t_{CLCL} +15	ns

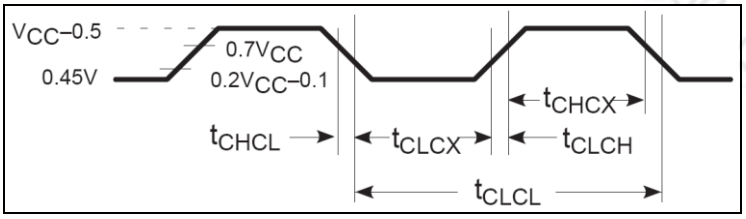

Figure 26–9. External Clock Input Timing

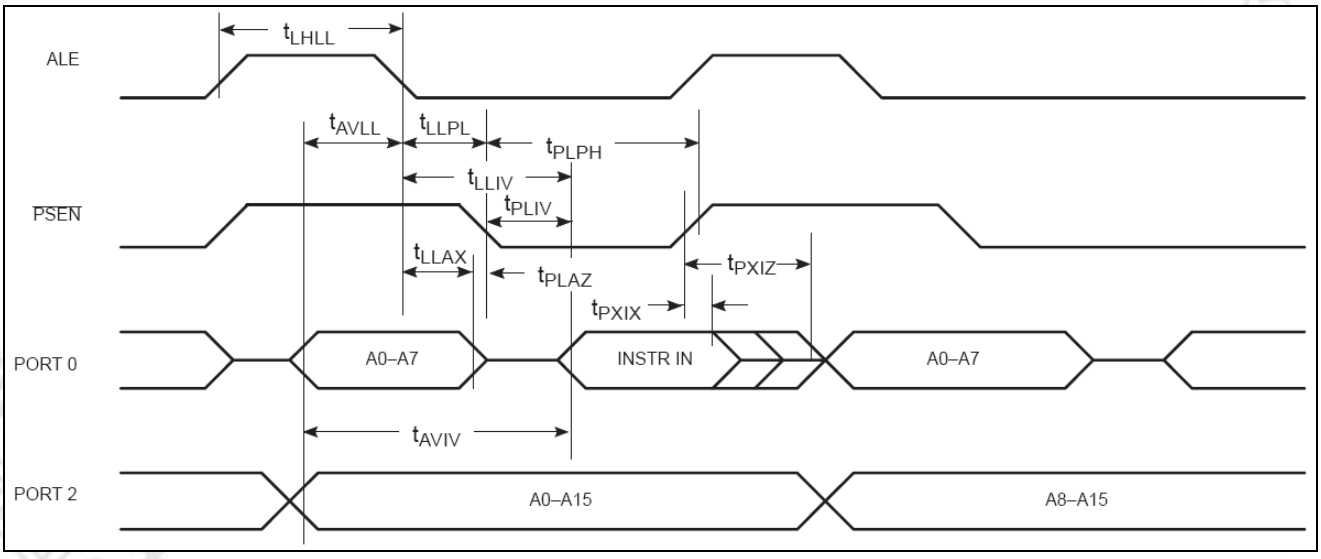

Figure 26–10. External Program Memory Read Cycle

Table 26–3. Characteristics of On-chip RC Oscillators

Symbol	Parameter	Condition	Frequency Deviation	Min.	Typ.	Max.	Unit
F_{IHRC}	System 22.1184MHz RC oscillator frequency[1][2]	25℃	1%	21.8972	22.1184	22.3396	MHz
		-40℃~85℃	3%	21.4548	22.1184	22.7820	MHz
F_{ILRC}	WDT and PDT 10kHz RC oscillator frequency		30%	7	10	13	kHz

[1] Internal 11.0592MHz is not listed for the same frequency deviation due to directly divided by 2 from 22.1184MHz source.

[2] A 0.1μF capacitor is recommended to be added on XTAL1 pin to gain the more precise frequency of the internal RC oscillator frequency if it is selected as the system clock source.

Table 26–4. Characteristics of Brown-out Detection

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
T_{BOD}	Brown-out detect pulse width	$V_{DD} < V_{BOD}$	600	-	-	μs
T_{BODRD}	Brown-out release delay period	$V_{DD} > V_{BOD}$	5.6	8	10.4	ms

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