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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Last Time Buy
Core Processor	8051
Core Size	8-Bit
Speed	40MHz
Connectivity	EBI/EMI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.25K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-BQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/n78e366afg

CONTENTS

2. FEATURES

- Fully static design 8-bit CMOS microcontroller.
- Wide supply voltage of 2.4V to 5.5V and wide frequency from 4MHz to 40MHz.
- 12T mode compatible with the tradition 8051 timing.
- 6T mode supported for double performance.
- On-chip RC oscillator of 22.1184MHz/11.0592MHz, trimmed to ±1% at room temperature for the precise system clock.
- 64k bytes Flash APROM for the application program.
- 2.5k bytes Flash LDROM for ISP code.
- In-System-Programmable (ISP) built in. ISP Erasing or programming supports wide operating voltage 3.0V~5.5V.
- Flash 10,000 writing cycle endurance. Greater than 10 years data retention under 85℃.
- 256 bytes of on-chip RAM.
- 1k bytes of on-chip auxiliary RAM (XRAM).
- 64k bytes Program Memory address space and 64k bytes Data Memory address space.
- Maximum five 8-bit general purpose I/O ports pin-to-pin compatible with standard 8051, additional $\overline{\text{INT2}}$ and $\overline{\text{INT3}}$ on packages except DIP-40.
- Three 16-bit Timers/Counters.
- One dedicate timer for Power Down mode waking-up.
- One full-duplex UART port.
- Five pulse width modulated (PWM) output channels.
- One SPI communication port.
- 11-source, 4-priority-level interrupts capability.
- Programmable Watchdog Timer.
- Power-on reset.
- Brown-out detection interrupt and reset, 4-level selected.
- Supports software reset function.
- Built-in power management with Idle mode and Power Down mode.
- Code lock for data security.

Table 4–1. Pin Description

Pin number				Symbol	Alternate Function		Type[1]	Description
DIP	PLCC	PQFP	LQFP		1	2		
10	11	5	5	P3.0	RXD		I/O	**PORT3:** Port 3 is an 8-bit quasi bi-directional I/O port. Its multifunction pins are for RXD, TXD, $\overline{INT0}$, $\overline{INT1}$, T0, T1, $\overline{WR}$, and $\overline{RD}$.
11	13	7	7	P3.1	TXD		I/O	
12	14	8	8	P3.2	$\overline{INT0}$		I/O	
13	15	9	9	P3.3	$\overline{INT1}$		I/O	
14	16	10	10	P3.4	T0		I/O	
15	17	11	11	P3.5	T1		I/O	
16	18	12	13	P3.6	$\overline{WR}$		I/O	
17	19	13	14	P3.7	$\overline{RD}$		I/O	
-	23	17	18	P4.0			I/O	**PORT4**[3]**:** Port 4 is an 8-bit quasi bi-directional I/O port. It also possesses bit-addressable feature as P0~P3. P4.2 and P4.3 are alternative function pins of $\overline{INT3}$ and $\overline{INT2}$.
-	34	28	30	P4.1			I/O	
-	1	39	42	P4.2	$\overline{INT3}$		I/O	
-	12	6	6	P4.3	$\overline{INT2}$		I/O	
-	-	-	48	P4.4			I/O	
-	-	-	12	P4.5			I/O	
-	-	-	24	P4.6			I/O	
-	-	-	36	P4.7			I/O	

[1] I/O type description. I: input, O: output, I/O: quasi bi-direction, D: open-drain, P: power pins, ST: Schmitt trigger.
[2] While switching to 6T mode, ALE will run at 1/3 of Fosc.
[3] A full 8-bit P4 is just on LQPF-48 package. PLCC-44 and PQFP-44 just have low nibble 4 bits of P4. DIP-40 does not have this additional P4.

PCON – Power Control

7	6	5	4	3	2	1	0
SMOD	-	-	POF	GF1	GF0	PD	IDL
r/w	-	-	r/w	r/w	r/w	r/w	r/w

Address: 87H reset value: see Table 6–2. N78E366A SFR Descriptions and Reset Values

Bit	Name	Description
3	GF1	**General purpose flag 1.** The general purpose flag that can be set or cleared by the user.
2	GF0	**General purpose flag 0.** The general purpose flag that can be set or cleared by the user.

P0 and P2 also serve as address/data bus when external memory is running or is accessed by MOVC or MOVX instruction. In these cases, it has strong pull-up and pull-down. In this application, there is no need of any external pull-up resistor. While external mode execution, P0 and P2 cannot be used as general purpose I/O anymore.

In standard 8051 instruction set, one kind of instructions, read-modify-write instructions, should be specially taken care of. Instead of the normal instructions, the read-modify-write instructions read the internal port latch (Px in SFRs) rather than the external port pin state. This kind of instructions read the port SFR value, modify it and write back to the port SFR. Read-modify-write instructions are listed as follows.

Instruction		Description
ANL		Logical AND. (ANL Px,A and ANL Px,direct)
ORL		Logical OR. (ORL Px,A and ORL Px,direct)
XRL		Logical exclusive OR. (XRL Px,A and XRL Px,direct)
JBC		Jump if bit = 1 and clear it. (JBC Px.y,LABEL)
CPL		Complement bit. (CPL Px.y)
INC		Increment. (INC Px)
DEC		Decrement. (DEC Px)
DJNZ		Decrement and jump if not zero. (DJNZ Px,LABEL)
MOV	Px.y,C	Move carry bit to Px.y.
CLR	Px.y	Clear bit Px.y.
SETB	Px.y	Set bit Px.y.

The last three seems not obviously read-modify-write instructions but actually they are. They read the entire port latch value, modify the changed bit, then write the new value back to the port latch.

P0 – Port 0 (bit-addressable)

7	6	5	4	3	2	1	0
P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Address: 80H reset value: 1111 1111b

Bit	Name	Description
7:0	P0[7:0]	**Port 0.** Port 0 is an 8-bit open-drain port by default. Via setting P0UP (P0OR.0) P0 will switch as weakly pulled up internally. P0 has an alternative function as AD[7:0] while external memory accessing. During external Program Memory execution, SFR P0 cannot be accessed.

of Idle mode still keeps at a “mA” level. To further reducing the current consumption to “μA” level, the CPU should stay in Power Down mode when nothing needs to be served, and has the ability of waking up at a programmable interval. N78E366A is equipped with this useful function. It provides a very low power internal RC 10kHz. Along with the low power consumption application, the Power Down Waking-up timer needs to count under Idle and Power Down mode and wake CPU up from Idle or Power Down mode. The demo code to accomplish this feature is shown below.

The demo code of Power Down waking-up timer waking up CPU from Power Down.

```
       ORG    0000H
       LJMP   START

       ORG    004BH
       LJMP   PDT_ISR

       ORG    0100H
PDT_ISR:
       ORL    PDCON,#01000000B          ;Clear Power Down Waking-up timer counter
       ANL    PDCON,#11011111B          ;Clear Power Down Waking-up timer interrupt flag
       RETI

START:
       ORL    PDCON,#00000111B          ;Choose interval length
       ORL    EIE,#00000010B            ;Enable Power Down Waking-up timer interrupt
       SETB   EA
       ORL    PDCON,#10000000B          ;Enable Power Down Waking-up timer to run

;*********************************************************************
;Enter into Power Down mode
;*********************************************************************
LOOP:
       ORL    PCON,#02H
       LJMP   LOOP
```

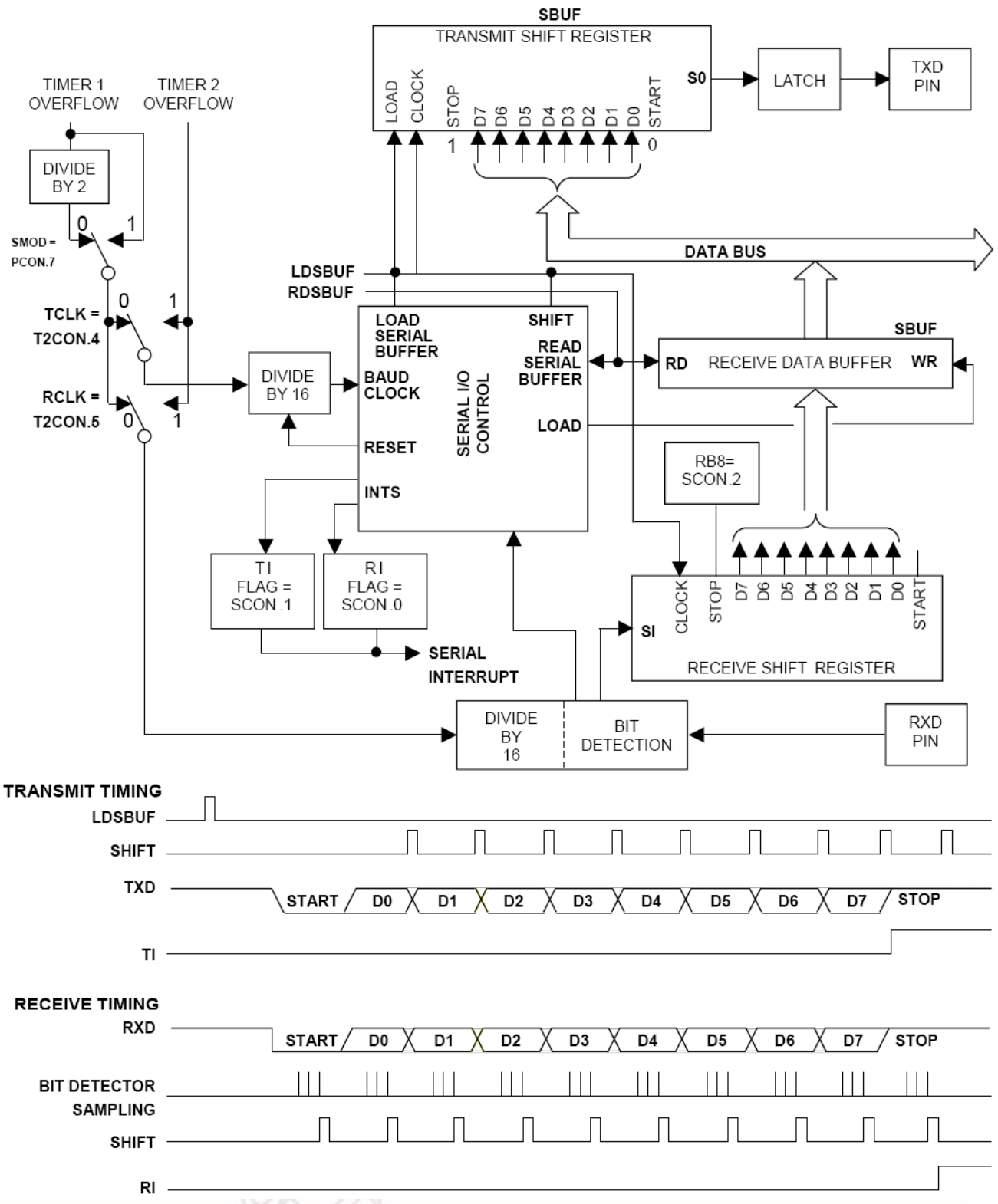


Figure 13–2. Serial Port Mode 1 Function Block and Timing Diagram

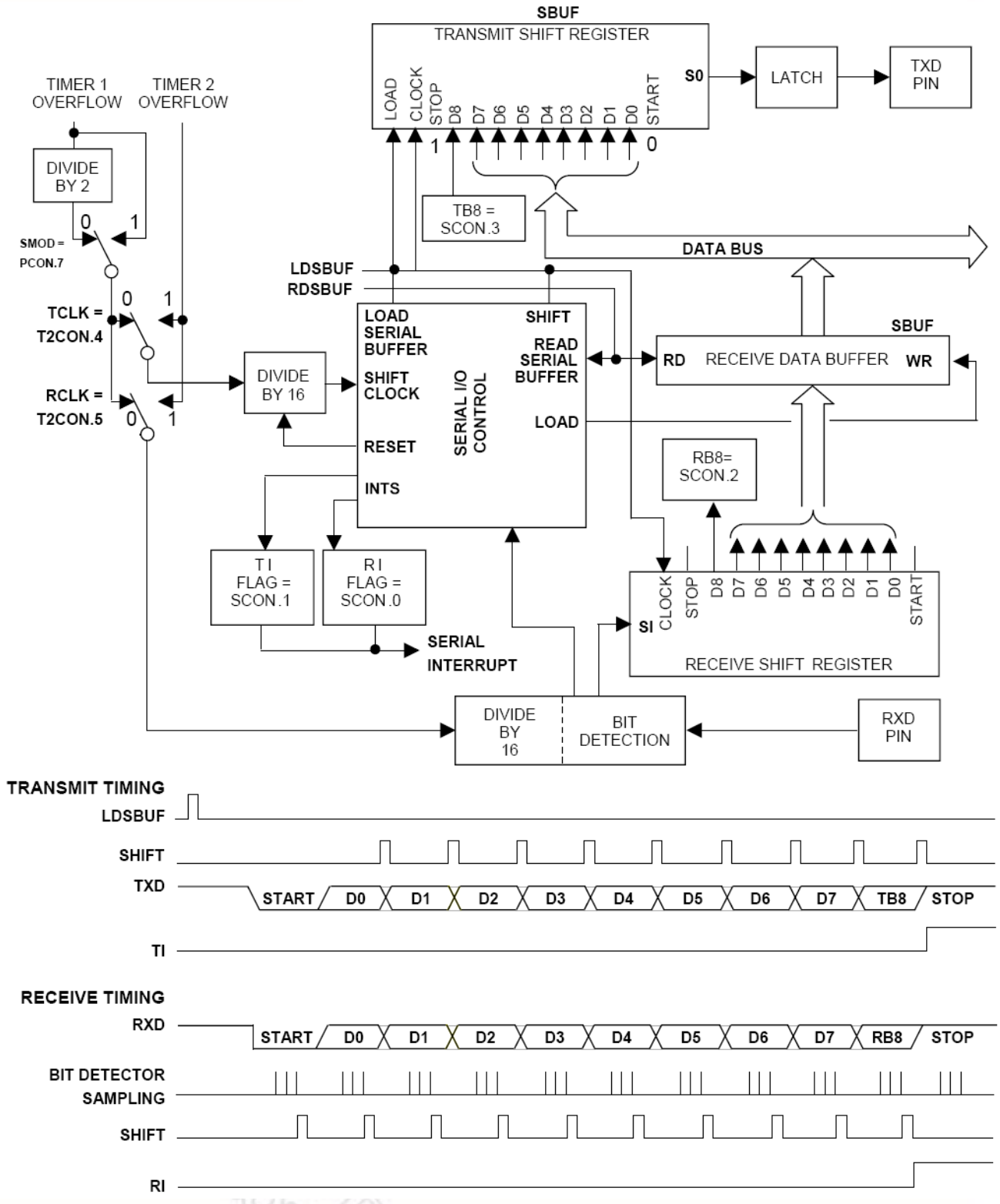


Figure 13–4. Serial Port Mode 3 Function Block and Timing Diagram

In an address byte, the 9th bit is 1 and in a data byte, it is 0. The address byte interrupts all slaves so that each slave can examine the received byte and see if it is being addressed. The addressed slave then clears its SM2 bit and prepares to receive incoming data bytes. The SM2 bits of slaves that were not addressed remain set, and they continue operating normally while ignoring the incoming data bytes.

Follow these steps to configure multiprocessor communications:

1. Set all devices (Masters and Slaves) to UART mode 2 or 3.

2. Write the SM2 bit of all the Slave devices to 1.

3. The Master device's transmission protocol is:

   – First byte: the address, identifying the target slave device, (9th bit = 1).

   – Next bytes: data, (9th bit = 0).

4. When the target Slave receives the first byte, all of the Slaves are interrupted because the 9th data bit is 1. The targeted Slave compares the address byte to its own address and then clears its SM2 bit in order to receive incoming data. The other slaves continue operating normally.

5. After all data bytes have been received, set SM2 back to 1 to wait for next address.

SM2 has no effect in Mode 0, and in Mode 1 can be used to check the validity of the stop bit. For mode 1 reception, if SM2 is 1, the receive interrupt will not be issue unless a valid stop bit is received.

14. SERIAL PERIPHERAL INTERFACE (SPI)

14.1 Features

N78E366A exists a Serial Peripheral Interface (SPI) block to support high speed serial communication. SPI is a full-duplex, high speed, synchronous communication bus between MCUs or other peripheral devices such as serial EEPROM, LCD driver, or D/A converter. It provides either Master or Slave mode, high speed rate up to $F_{PERIPH}/16$ for Master mode and $F_{PERIPH}/4$ for Slave mode, transfer complete and write collision flag. For a multi-master system, SPI supports Master Mode Fault to protect a multi-master conflict.

14.2 Function Description

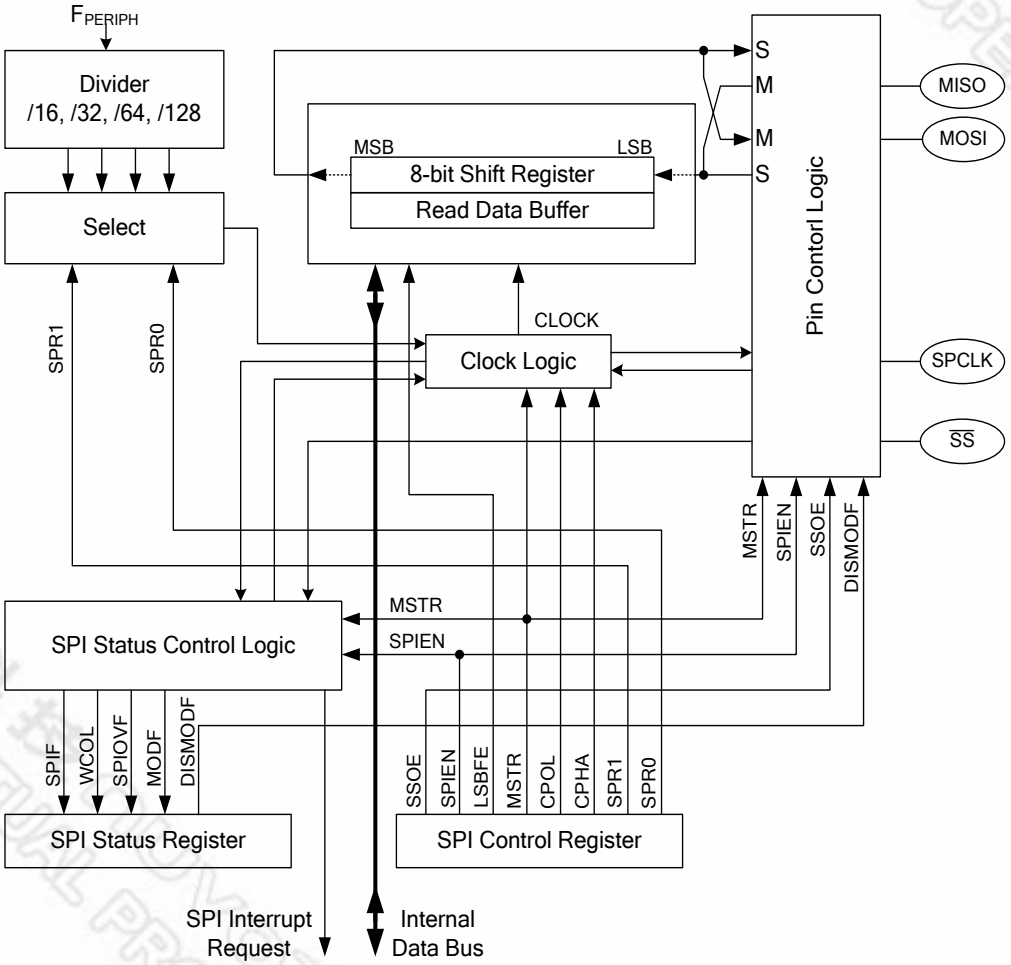


Figure 14–1. SPI Block Diagram

Concerning the Slave mode, the $\overline{SS}$ signal needs to be taken care. As shown in Figure 14–4. SPI Clock Formats, when CPHA = 0, the first SPCLK edge is the sampling strobe of MSB (for an example of LSBFE = 0, MSB first). Therefore, the Slave must shift its MSB data before the first SPCLK edge. The falling edge of $\overline{SS}$ is used for preparing the MSB on MISO line. The $\overline{SS}$ pin therefore must toggle high and then low between each successive serial byte. Furthermore, if the slave writes data to the SPI data register (SPDR) while $\overline{SS}$ is low, a write collision error occurs.

When CPHA = 1, the sampling edge thus locates on the second edge of SPCLK clock. The Slave uses the first SPCLK clock to shift MSB out rather than the $\overline{SS}$ falling edge. Therefore, the $\overline{SS}$ line can remain low between successive transfers. This format may be preferred in systems having single fixed Master and single fixed Slave. The $\overline{SS}$ line of the unique Slave device can be tied to V_{SS} as long as only CPHA = 1 clock mode is used.

Note: The SPI should be configured before it is enabled (SPIEN = 1), or a change of LSBFE, MSTR, CPOL, CPHA and SPR[1:0] will abort a transmission in progress and force the SPI system into idle state. Prior to any configuration bit changed, SPIEN must be disabled first.

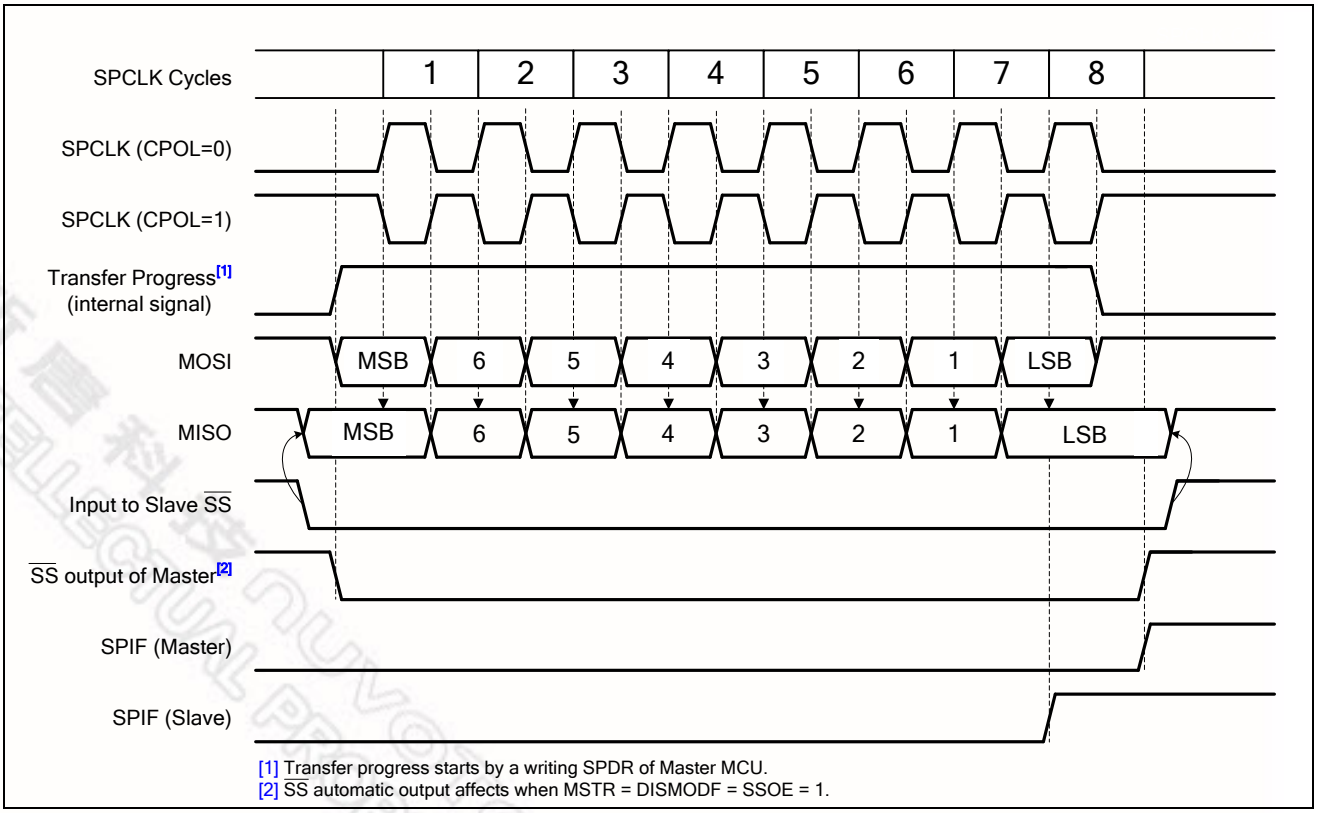


Figure 14–5. SPI Clock and Data Format with CPHA = 0

Bit	Name	Description
0	PWM0EN	**PWM0 enable.** 0 = PWM0 is disabled and stops. 1 = PWM0 is enabled and runs.

PWMCON1 – PWM Control 1

7	6	5	4	3	2	1	0
-	-	-	-	-	PWM4OE	-	PWM4EN
-	-	-	-	-	r/w	-	r/w

Address: CEH reset value: 0000 0000b

Bit	Name	Description
7:3	-	**Reserved.**
2	PWM4OE	**PWM4 output enable.** 0 = P1.7 serves as general purpose I/O. 1 = P1.7 serves as output pin of PWM4 signal.
1	-	**Reserved.**
0	PWM4EN	**PWM0 enable.** 0 = PWM4 is disabled and stops. 1 = PWM4 is enabled and runs.

PWMP – PWM Period

7	6	5	4	3	2	1	0
PWMP[7:0]							
r/w							

Address: D9H reset value: 0000 0000b

Bit	Name	Description
7:0	PWMP[7:0]	**PWM period.** This byte controls the period of the PWM output of PWM0~PWM4 channels.

PWM0 – PWM0 Duty

7	6	5	4	3	2	1	0
PWM0[7:0]							
r/w							

Address: DAH reset value: 0000 0000b

Bit	Name	Description
7:0	PWM0[7:0]	**PWM0 duty.** This byte controls the duty of the PWM0 output.

PWM1 – PWM1 Duty

7	6	5	4	3	2	1	0
PWM1[7:0]							
r/w							

Address: DBH reset value: 0000 0000b

Bit	Name	Description
7:0	PWM1[7:0]	**PWM1 duty.** This byte controls the duty of the PWM1 output.

PWM2 – PWM2 Duty

7	6	5	4	3	2	1	0
PWM2[7:0]							
r/w							

Address: DDH reset value: 0000 0000b

Bit	Name	Description
7:0	PWM2[7:0]	**PWM2 duty.** This byte controls the duty of the PWM2 output.

PWM3 – PWM3 Duty

7	6	5	4	3	2	1	0
PWM3[7:0]							
r/w							

Address: DEH reset value: 0000 0000b

Bit	Name	Description
7:0	PWM3[7:0]	**PWM3 duty.** This byte controls the duty of the PWM3 output.

PWM4 – PWM4 Duty

7	6	5	4	3	2	1	0
PWM4[7:0]							
r/w							

Address: CFH reset value: 0000 0000b

Bit	Name	Description
7:0	PWM4[7:0]	**PWM4 duty.** This byte controls the duty of the PWM4 output.

The repetition frequency of PWM, F_{PWM} is given by,

$F_{PWM} = \frac{F_{PERIPH}}{(PWMP + 1) \times 255}$, pre-scalar division factor = PWM + 1.

PWM high duty of PWMx = $\frac{PWMx}{255}$.

16. TIMED ACCESS PROTECTION (TA)

N78E366A has several features like the Watchdog Timer, the ISP function, Boot select control, etc. are crucial to proper operation of the system. If leaving these control registers unprotected, errant code may write undetermined value into them, it results in incorrect operation and loss of control. In order to prevent this risk, the N78E366A has a protection scheme which limits the write access to critical SFRs. This protection scheme is done using a timed access. The following registers are related to TA process.

TA – Timed Access

7	6	5	4	3	2	1	0
TA[7:0]							
w							

Address: C7H reset value: 0000 0000b

Bit	Name	Description
7:0	TA[7:0]	**Timed access.** The timed access register controls the access to protected SFRs. To access protected bits, the user must first write AAH to the TA and immediately followed by a write of 55H to TA. After these two steps, a writing permission window is opened for three machine-cycles during which the user may write to protected SFRs.

In timed access method, the bits, which are protected, have a timed write enable window. A write is successful only if this window is active, otherwise the write will be discarded. When the software writes AAH to TA, a counter is started. This counter waits for three machine-cycles looking for a write of 55H to TA. If the second write of 55H occurs within three machine-cycles of the first write of AAH, then the timed access window is opened. It remains open for three machine-cycles during which the user may write to the protected bits. After three machine-cycles, this window automatically closes. Once the window closes, the procedure must be repeated to access the other protected bits. Not that the TA protected SFRs are required timed access for writing. But the reading is not protected. The user may read TA protected SFR without giving AAH and 55H to TA. The suggestion code for opening the timed access window is shown below.

```
(CLR    EA)                 ;if any interrupt is enabled, disable temporally
 MOV    TA,#0AAH
 MOV    TA,#55H
(Instruction that writes a TA protected register)
(SETB   EA)                 ;resume interrupts enabled
```

The writings of AAH, 55H to TA register and the writing-protection register must occur within 3 machine-cycles of each other. Any enabled interrupt should be disabled during this procedure to avoid delay between these three writings. If there is no interrupt enabled, the `CLR EA` and `SETB EA` instructions can be left out. Once the timed access window closes, the procedure must be repeated to access the other protected bits.

18. IN SYSTEM PROGRAMMING (ISP)

The internal Program Memory supports both hardware programming and in system programming (ISP). Hardware programming mode uses gang-writers to reduce programming costs and time to market while the products enter into the mass production state. However, if the product is just under development or the end product needs firmware updating in the hand of an end user, the hardware programming mode will make repeated programming difficult and inconvenient. ISP method makes it easy and possible. N78E366A supports ISP mode allowing a device to be reprogrammed under software control. Furthermore, the capability to update the application firmware makes wide range of applications possible.

ISP is performed without removing the microcontroller from the system. The most common method to perform ISP is via UART along with the firmware in LDROM. General speaking, PC transfers the new APROM code through serial port. Then LDROM firmware receives it and re-programs into APROM through ISP commands. Nuvoton provides ISP firmware, USB ISP writer and PC application program for N78E366A. It makes users quite easy perform ISP through Nuvoton standard ISP tool. Please explore Nuvoton 8-bit Microcontroller website: Nuvoton 80C51 Microcontroller Development Tool.

18.1 ISP Procedure

Unlike RAM's real-time operation, to update flash data often takes long time. Furthermore, it is a quite complex timing procedure to erase, program, or read flash data. Fortunately, N78E366A carried out the flash operation with convenient mechanism to help the user update the flash content. After ISP enabled by setting ISPEN (CHPCON.0 with TA protected), the user can easily fill the 16-bit target address in ISPAH and ISPAL, data in ISPFD and command in ISPCN. Then the ISP is ready to begin by setting a triggering bit ISPGO (ISPTRG.0). Note that ISPTRG is also TA protected. At this moment, the CPU holds the Program Counter and the built-in ISP automation takes over to control the internal charge-pump for high voltage and the detail signal timing. After ISP action completed, the Program Counter continues to run the following instructions. The ISPGO bit will be automatically cleared. The user may repeat steps above for next ISP action if necessary. Through this progress, the user can easily erase, program, and verify the embedded flash by just taking care of the pure software.

The following registers relate to ISP processing.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_{IL}	Logical 0 input current (Ports 1 ~ 4 and Port 0 with internal pull-up enabled)	V_{DD} = 5.5V, V_{IN} = 0.4V V_{DD} = 3.6V, V_{IN} = 0.4V			-50 -20	µA
I_{TL}	Logical 1-to-0 transition current[2] (Ports 1~4 and Port 0 with internal pull-up enabled)	V_{DD} = 5.5V V_{DD} = 3.6V		-570 -240	-650 -290	µA
I_{LI}	Input leakage current (Port 0)	0 < V_{IN} < V_{DD}			±10	µA
I_{DD}	Supply current[3]	V_{DD} = 5.0V, external clock, 12T			0.21F + 3.5	mA
		V_{DD} = 3.3V, external clock, 12T			0.15F + 2.9	mA
		V_{DD} = 5.0V, external clock, 6T			0.35F + 3.3	mA
		V_{DD} = 3.3V, external clock, 6T			0.32F + 2.3	mA
		V_{DD} = 5.0V, internal 22.1184MHz, 12T			5.8	mA
		V_{DD} = 3.3V, internal 11.0592MHz, 12T			3.9	mA
		V_{DD} = 5.0V, internal 22.1184MHz, 6T			8.6	mA
		V_{DD} = 3.3V, internal 11.0592MHz, 6T			5.1	mA
I_{ID}	Idle mode current	V_{DD} = 5.0V, external clock, 12T			0.11F + 2.0	mA
		V_{DD} = 3.3V, external clock, 12T			0.09F + 0.9	mA
		V_{DD} = 5.0V, external clock, 6T			0.15F + 1.7	mA
		V_{DD} = 3.3V, external clock, 6T			0.14F + 0.7	mA
		V_{DD} = 5.0V, internal 22.1184MHz, 12T			2.0	mA
		V_{DD} = 3.3V, internal 11.0592MHz, 12T			1.4	mA
		V_{DD} = 5.0V, internal 22.1184MHz, 6T			2.5	mA
		V_{DD} = 3.3V, internal 11.0592MHz, 6T			1.8	mA
I_{PD}	Power Down mode current			2	35	µA
R_{RST}	RST pin internal pull-down resistor	2.4 < V_{DD} < 5.5V	45		800	kΩ
V_{BOD0}	Brown-out threshold 2.2V		2.05	2.2	2.3	V
V_{BOD1}	Brown-out threshold 2.7V		2.6	2.7	2.85	V
V_{BOD2}	Brown-out threshold 3.8V		3.65	3.8	4.0	V
V_{BOD3}	Brown-out threshold 4.5V		4.35	4.5	4.75	V
V_{BODHYS}	Brown-out hysteresis		20		200	mV
V_{POR}	Power-on reset threshold			2.0		V

[1] Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows,
Maximum I_{OL} per port pin: 20mA
Maximum I_{OL} per 8-bit port: 40mA
Maximum total I_{OL} for all outputs: 100mA

[2] Pins of ports 1~4 and port 0 with internal pull-up enabled will source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 1.5V ~ 2.5V.

[3] It is measured while MCU keeps in running SJMP $ loop continuously. P0 is externally or internally pulled-up.

Figures below shows supply and Idle mode current under 12T/6T with internal program memory mode.

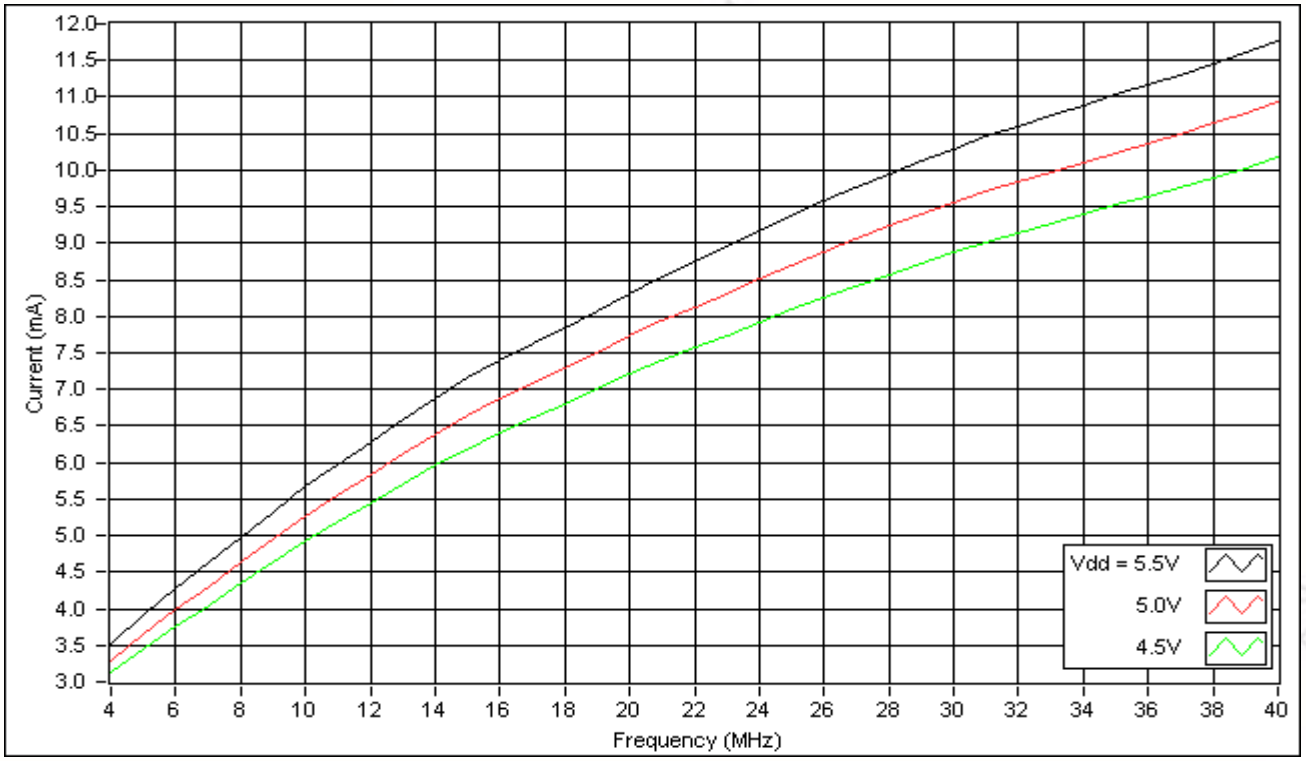


Figure 26–1. Supply Current Under 12T Mode, External Clock (1)

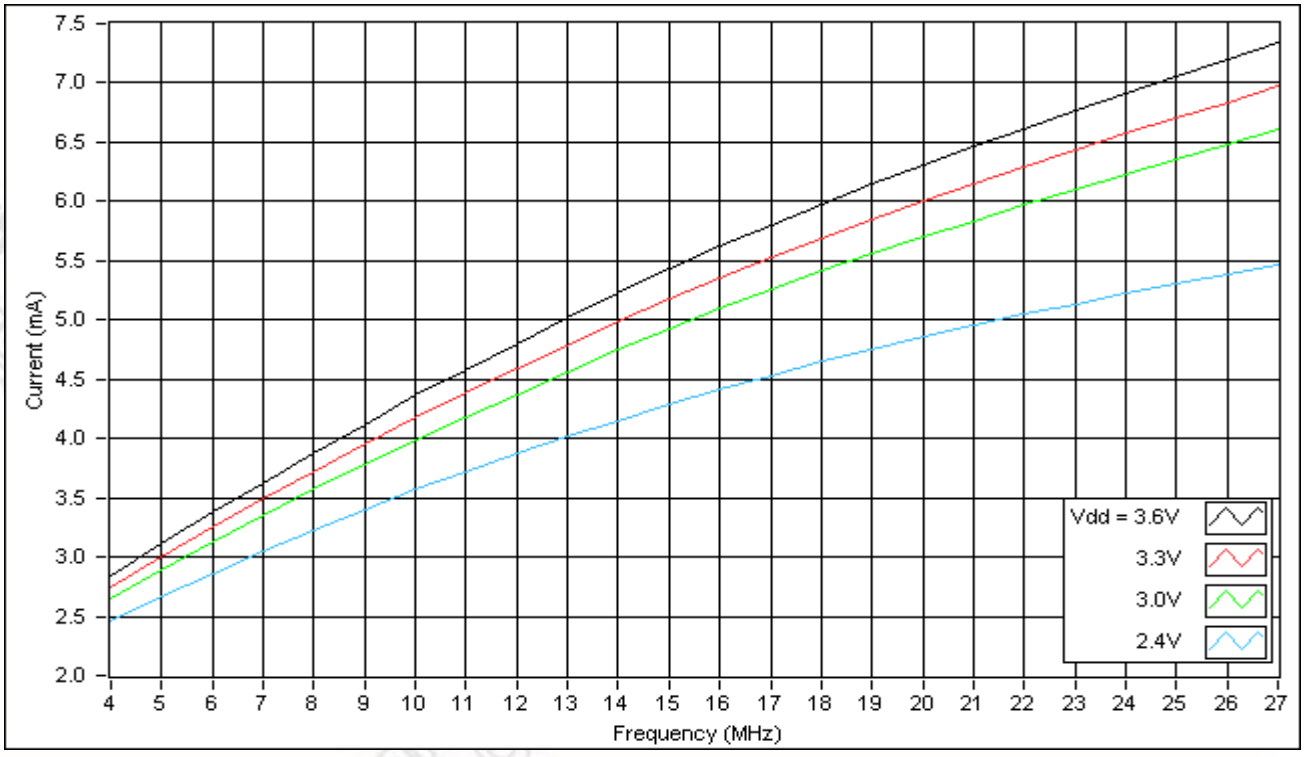


Figure 26–2. Supply Current Under 12T Mode, External Clock (2)

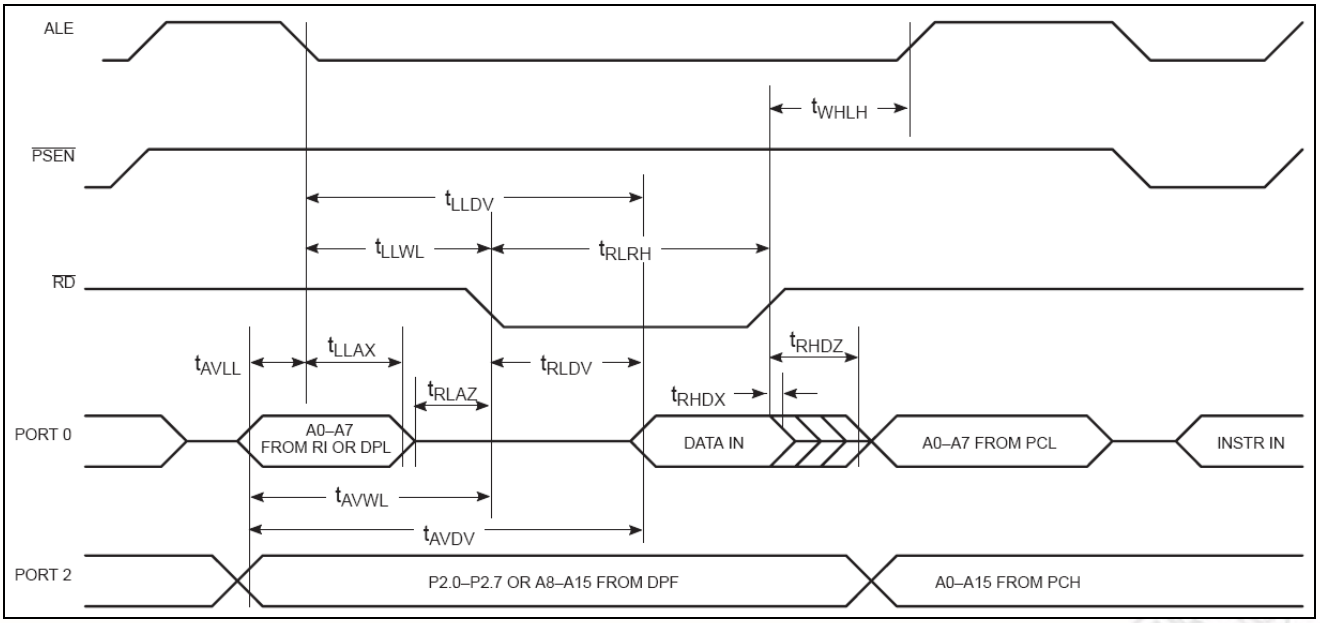


Figure 26–11. External Data Memory Read Cycle

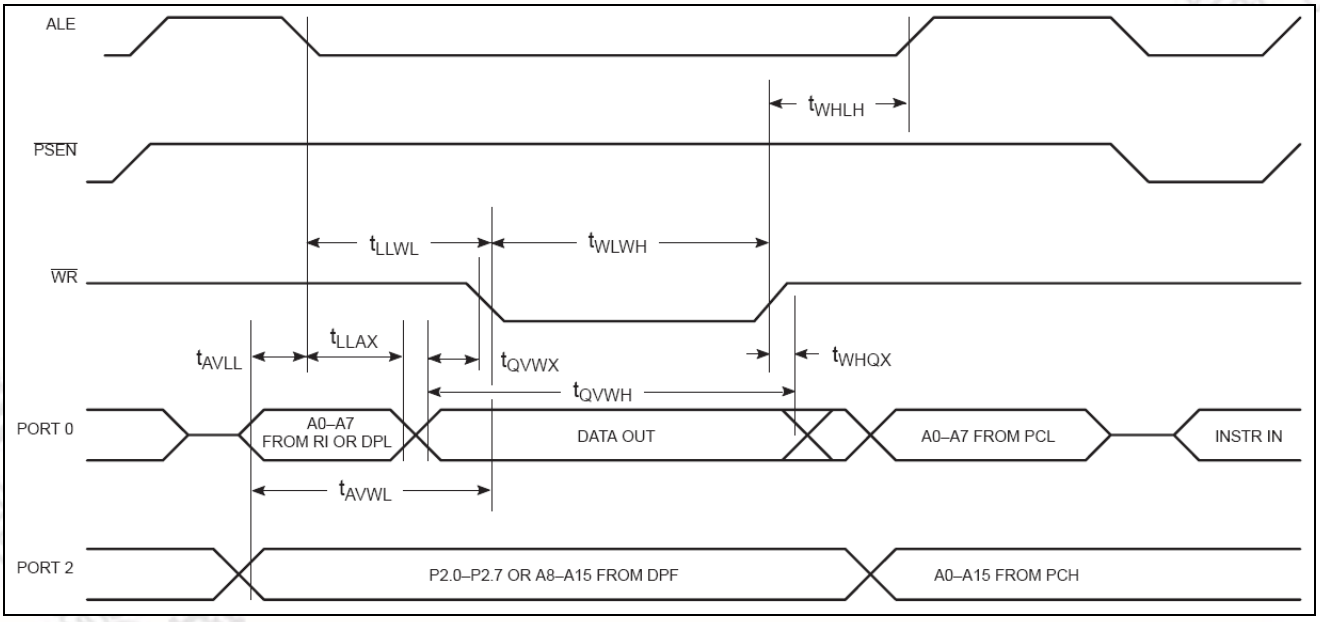


Figure 26–12. External Data Memory Write Cycle

Table 26–3. Characteristics of On-chip RC Oscillators

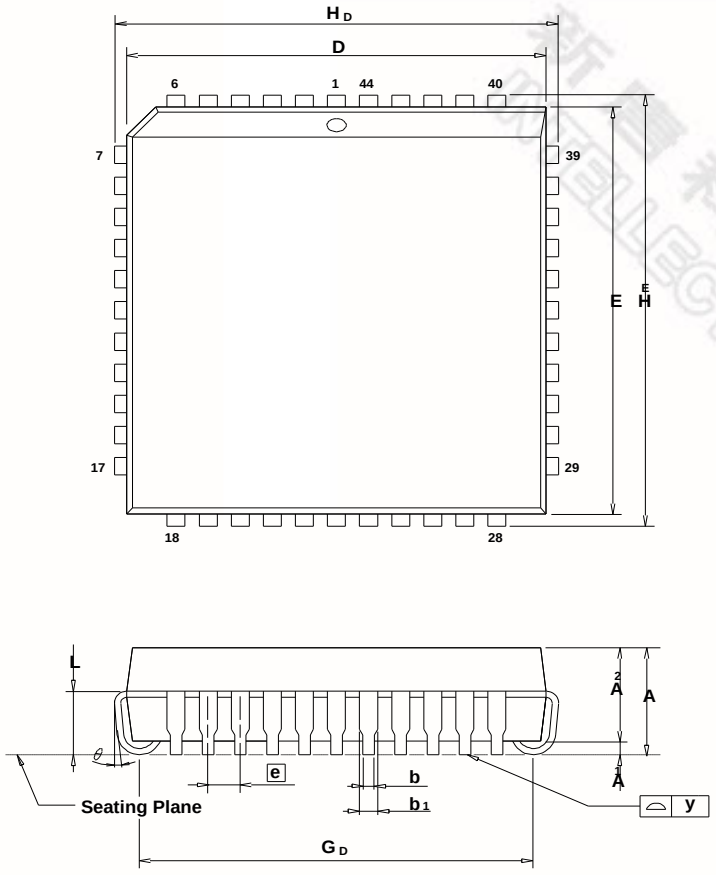
Symbol	Parameter	Condition	Frequency Deviation	Min.	Typ.	Max.	Unit
F_{IHRC}	System 22.1184MHz RC oscillator frequency[1][2]	25℃	1%	21.8972	22.1184	22.3396	MHz
		-40℃~85℃	3%	21.4548	22.1184	22.7820	MHz
F_{ILRC}	WDT and PDT 10kHz RC oscillator frequency		30%	7	10	13	kHz

[1] Internal 11.0592MHz is not listed for the same frequency deviation due to directly divided by 2 from 22.1184MHz source.

[2] A 0.1μF capacitor is recommended to be added on XTAL1 pin to gain the more precise frequency of the internal RC oscillator frequency if it is selected as the system clock source.

Table 26–4. Characteristics of Brown-out Detection

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
T_{BOD}	Brown-out detect pulse width	$V_{DD} < V_{BOD}$	600	-	-	μs
T_{BODRD}	Brown-out release delay period	$V_{DD} > V_{BOD}$	5.6	8	10.4	ms



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.185	—	—	4.70
A_1	0.020	—	—	0.51	—	—
A_2	0.145	0.150	0.155	3.68	3.81	3.94
b_1	0.026	0.028	0.032	0.66	0.71	0.81
b	0.016	0.018	0.022	0.41	0.46	0.56
c	0.008	0.010	0.014	0.20	0.25	0.36
D	0.648	0.653	0.658	16.46	16.59	16.71
E	0.648	0.653	0.658	16.46	16.59	16.71
e	0.050 BSC			1.27 BSC		
G_D	0.590	0.610	0.630	14.99	15.49	16.00
G_E	0.590	0.610	0.630	14.99	15.49	16.00
H_D	0.680	0.690	0.700	17.27	17.53	17.78
H_E	0.680	0.690	0.700	17.27	17.53	17.78
L	0.090	0.100	0.110	2.29	2.54	2.79
y	—	—	0.004	—	—	0.10

Figure 27–2. PLCC-44 Package Dimention