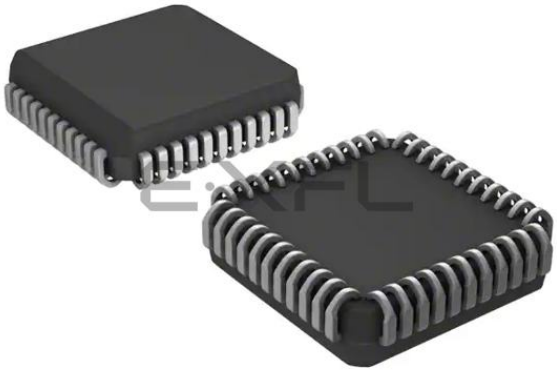

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Details	
Product Status	Last Time Buy
Core Processor	8051
Core Size	8-Bit
Speed	40MHz
Connectivity	EBI/EMI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.25K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/n78e366apg

3. BLOCK DIAGRAM

Figure 3–1 shows the functional block diagram of N78E366A. It gives the outline of the device. The user can find all the device's peripheral functions in the diagram.

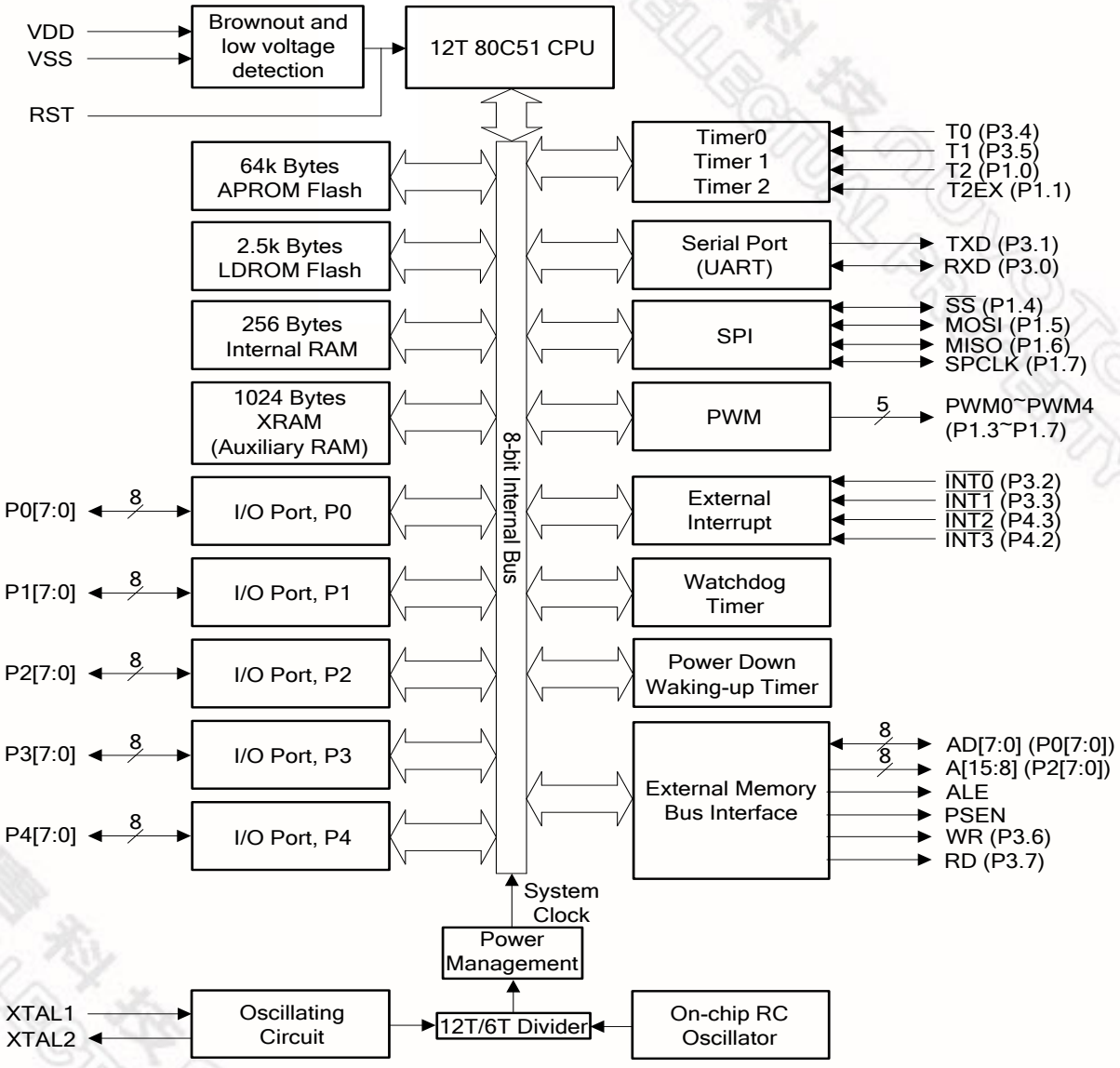


Figure 3–1. N78E366A Function Block Diagram

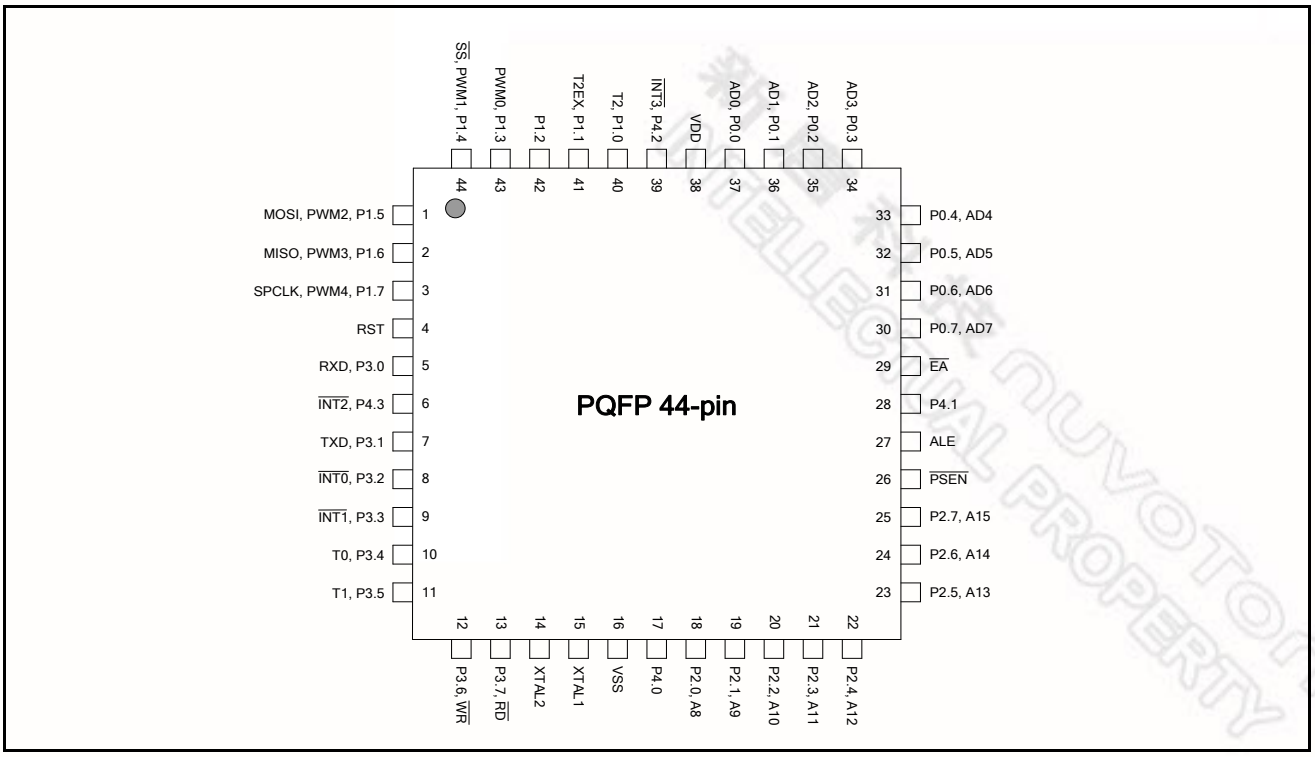


Figure 4–3. Pin Assignment of PQFP 44-Pin

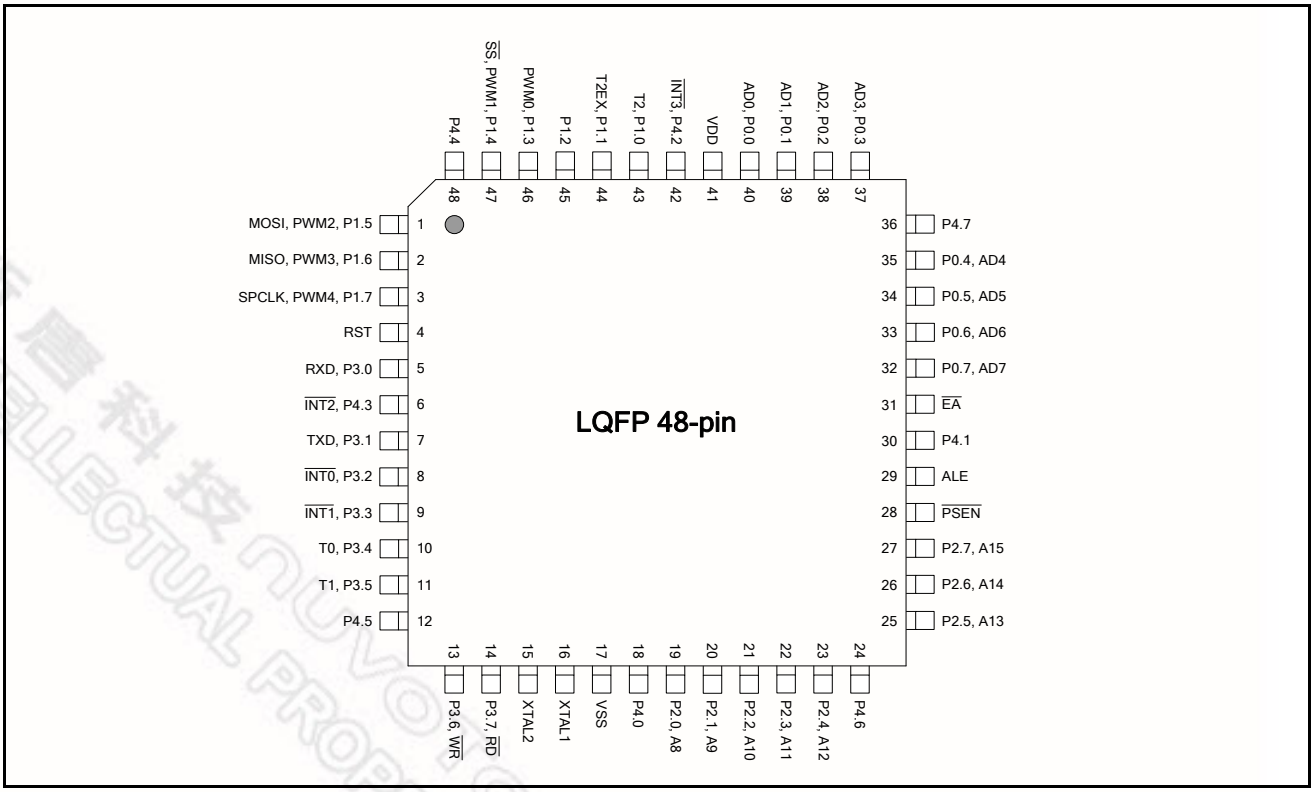


Figure 4–4. Pin Assignment of LQFP 48-Pin

5.3 Internal Data Memory

Figure 5–3 shows the internal and external Data Memory spaces available on N78E366A. Internal Data Memory can be divided into three blocks. They are the lower 128 bytes of RAM, the upper 128 bytes of RAM, and the 128 bytes of SFR space. Internal Data Memory addresses are always 8-bit wide, which implies an address space of only 256 bytes. Direct addressing higher than 7FH will access the special function registers (SFRs) space and indirect addressing higher than 7FH will access the upper 128 bytes of RAM. Although the SFR space and the upper 128 bytes of RAM share the same logic address, 80H through FFH, actually they are physically separate entities. Direct addressing to distinguish with the higher 128 bytes of RAM can only access these SFRs. Sixteen addresses in SFR space are both byte and bit-addressable. The bit-addressable SFRs are those whose addresses end in 0H or 8H.

The lower 128 bytes of internal RAM are present in all 8051 devices. The lowest 32 bytes are grouped into 4 banks of 8 registers. Program instructions call these registers as R0 through R7. Two bits RS0 and RS1 in the Program Status Word (PSW[3:4]) select which Register Bank is used. This benefits more efficiency of code space, since register instructions are shorter than instructions that use direct addressing. The next 16 bytes above the Register Banks (byte-address 20H through 2FH) form a block of bit-addressable memory space (bit-address 00H through 7FH). The 8051 instruction set includes a wide selection of single-bit instructions, and the 128 bits in this area can be directly addressed by these instructions. The bit addresses in this area are 00H through 7FH.

All bytes in the lower 128-byte space can be accessed by either direct or indirect addressing. Indirect addressing can only access the upper 128.

Another application implemented with the whole block of internal 256-byte RAM is for the stack. This area is selected by the Stack Pointer (SP), which stores the address of the top of the stack. Whenever a JMP, CALL or interrupt is invoked, the return address is placed on the stack. There is no restriction as to where the stack can begin in the RAM. By default however, the Stack Pointer contains 07H at reset. The user can then change this to any value desired. The SP will point to the last used value. Therefore, the SP will be incremented and then address saved onto the stack. Conversely, while popping from the stack the contents will be read first, and then the SP is decreased.

5.4 On-chip XRAM

N78E366A provides additional on-chip auxiliary RAM called XRAM to enlarge RAM space. The 1024 bytes of XRAM (000H to 3FFH) are indirectly accessed by move external instruction MOVX. For details, see Section 8. "AUXILIARY RAM (XRAM)" on page 28.

5.5 External Data Memory

Access to external Data Memory can use either a 16-bit address (using 'MOVX @DPTR') or an 8-bit address (using 'MOVX @Ri', i = 0 or 1). For another 1k-byte XRAM exists, remember the bit XRAMEN (CHPCON.4) should be cleared as logic 0 in order to access the range of 000H to 3FFH address of the external Data Memory.

16-bit addresses are often used to access up to 64k bytes of external RAM. Whenever a 16-bit address is used, P0, P2, P3.7 and P3.6 serve as the low byte address/data, the high byte address, $\overline{RD}$ strobe and $\overline{WR}$ strobe signals respectively. Meanwhile the pins listed above cannot be used as general purpose I/O during external Data Memory access.

8-bit addresses are often used in conjunction with one or more other I/O lines to page the RAM. For example, if a 1k-byte external RAM is used, Port 0 serves as a multiplexed address/data bus to the RAM, and 2 pins of Port 2 are used to page the RAM. The CPU generates $\overline{RD}$ and $\overline{WR}$ (alternate functions of P3.7 and P3.6) to strobe the memory. In 8-bit addressing mode, P2 pins other than the two pins for RAM paging are free for general purpose I/O usage. This will facilitate P2 application. Of course, the user may use any other I/O lines instead of P2 to page the RAM.

In all cases, the low byte of the address is time-multiplexed with the data byte on Port 0. ALE (Address Latch Enable) should be used to capture the address byte into an external latch. The address byte is valid at the negative transition of ALE. Then, in a write cycle, the data byte to be written appears on Port 0 just before $\overline{WR}$ is activated, and remains there until after $\overline{WR}$ is deactivated. In a read cycle, the incoming byte is accepted at Port 0 just before the read strobe is deactivated. During any access to external memory, the CPU writes 0FFH to the Port 0 latch (P0 in SFRs), thus obliterating whatever information the Port 0 SFR may have been holding.

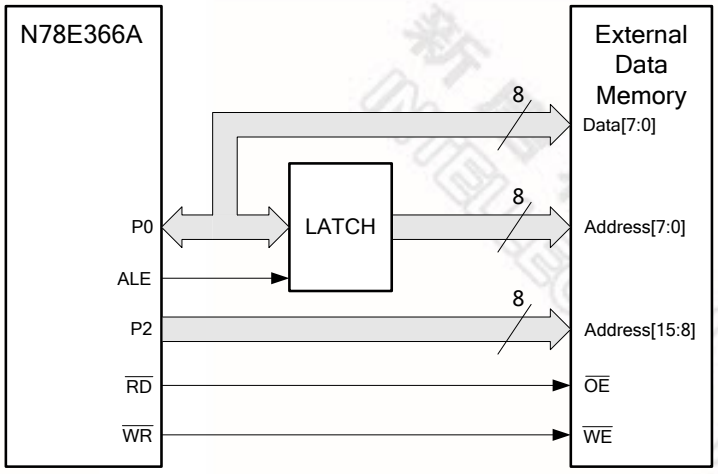


Figure 5–5. Data Memory Interface

PCON – Power Control

7	6	5	4	3	2	1	0
SMOD	-	-	POF	GF1	GF0	PD	IDL
r/w	-	-	r/w	r/w	r/w	r/w	r/w

Address: 87H reset value: see Table 6–2. N78E366A SFR Descriptions and Reset Values

Bit	Name	Description
3	GF1	**General purpose flag 1.** The general purpose flag that can be set or cleared by the user.
2	GF0	**General purpose flag 0.** The general purpose flag that can be set or cleared by the user.

9. I/O PORT STRUCTURE AND OPERATION

N78E366A has maximum five 8-bit width, bit-addressable ports P0~P4. The configuration of P1~P4 is the quasi bi-directional I/O. This type rules as both input and output. When the port outputs a logic high, it is weakly driven, allowing an external device to pull the pin low. When the pin is pulled low, it is driven strongly and able to sink a large current. In the quasi bi-directional I/O structure, there are three pull-up transistors. Each of them serves different purposes. One of these pull-ups, called the “very weak” pull-up, is turned on whenever the port latch contains a logic 1. The “very weak” pull-up sources a very small current that will pull the pin high if it is left floating.

A second pull-up, called the “weak” pull-up, is turned on when the outside port pin itself is at a logic 1 level. This pull-up provides the primary source current for a quasi bi-directional pin that is outputting a 1. If a pin that has a logic 1 on it is pulled low by an external device, the “weak” pull-up turns off, and only the “very weak” pull-up remains on. In order to pull the pin low under these conditions, the external device has to sink enough current (larger than I_{TL}) to overcome the “weak” pull-up and make the voltage on the port pin below its input threshold (lower than V_{IL}).

The third pull-up is the “strong” pull-up. This pull-up is used to speed up low-to-high transitions on a quasi bi-directional port pin when the port latch changes from a logic 0 to a logic 1. When this occurs, the strong pull-up turns on for two-peripheral-clock time in order to pull the port pin high quickly. Then it turns off and “weak: pull-up continues remaining the port pin high. The quasi bi-directional port structure is shown as below.

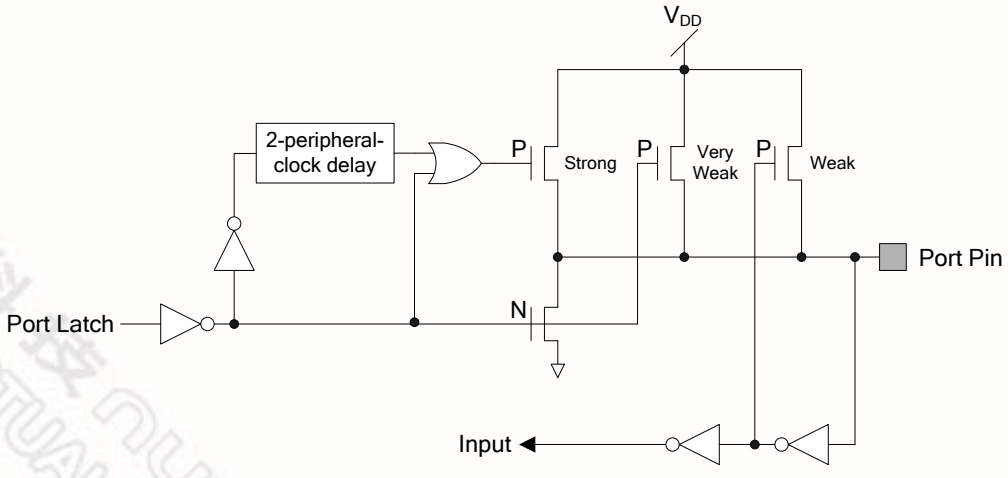


Figure 9–1. Quasi Bi-direction I/O Structure

The default configuration of P0 is open-drain structure. To serve as an I/O port the external pull-up resistor is always necessary. N78E366A also provide an internal P0 pull-up resistors for each pins. Via setting P0UP (P0OR.0) P0 will switch on its weak pull-up internally and behave the same as the quasi bi-directional I/O pins.

P0 and P2 also serve as address/data bus when external memory is running or is accessed by MOVC or MOVX instruction. In these cases, it has strong pull-up and pull-down. In this application, there is no need of any external pull-up resistor. While external mode execution, P0 and P2 cannot be used as general purpose I/O anymore.

In standard 8051 instruction set, one kind of instructions, read-modify-write instructions, should be specially taken care of. Instead of the normal instructions, the read-modify-write instructions read the internal port latch (Px in SFRs) rather than the external port pin state. This kind of instructions read the port SFR value, modify it and write back to the port SFR. Read-modify-write instructions are listed as follows.

Instruction		Description
ANL		Logical AND. (ANL Px,A and ANL Px,direct)
ORL		Logical OR. (ORL Px,A and ORL Px,direct)
XRL		Logical exclusive OR. (XRL Px,A and XRL Px,direct)
JBC		Jump if bit = 1 and clear it. (JBC Px.y,LABEL)
CPL		Complement bit. (CPL Px.y)
INC		Increment. (INC Px)
DEC		Decrement. (DEC Px)
DJNZ		Decrement and jump if not zero. (DJNZ Px,LABEL)
MOV	Px.y,C	Move carry bit to Px.y.
CLR	Px.y	Clear bit Px.y.
SETB	Px.y	Set bit Px.y.

The last three seems not obviously read-modify-write instructions but actually they are. They read the entire port latch value, modify the changed bit, then write the new value back to the port latch.

P0 – Port 0 (bit-addressable)

7	6	5	4	3	2	1	0
P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Address: 80H reset value: 1111 1111b

Bit	Name	Description
7:0	P0[7:0]	**Port 0.** Port 0 is an 8-bit open-drain port by default. Via setting P0UP (P0OR.0) P0 will switch as weakly pulled up internally. P0 has an alternative function as AD[7:0] while external memory accessing. During external Program Memory execution, SFR P0 cannot be accessed.

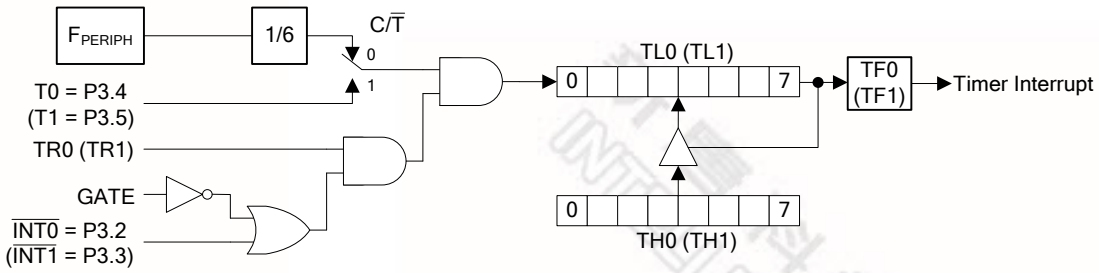


Figure 10–3. Timer/Counter 0 and 1 in Mode 2

10.1.4 Mode 3 (Two Separate 8-bit Timers)

Mode 3 has different operating methods for the two Timer/Counters. For Timer/Counter 1, Mode 3 simply freezes the counter. Timer/Counter 0, however, configures TL0 and TH0 as two separate 8 bit count registers in this mode. TL0 uses the Timer/Counter 0 control bits C/$\overline{T}$, GATE, TR0, $\overline{INT0}$, and TF0. The TL0 also can be used as a 1-to-0 transition counter on pin T0 as determined by C/$\overline{T}$ (TMOD.2). TH0 is forced as a clock cycle counter and takes over the usage of TR1 and TF1 from Timer/Counter 1. Mode 3 is used in case which an extra 8 bit timer is needed. If Timer/Counter 0 is configured in Mode 3, Timer/Counter 1 can be turned on or off by switching it out of or into its own Mode 3. It can still be used in Modes 0, 1 and 2 although its flexibility is restricted. It no longer has control over its overflow flag TF1 and the enable bit TR1. However Timer 1 can still be used as a Timer/Counter and retains the use of GATE and $\overline{INT1}$ pin. It can be used as a baud rate generator for the serial port or other application not requiring an interrupt.

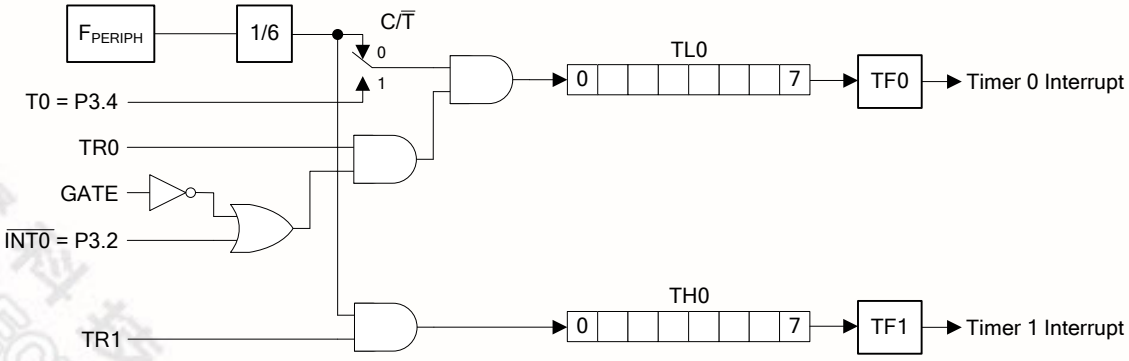


Figure 10–4. Timer/Counter 0 in Mode 3

12. POWER DOWN WAKING-UP TIMER

12.1 Function Description of Power Down Waking-up Timer

N78E366A provides another free-running Timer, Power Down waking-up timer which serves as a event timer or a durational system supervisor in a monitoring system which generally operates in Idle or Power Down modes. It is basic a setting of dividers that divide the peripheral clock. The divider output is selectable and determines the time-out interval. When the time-out interval is fulfilled, it will wake the system up from Idle or Power Down mode and an interrupt event will occur.

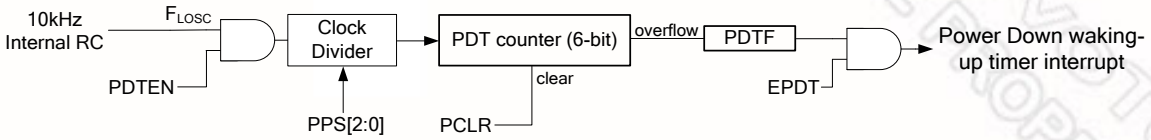


Figure 12–1. Power Down Waking-up Timer Block Diagram

The Power Down waking-up timer should first be reset 00H by using PDCLR(PDCON.6) to ensure that the timer starts from a known state. The PDCLR bit is used to restart the Power Down waking-up timer. This bit is self-cleared thus the user doesn't need to clear it. After writing a 1 to PDCLR, the hardware will automatically clear it. After PDTEN set as 1, the Power Down waking-up timer will start counting clock cycles. The time-out interval is selected by the three bits PPS2, PPS1, and PPS0 (PDCON[2:0]). When the selected time-out occurs, the Power Down waking-up timer will set the interrupt flag PDTF (PDCON.5). The Power Down waking-up timer interrupt enable bit locates at bit 1 in EIE. In general, software should restart the counter to put it into a known state by setting WDCLR.

PDCON – Power Down Waking-up Timer Control

7	6	5	4	3	2	1	0
PDTEN	PDCLR	PDTF	-	-	PPS2	PPS1	PPS0
r/w	w	r/w	-	-	r/w	r/w	r/w

Address: ABH reset value: 0000 0000b

Bit	Name	Description
7	PDTEN	**Power Down waking-up timer enable.** 0 = Disable Power Down waking-up timer. 1 = Enable Power Down waking-up timer. The PDT counter starts running.
6	PDCLR	**Power Down waking-up timer clear.** Setting this bit will reset the Power Down waking-up timer count to 00H. It put the counter in a known state. This bit is written-only and has no need to be cleared via software.

of Idle mode still keeps at a “mA” level. To further reducing the current consumption to “μA” level, the CPU should stay in Power Down mode when nothing needs to be served, and has the ability of waking up at a programmable interval. N78E366A is equipped with this useful function. It provides a very low power internal RC 10kHz. Along with the low power consumption application, the Power Down Waking-up timer needs to count under Idle and Power Down mode and wake CPU up from Idle or Power Down mode. The demo code to accomplish this feature is shown below.

The demo code of Power Down waking-up timer waking up CPU from Power Down.

```
       ORG    0000H
       LJMP   START

       ORG    004BH
       LJMP   PDT_ISR

       ORG    0100H
PDT_ISR:
       ORL    PDCON,#01000000B          ;Clear Power Down Waking-up timer counter
       ANL    PDCON,#11011111B          ;Clear Power Down Waking-up timer interrupt flag
       RETI

START:
       ORL    PDCON,#00000111B          ;Choose interval length
       ORL    EIE,#00000010B            ;Enable Power Down Waking-up timer interrupt
       SETB   EA
       ORL    PDCON,#10000000B          ;Enable Power Down Waking-up timer to run

;*********************************************************************
;Enter into Power Down mode
;*********************************************************************
LOOP:
       ORL    PCON,#02H
       LJMP   LOOP
```

This gives a repetition frequency range of 122Hz to 31.25kHz (F_{PERIPH} = 16MHz). By loading the PWMx registers with either 00H or FFH, the PWM channels will generate a constant low or high level output, respectively.

When a compare register PWMx is loaded with a new value, the associated output updated immediately. It does not have to wait until the end of the current counter period.

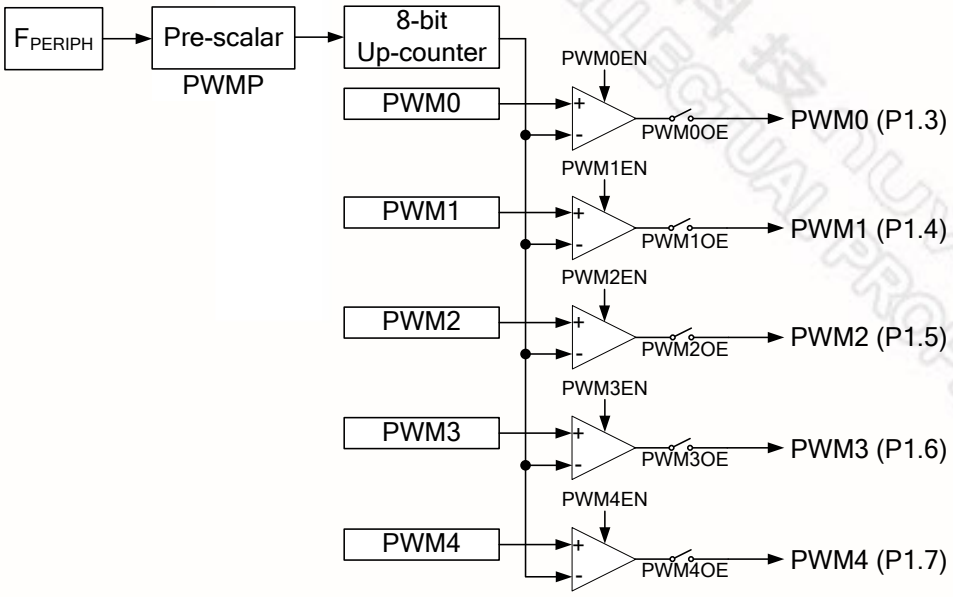


Figure 15–1. PWM Function Block

PWM demo code,

```
MOV     PWMP,#128               ;determine PWM period
MOV     PWM0,#0H                ;duty = 0%
MOV     PWM1,#40H               ;duty = 25%
MOV     PWM2,#80H               ;duty = 50%
MOV     PWM3,#0C0H              ;duty = 75%
MOV     PWM4,#0FFH              ;duty = 100%
ORL     PWMCON0,#00110011b      ;enable PWM0~3
ORL     PWMCON1,#00000001b      ;enable PWM4
ORL     PWMCON0,#11001100b      ;output enable PWM0~3
ORL     PWMCON1,#00000100b      ;output enable PWM4
```

16. TIMED ACCESS PROTECTION (TA)

N78E366A has several features like the Watchdog Timer, the ISP function, Boot select control, etc. are crucial to proper operation of the system. If leaving these control registers unprotected, errant code may write undetermined value into them, it results in incorrect operation and loss of control. In order to prevent this risk, the N78E366A has a protection scheme which limits the write access to critical SFRs. This protection scheme is done using a timed access. The following registers are related to TA process.

TA – Timed Access

7	6	5	4	3	2	1	0
TA[7:0]							
w							

Address: C7H reset value: 0000 0000b

Bit	Name	Description
7:0	TA[7:0]	**Timed access.** The timed access register controls the access to protected SFRs. To access protected bits, the user must first write AAH to the TA and immediately followed by a write of 55H to TA. After these two steps, a writing permission window is opened for three machine-cycles during which the user may write to protected SFRs.

In timed access method, the bits, which are protected, have a timed write enable window. A write is successful only if this window is active, otherwise the write will be discarded. When the software writes AAH to TA, a counter is started. This counter waits for three machine-cycles looking for a write of 55H to TA. If the second write of 55H occurs within three machine-cycles of the first write of AAH, then the timed access window is opened. It remains open for three machine-cycles during which the user may write to the protected bits. After three machine-cycles, this window automatically closes. Once the window closes, the procedure must be repeated to access the other protected bits. Not that the TA protected SFRs are required timed access for writing. But the reading is not protected. The user may read TA protected SFR without giving AAH and 55H to TA. The suggestion code for opening the timed access window is shown below.

```
(CLR    EA)                 ;if any interrupt is enabled, disable temporally
 MOV    TA,#0AAH
 MOV    TA,#55H
(Instruction that writes a TA protected register)
(SETB   EA)                 ;resume interrupts enabled
```

The writings of AAH, 55H to TA register and the writing-protection register must occur within 3 machine-cycles of each other. Any enabled interrupt should be disabled during this procedure to avoid delay between these three writings. If there is no interrupt enabled, the `CLR EA` and `SETB EA` instructions can be left out. Once the timed access window closes, the procedure must be repeated to access the other protected bits.

Bit	Name	Description
5	PT2	**Timer 2 interrupt priority low bit.**
4	PS	**Serial port (UART) interrupt priority low bit.**
3	PT1	**Timer 1 interrupt priority low bit.**
2	PX1	**External interrupt 1 priority low bit.**
1	PT0	**Timer 0 interrupt priority low bit.**
0	PX0	**External interrupt 0 priority low bit.**

[1] IP is used in combination with the IPH to determine the priority of each interrupt source. See Table 17–2. Interrupt Priority Level Setting for correct interrupt priority configuration.

IPH – Interrupt Priority High

7	6	5	4	3	2	1	0
PX3H[2]	PX2H[2]	PT2H[3]	PSH[3]	PT1H[3]	PX1H[3]	PT0H[3]	PX0H[3]
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Address: BAH reset value: 0000 0000b

Bit	Name	Description
7	PX3H	**External interrupt 3 priority high bit.**
6	PX2H	**External interrupt 3 priority high bit.**
5	PT2H	**Timer 2 interrupt priority high bit.**
4	PSH	**Serial port (UART) interrupt priority high bit.**
3	PT1H	**Timer 1 interrupt priority high bit.**
2	PX1H	**External interrupt 1 priority high bit.**
1	PT0H	**Timer 0 interrupt priority high bit.**
0	PX0H	**External interrupt 0 priority high bit.**

[2] PX2H and PX3H are used in combination with the PX2 (XICON.3) and PX3 (XICON.7) respectively to determine the priority of external interrupt 2 and 3. See Table 17–2. Interrupt Priority Level Setting for correct interrupt priority configuration.

[3] These bits is used in combination with the IP respectively to determine the priority of each interrupt source. See Table 17–2. Interrupt Priority Level Setting for correct interrupt priority configuration.

EIP – Extensive Interrupt Priority[4]

7	6	5	4	3	2	1	0
-	-	-	-	-	PBOD	PPDT	PSPI
-	-	-	-	-	r/w	r/w	r/w

Address: BCH reset value: 0000 0000b

Bit	Name	Description
7:3	-	**Reserved.**
2	PBOD	**Brown-out detection interrupt priority low bit.**
1	PPDT	**Power Down waking-up timer interrupt priority low bit.**
0	PSPI	**SPI interrupt priority low bit.**

[4] EIP is used in combination with the EIPH to determine the priority of each interrupt source. See Table 17–2. Interrupt Priority Level Setting for correct interrupt priority configuration.

EIPH – Extensive Interrupt Priority High[1]

7	6	5	4	3	2	1	0
-	-	-	-	-	PBODH	PPDTH	PSPIH
-	-	-	-	-	r/w	r/w	r/w

Address: BBH reset value: 0000 0000b

Bit	Name	Description
7:3	-	**Reserved.**
2	PBODH	**Brown-out detection interrupt priority high bit.**
1	PPDTH	**Power Down waking-up timer interrupt priority high bit.**
0	PSPIH	**SPI interrupt priority high bit.**

[1] EIPH is used in combination with the EIP to determine the priority of each interrupt source. See Table 17–2. Interrupt Priority Level Setting for correct interrupt priority configuration.

TCON – Timer 0 and 1 Control (bit-addressable)

7	6	5	4	3	2	1	0
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Address: 88H reset value: 0000 0000b

Bit	Name	Description
3	IE1	**External interrupt 1 edge flag.** This flag is set via hardware when an edge/level of type defined by IT1 is detected. If IT1 = 1, this bit will remain set until cleared via software or at the beginning of the External Interrupt 1 service routine. If IT1 = 0, this flag is the inverse of the $\overline{INT1}$ input signal's logic level.
2	IT1	**External interrupt 1 type select.** This bit selects whether the $\overline{INT1}$ pin will detect falling edge or low level triggered interrupts. 0 = $\overline{INT1}$ is low level triggered. 1 = $\overline{INT1}$ is falling edge triggered.
1	IE0	**External interrupt 0 edge flag.** This flag is set via hardware when an edge/level of type defined by IT0 is detected. If IT0 = 1, this bit will remain set until cleared via software or at the beginning of the External Interrupt 0 service routine. If IT0 = 0, this flag is the inverse of the $\overline{INT0}$ input signal's logic level.
0	IT0	**External interrupt 0 type select.** This bit selects whether the $\overline{INT0}$ pin will detect falling edge or low level triggered interrupts. 0 = $\overline{INT0}$ is low level triggered. 1 = $\overline{INT0}$ is falling edge triggered.

CHPCON – Chip Control (TA protected)

7	6	5	4	3	2	1	0
SWRST	ISPF	LDUEN	XRAMEN	-	-	BS	ISPEN
w	r/w	r/w	r/w	-	-	r/w	r/w

Address: 9FH reset value: see Table 6–2. N78E366A SFR Descriptions and Reset Values

Bit	Name	Description
0	ISPEN	**ISP enable.** 0 = Enable ISP function. 1 = Disable ISP function. To enable ISP function will start the internal 22.1184MHz RC oscillator for timing control. To clear ISPEN should always be the last instruction after ISP operation in order to stop internal RC for reducing power consumption.

PMC – Power Monitoring Control (TA protected)

7	6	5	4	3	2	1	0
BODEN	-	-	BORST	BOF	LPBOD	-	BOS
r/w	-	-	r/w	r/w	r/w	-	r

Address: ACH reset value: see Table 6–2. N78E366A SFR Descriptions and Reset Values

Bit	Name	Description
3	LPBOD	**Low power Brown-out detection enable.** This bit switches the Brown-out detection into a power saving mode. This bit is only effective while BODEN = 1. 0 = Disable Brown-out power saving mode. Brown-out detection operates in normal mode if enabled. The detection is always on. 1 = Enable Brown-out power saving mode. Brown-out detection operates in power saving mode if enabled. Enable this bit will switch on internal 10kHz RC to be a timer for about 12.8ms interval of detection. The discrete detection will save much power but the hysteresis feature disappears.

20.2 External Clock Source

The system clock source can be from external XTAL1 pin. When XTAL1 pin is driven by an external clock source, XTAL2 should be left floating. XTAL1 and XTAL2 are the input and output, respectively, of an internal inverting amplifier. A crystal or resonator can be used by connecting between XTAL1 and XTAL2 pins. The crystal or resonator frequency from 4MHz up to 40MHz is allowed. While an external crystal or resonator is used, ROG (CONFIG3.5) is for half gain selection of the inverting amplifier. When the system clock is lower than 24MHz and ROG is configured as a 0, the system EMI can be reduced. CKF (CONFIG3.4) is the control bit of clock filter circuit of XTAL1 input pin.

20.3 On-chip RC Oscillator

The on-chip RC oscillator is enabled while FOSC (CONFIG3.1) is 0. Setting INTOSCFS (CONFIG3.3) logic 0 will switch to a divided-by-2 path. Note that a 0.1μF capacitor is recommended to be added on XTAL1 pin to gain the more precise frequency of the internal RC oscillator frequency if it is selected as the system clock source.

CONFIG2

7	6	5	4	3	2	1	0
CBODEN	CBOV1	CBOV0	CBORST	-	-	-	-
r/w	r/w	r/w	r/w	-	-	-	-

unprogrammed value: 1111 1111b

Bit	Name	Description
7	CBODEN	**CONFIG Brown-out detect enable.** 1 = Enable Brown-out detection. 0 = Disable Brown-out detection.
6 5	CBOV1 CBOV0	**CONFIG Brown-out voltage select.** These two bits select one of four Brown-out voltage level. CBOV1 CBOV0 Brown-out Voltage 1 1 2.2V 1 0 2.7V 0 1 3.8V 0 0 4.5V
4	CBORST	**CONFIG Brown-out reset enable.** This bit decides if a Brown-out reset is caused after a Brown-out event. 1 = Enable Brown-out reset when V_{DD} drops below V_{BOD}. 0 = Disable Brown-out reset when V_{DD} drops below V_{BOD}.

PMC – Power Monitoring Control (TA protected)

7	6	5	4	3	2	1	0
BODEN[1]	-	-	BORST[1]	BOF	LPBOD	-	BOS
r/w	-	-	r/w	r/w	r/w	-	r

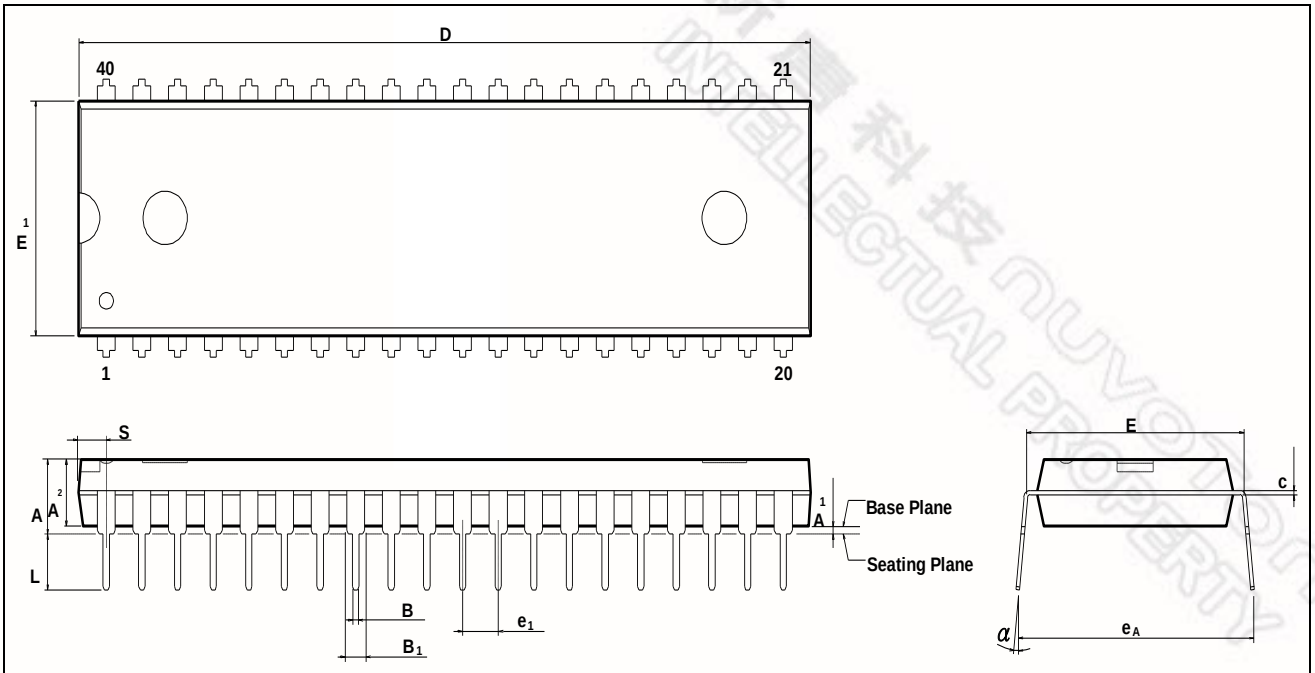
Address: ACH reset value: see Table 6–2. N78E366A SFR Descriptions and Reset Values

Bit	Name	Description
7	BODEN	**Brown-out detect enable.** 0 = Disable Brown-out detection. 1 = Enable Brown-out detection.
6:5	-	**Reserved.**
4	BORST	**Brown-out reset enable.** This bit decides if a Brown-out reset is caused after a Brown-out event. 0 = Disable Brown-out reset when V_{DD} drops below V_{BOD}. 1 = Enable Brown-out reset when V_{DD} drops below V_{BOD}.
3	BOF	**Brown-out flag.** This flag will be set as a logic 1 via hardware after a V_{DD} dropping below or rising above V_{BOD} event occurs. If both EBOD (EIE.2) and EA (IE.7) are set, a Brown-out interrupt requirement will be generated. This bit must be cleared via software.
3	LPBOD	**Low power Brown-out detection enable.** This bit switches the Brown-out detection into a power saving mode. This bit is only effective while BODEN = 1. 0 = Disable Brown-out power saving mode. Brown-out detection operates in normal mode if enabled. The detection is always on. 1 = Enable Brown-out power saving mode. Brown-out detection operates in power saving mode if enabled. Enable this bit will switch on internal 10kHz RC to be a timer for about 12.8ms interval of detection. The discrete detection will save much power but the hysteresis feature disappears.

Table 25–1. Instruction Set for N78E366A

Instruction		OPCODE	Bytes	Clock Cycles in 12T Mode	Clock Cycles in 6T Mode
INC	A	04	1	12	6
INC	Rn	08~0F	1	12	6
INC	@Ri	06, 07	1	12	6
INC	direct	05	2	12	6
INC	DPTR	A3	1	24	12
DEC	A	14	1	12	6
DEC	Rn	18~1F	1	12	6
DEC	@Ri	16, 17	1	12	6
DEC	direct	15	2	12	6
MUL	AB	A4	1	48	24
DIV	AB	84	1	48	24
DA	A	D4	1	12	6
ANL	A, Rn	58~5F	1	12	6
ANL	A, @Ri	56, 57	1	12	6
ANL	A, direct	55	2	12	6
ANL	A, #data	54	2	12	6
ANL	direct, A	52	2	12	6
ANL	direct, #data	53	3	24	12
ORL	A, Rn	48~4F	1	12	6
ORL	A, @Ri	46, 47	1	12	6
ORL	A, direct	45	2	12	6
ORL	A, #data	44	2	12	6
ORL	direct, A	42	2	12	6
ORL	direct, #data	43	3	24	12
XRL	A, Rn	68~6F	1	12	6
XRL	A, @Ri	66, 67	1	12	6
XRL	A, direct	65	2	12	6
XRL	A, #data	64	2	12	6
XRL	direct, A	62	2	12	6
XRL	direct, #data	63	3	24	12
CLR	A	E4	1	12	6
CPL	A	F4	1	12	6
RL	A	23	1	12	6
RLC	A	33	1	12	6
RR	A	03	1	12	6
RRC	A	13	1	12	6
SWAP	A	C4	1	12	6
MOV	A, Rn	E8~EF	1	12	6
MOV	A, @Ri	E6, E7	1	12	6
MOV	A, direct	E5	2	12	6

27. PACKAGES



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.210	—	—	5.33
A_1	0.010	—	—	0.25	—	—
A_2	0.150	0.155	0.160	3.81	3.94	4.06
B	0.016	0.018	0.022	0.41	0.46	0.56
B_1	0.048	0.050	0.054	1.22	1.27	1.37
c	0.008	0.010	0.014	0.20	0.25	0.36
D	—	2.055	2.070	—	52.20	52.58
E	0.590	0.600	0.610	14.99	15.24	15.49
E_1	0.540	0.545	0.550	13.72	13.84	13.97
e_1	0.090	0.100	0.110	2.29	2.54	2.79
L	0.120	0.130	0.140	3.05	3.30	3.56
α	0	—	15	0	—	15
e_A	0.630	0.650	0.670	16.00	16.51	17.02
S	—	—	0.090	—	—	2.29

Figure 27–1. DIP-40 Package Dimention

28. DOCUMENT REVISION HISTORY

Version	Date	Page	Description
V1.0	2010/8/13		Initial release.
V1.1	2010/9/20	124	Increase the maximum value of Power Down mode current.
V1.2	2010/12/1	79 94 85	1. Add restriction of disabling interrupts during TA protected writing. 2. Add restriction of disabling interrupts during ISP. 3. Add more descriptions of software clearing interrupt flags.
V2.0	2011/3/11	28	Change XRAM default state “enabled” after all resets to fit general applications.