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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	23
Program Memory Size	16KB (16K x 8)
Program Memory Type	ROM
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.9V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.600", 15.24mm)
Supplier Device Package	28-DIP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86l8808pscr2607

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ZiLOG Worldwide Headquarters
532 Race Street
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Telephone: 408.558.8500
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Pin Description

The pin assignment for the 28-pin dual in-line package (DIP)/small outline integrated circuit (SOIC) is shown in Figure 3. The pins are identified in Table 3.

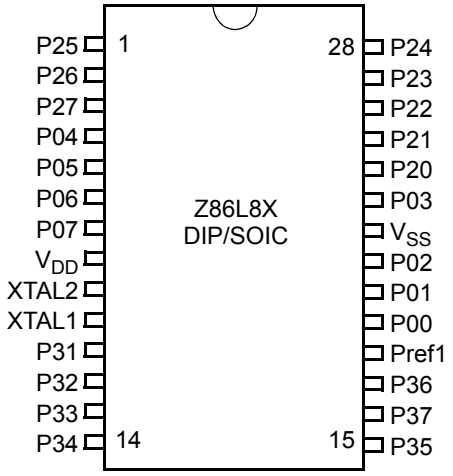


Figure 3. 28-Pin DIP/SOIC Pin Assignment

Table 3. 28-Pin DIP and SOIC Pin Identification

28-Pin DIP and SOIC	Standard Mode	Direction	Description
19	P00	Input/Output	Port 0 is nibble programmable.
20	P01	Input/Output	Port 0–3 can be configured as a
21	P02	Input/Output	mouse/trackball input.
23	P03	Input/Output	
4	P04	Input/Output	
5	P05	Input/Output	
6	P06	Input/Output	
7	P07	Input/Output	
24	P20	Input/Output	Port 2 pins are individually
25	P21	Input/Output	configurable as input or output.
26	P22	Input/Output	
27	P23	Input/Output	
28	P24	Input/Output	
1	P25	Input/Output	
2	P26	Input/Output	
3	P27	Input/Output	
18	Pref1	Input	Analog ref input; connect to V_{CC} if not used

Table 3. 28-Pin DIP and SOIC Pin Identification (Continued)

28-Pin DIP and SOIC	Standard Mode	Direction	Description
11	P31	Input	IRQ2/modulator input
12	P32	Input	IRQ0
13	P33	Input	IRQ1
14	P34	Output	T8 output
15	P35	Output	T16 output
17	P36	Output	T8/T16 output
16	P37	Output	
10	XTAL1	Input	Crystal, oscillator clock
9	XTAL2	Output	Crystal, oscillator clock
8	V_{DD}		Power supply
22	V_{SS}		Ground

Absolute Maximum Ratings

Table 4 lists the absolute maximum ratings for the Z86L82/85/88 microcontrollers.

Table 4. Absolute Maximum Ratings

Symbol	Description	Min	Max	Units
V_{max}	Supply Voltage (*)	–0.3	+7.0	V
T_{STG}	Storage Temperature	–65°	+150°	C
T_A	Oper. Ambient Temperature		†	C

Notes:
* Voltage on all pins with respect to GND
† See “Ordering Information” on page 69.

Stresses greater than those listed under Absolute Maximum Ratings might cause permanent damage to the device. This rating is a stress rating only. Functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period might affect device reliability.

Table 7. AC Characteristics (Continued)

			T_A = 0°C to +70°C 8.0 MHz					Stop-Mode Recovery
Number	Symbol	Parameter	V_{CC}	Min	Max	Units	Notes	(D1, D0)
12	Twdt	Watch-Dog Timer Delay Time	2.0 V	20		ms	5	0, 0
			3.6 V	7.5		ms	5	
			2.0 V	20		ms	5	0, 1
			3.6 V	7.5		ms	5	
			2.0 V	40		ms	5	1, 0
			3.6 V	15		ms	5	
		(60 ms)	2.0 V	160		ms	5	1, 1
			3.6 V	60		ms	5	

Notes:
1. Timing Reference uses 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33–P31)
3. Interrupt request through Port 3 (P30)
4. SMR – D5 = 0.
5. For internal RC oscillator

Functional Description

The Z86L8X incorporates special functions to enhance the Z8's functionality in consumer and battery-operated applications.

Program Memory

The Z86L8X family addresses 4/8/16 KB of internal program memory. The first 12 bytes are reserved for interrupt vectors. These locations contain the five 16-bit vectors that correspond to the five available interrupts.

RAM

The Z86L8X device has 237 bytes of RAM that make up the register file.

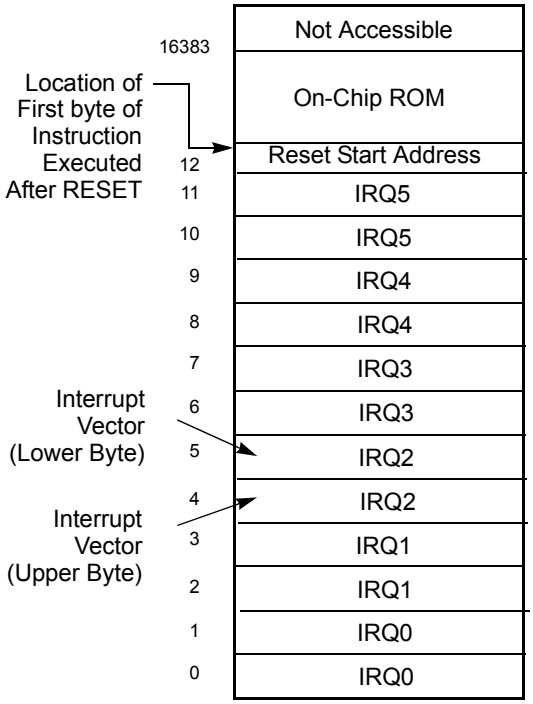
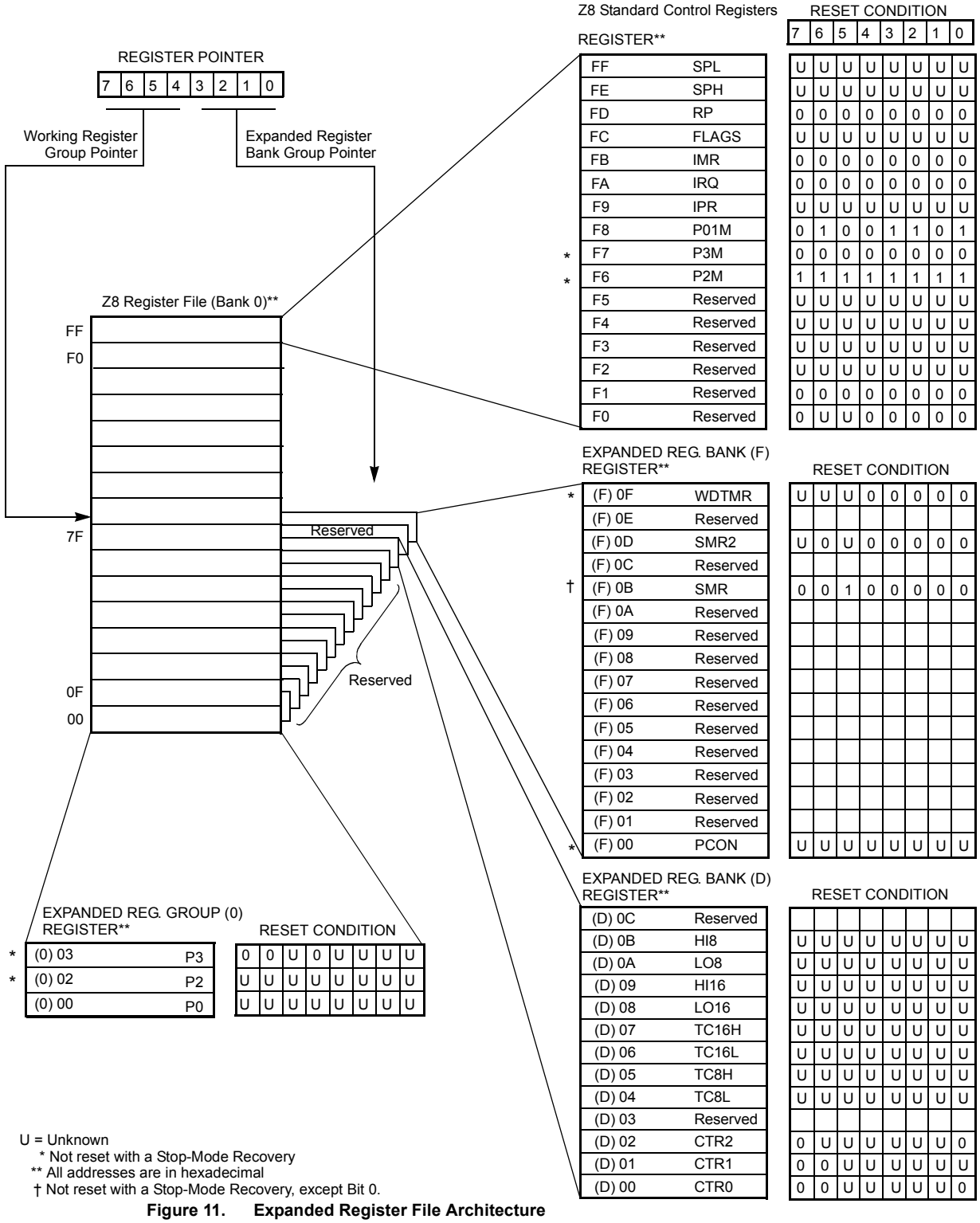


Figure 10. Program Memory Map (16K ROM)

Expanded Register File

The register file has been expanded to allow for additional system control registers and for mapping of additional peripheral devices into the register address area. The Z8 register address space R0 through R15 has been implemented as



U = Unknown
* Not reset with a Stop-Mode Recovery
** All addresses are in hexadecimal
† Not reset with a Stop-Mode Recovery, except Bit 0.

Figure 11. Expanded Register File Architecture

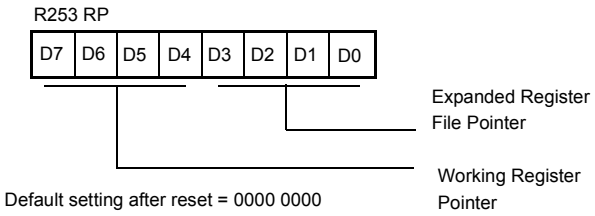


Figure 12. Register Pointer Register

Expanded Register File Control Registers (0D)

Figure 13, Figure 14, and Figure 15 show the expanded register file control registers (0D).

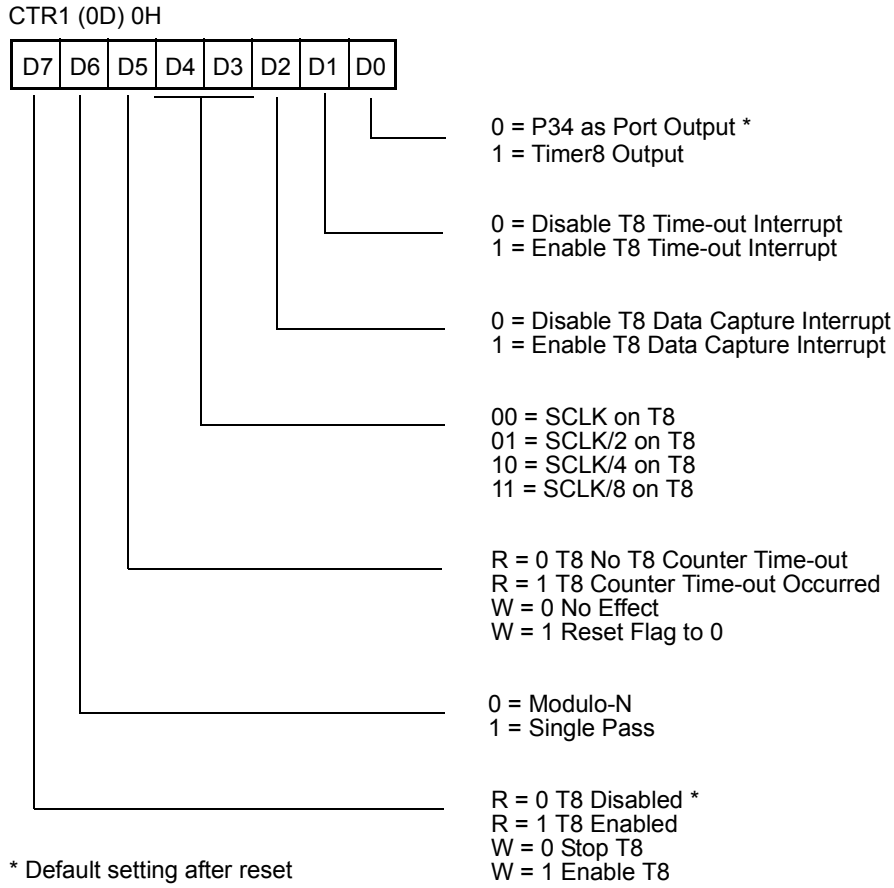


Figure 13. TC8 Control Register—(0D) OH: Read/Write Except Where Noted

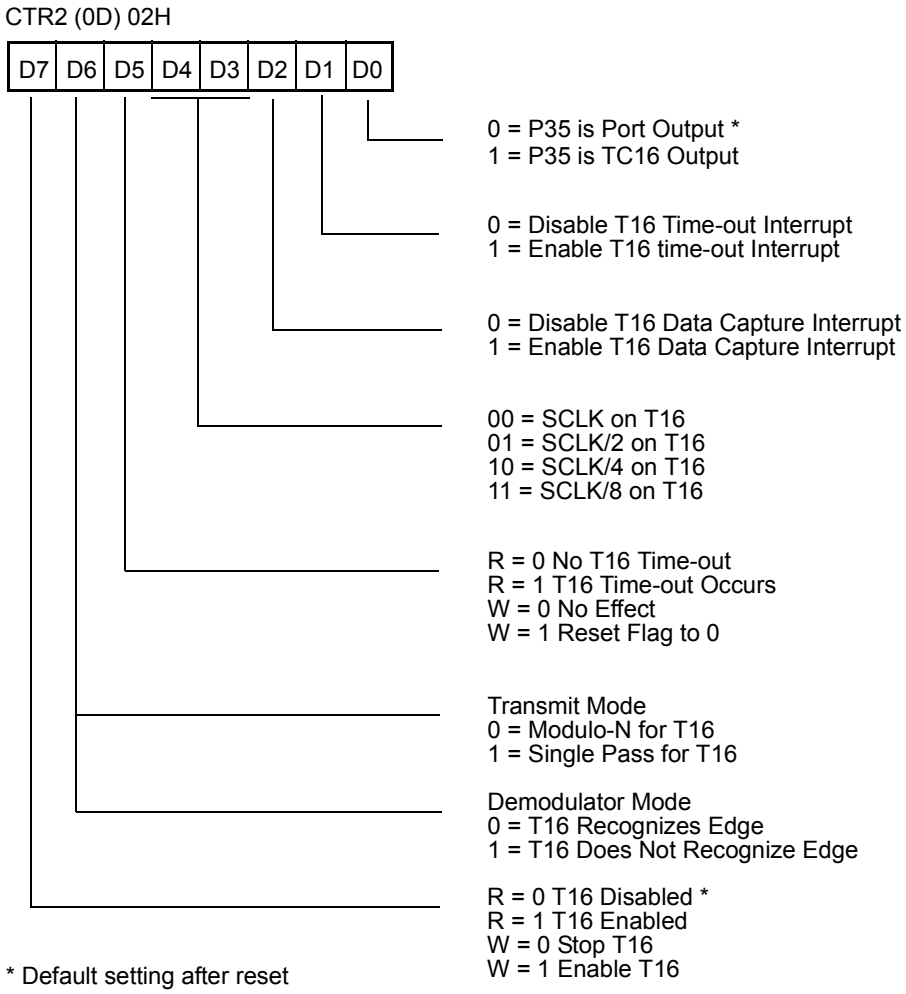
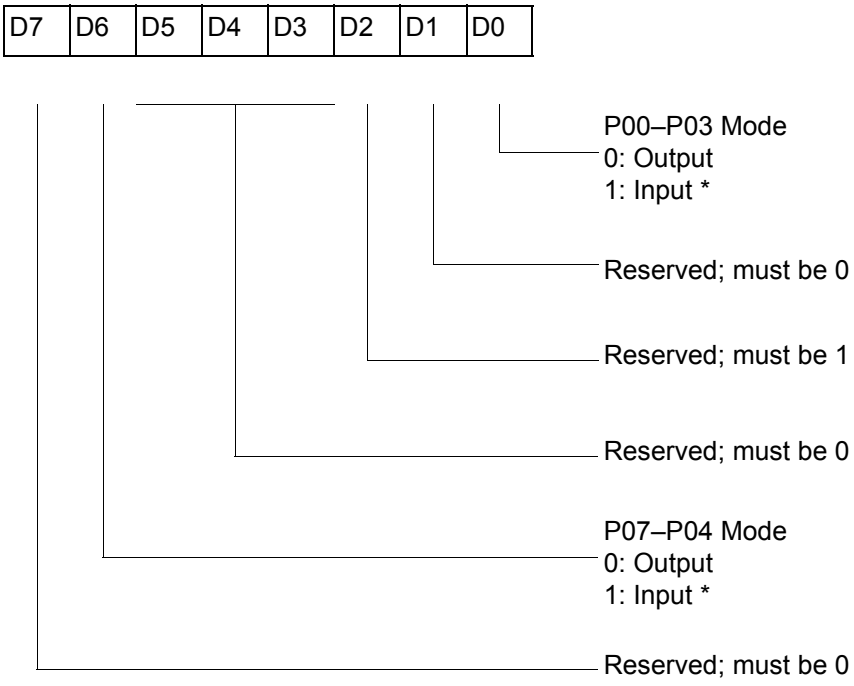


Figure 15. T16 Control Register—(0D) 2H: Read/Write Except Where Noted

R248 P01M



* Default setting after reset

Figure 22. Port 0 and 1 Mode Register (F8h: Write Only)

Table 19. CTR1(D)01h Register (Continued)

Field	Bit Position		Value	Description
Initial_T8_Out/Rising_Edge	------1-			Transmit Mode
		R/W	0	T8_OUT is 0 Initially
			1	T8_OUT is 1 Initially
				Demodulation Mode
		R	0	No Rising Edge
			1	Rising Edge Detected
		W	0	No Effect
			1	Reset Flag to 0
Initial_T16_Out/Falling_Edge	-------0			Transmit Mode
		R/W	0	T16_OUT is 0 Initially
			1	T16_OUT is 1 Initially
				Demodulation Mode
		R	0	No Falling Edge
			1	Falling Edge Detected
		W	0	No Effect
			1	Reset Flag to 0

Note:
*Default upon Power-On Reset

Mode

If it is 0, the counter/timers are in the transmit mode; otherwise, they are in the demodulation mode.

P36_Out/Demodulator_Input

In transmit mode, this bit defines whether P36 is used as a normal output pin or the combined output of T8 and T16.

In demodulation mode, this bit defines whether the input signal to the counter/timers is from P20 or P31.

T8/T16_Logic/Edge_Detect

In transmit mode, this field defines how the outputs of T8 and T16 are combined (AND, OR, NOR, NAND).

In demodulation mode, this field defines which edge needs to be detected by the edge detector.

Transmit_Submode/Glitch_Filter

In transmit mode, this field defines whether T8 and T16 are in the “Ping-Pong” mode or in independent normal operation mode. Setting this field to “Normal

In demodulation mode, when this bit is set to 0, T16 captures and reloads on detection of all the edges. When this bit is set to 1, T16 captures and detects on the first edge but ignores the subsequent edges. For details, see “T16 Demodulation Mode” on page 51.

Time_Out

This bit is set when T16 times out (terminal count reached). To reset this bit, a 1 must be written to this location.

T16_Clock

This bit defines the frequency of the input signal to Counter/Timer16.

Capture_INT_Mask

This bit is set to allow an interrupt when data is captured into LO16 and HI16.

Counter_INT_Mask

This bit is set to allow an interrupt when T16 times out.

P35_Out

This bit defines whether P35 is used as a normal output pin or T16 output.

Counter/Timer Functional Blocks

The following are the counter/timer functional blocks:

- Input circuit
- Eight-bit counter/timer circuits (page 44)
- Sixteen-bit counter/timer circuits (page 50)
- Output circuit (page 54)

Input Circuit

The edge detector monitors the input signal on P31 or P20. Based on CTR1 D5–D4, a pulse is generated at the Pos Edge or Neg Edge line when an edge is detected. Glitches in the input signal that have a width less than specified (CTR1 D3, D2) are filtered out (see Figure 31).

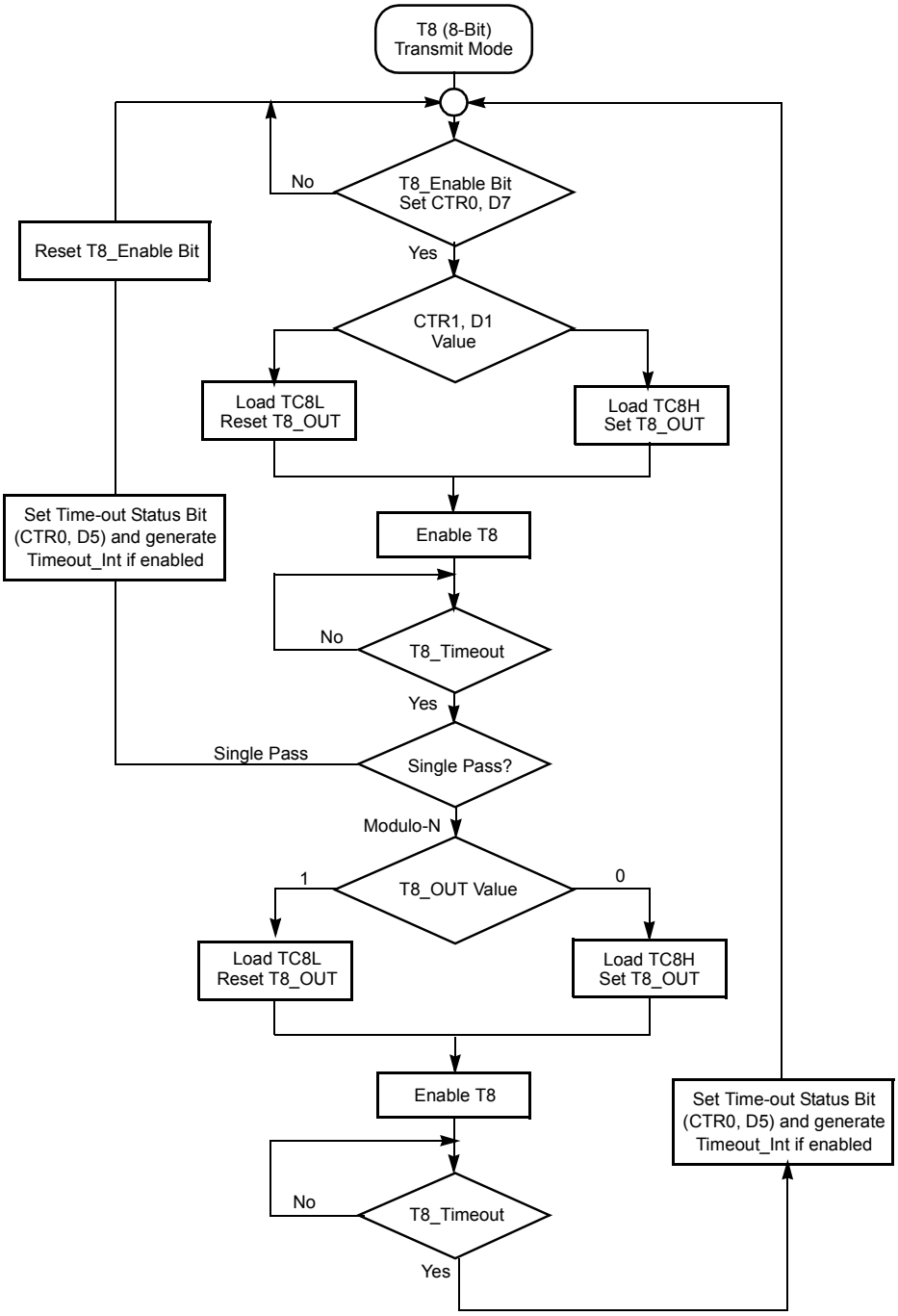


Figure 33. Transmit Mode Flowchart

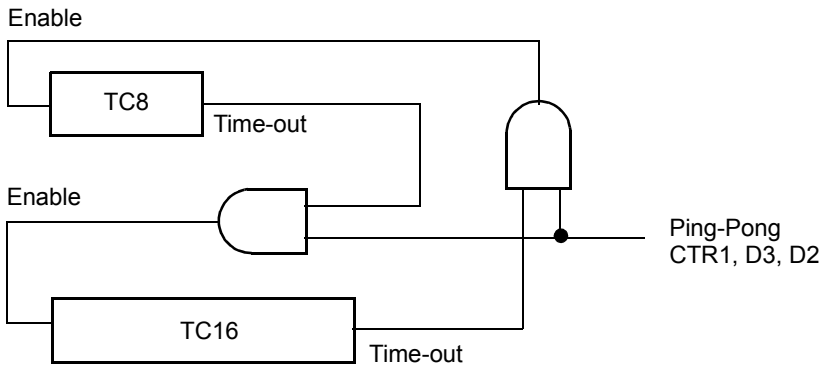


Figure 41. Ping-Pong Mode

Starting Ping-Pong Mode

First, make sure both counter/timers are not running. Then set T8 into Single-Pass Mode (CTR0 D6), set T16 into Single-Pass Mode (CTR2 D6), and set the Ping-Pong Mode (CTR1 D2, D3). These instructions do not have to be in any particular order. Finally, start Ping-Pong Mode by enabling either T8 (CTR0 D7) or T16 (CTR2 D7).

During Ping-Pong Mode

The enable bits of T8 and T16 (CTR0 D7, CTR2 D7) are set and cleared alternately by hardware. The time-out bits (CTR0 D5, CTR2 D5) are set every time the counter/timers reach the terminal count.

Output Circuit

Figure 42 shows the output circuit.

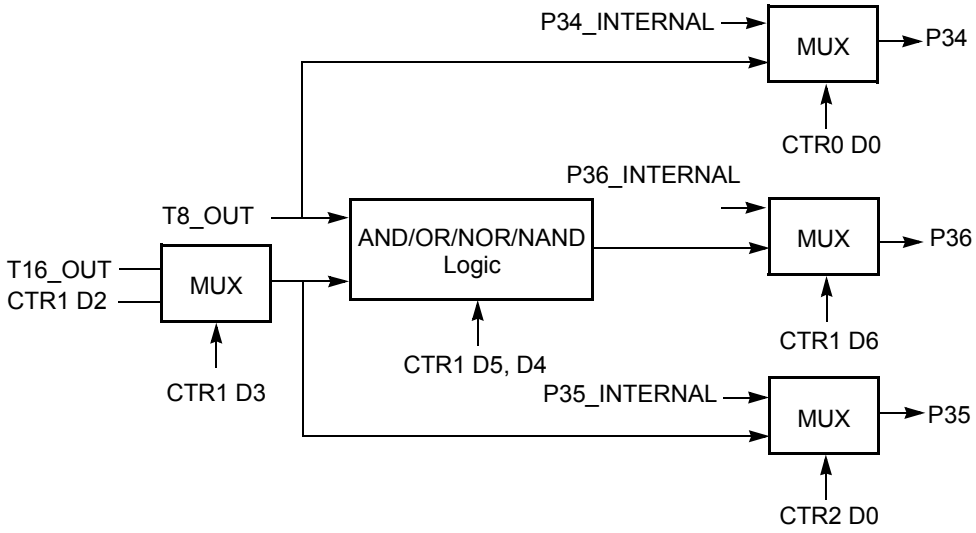


Figure 42. Output Circuit

Interrupts

The Z86L8X features five different interrupts. The interrupts are maskable and prioritized, as shown in Figure 43. The five sources are divided as follows: three sources are claimed by Port 3 lines P33–P31and two by the counter/timers (see Table 21). The Interrupt Mask Register, globally or individually, enables or disables the five interrupt requests.

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder controlled by the Interrupt Priority register. An interrupt machine cycle is activated when an interrupt request is granted. As a result, all subsequent interrupt are disabled, and the Program Counter and Status Flags are saved. The cycle then branches to the program memory vector location reserved for that interrupt. All Z86L8X interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request. To accommodate polled interrupt systems, interrupt inputs are masked, and the Interrupt Request register is polled to determine which of the interrupt requests require service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 can be rising, falling, or both edge triggered; all are programmable by the user. The software can poll to identify the state of the pin.

Programming bits for the Interrupt Edge Select are located in the IRQ Register (R250), bits D7 and D6. The configuration is indicated in Table 22.

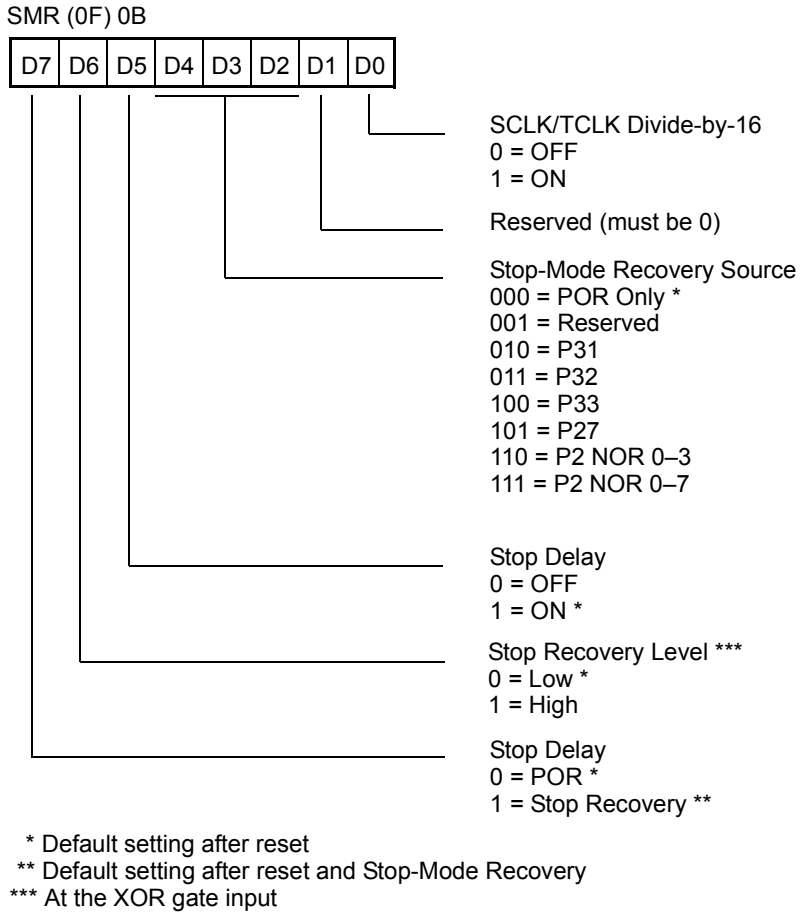
Table 22. IRQ Register *

IRQ		Interrupt Edge	
D7	**D6**	**IRQ2 (P31)**	**IRQ0 (P32)**
0	0	F	F
0	1	F	R
1	0	R	F
1	1	R/F	R/F

Notes:
F = Falling Edge
R = Rising Edge
*In stop mode, the comparators are turned off.

Clock

The Z86L8X on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, LC, ceramic resonator, or any suitable external clock source (XTAL1 = Input; XTAL2 = Output). The crystal must be AT cut, 1 MHz to 8 MHz maximum, with a series resistance (RS) less than or equal to 100 Ohms. The Z86LXX on-chip oscillator can be driven with a low-cost RC network or other suitable external clock source.



* Default setting after reset
** Default setting after reset and Stop-Mode Recovery
*** At the XOR gate input

Figure 46. Stop-Mode Recovery Register

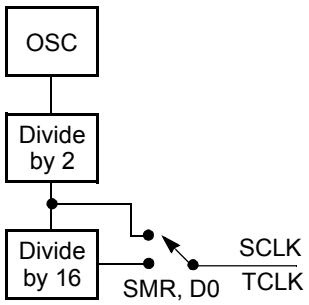


Figure 47. SCLK Circuit

SCLK/TCLK Divide-by-16 Select (D0)

D0 of the SMR controls a Divide-by-16 prescaler of SCLK/TCLK. The purpose of this control is to selectively reduce device power consumption during normal processor execution (SCLK control) and/or HALT Mode (where TCLK sources interrupt logic). After Stop-Mode Recovery, this bit is set to a 0.

Stop-Mode Recovery Source (D2, D3, and D4)

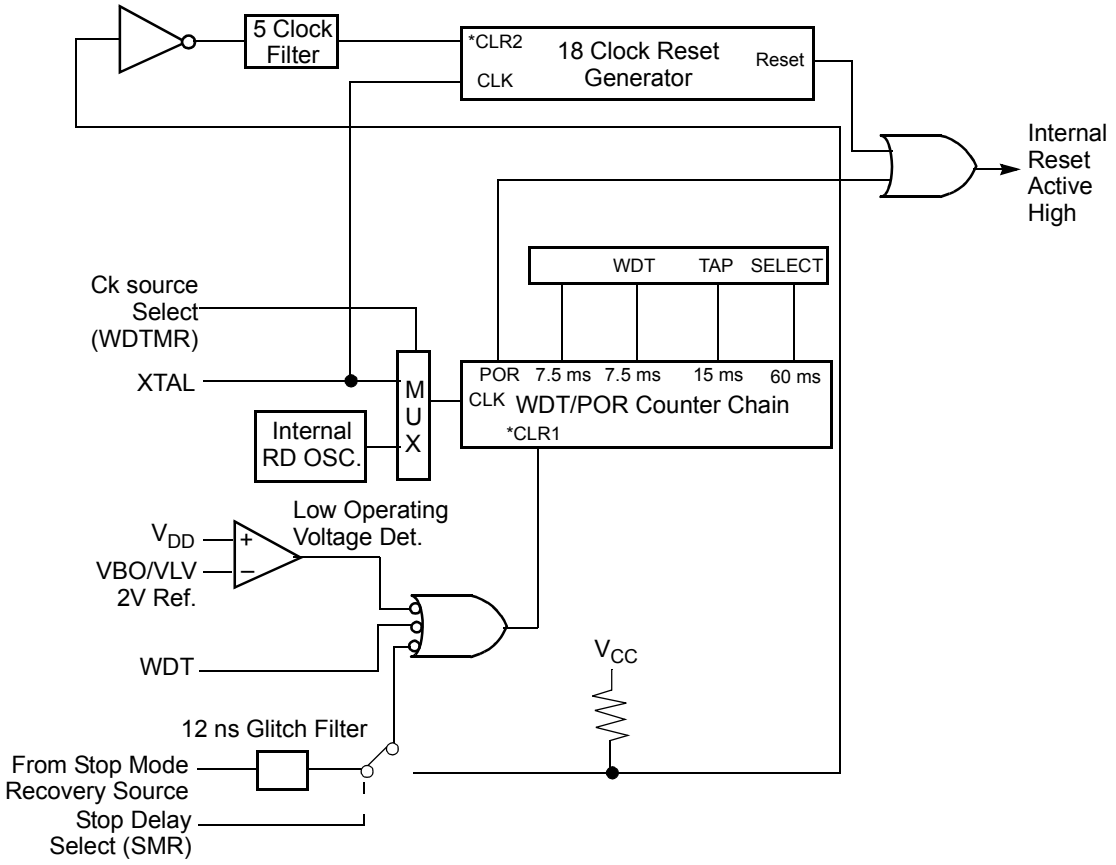
These three bits of the SMR specify the wake-up source of the STOP recovery (Figure 48 and Table 23 on page 63).

WDTMR During STOP (D3)

This bit determines whether or not the WDT is active during STOP Mode. Since the XTAL clock is stopped during STOP Mode, the on-board RC has to be selected as the clock source to the WDT/POR counter. A 1 indicates active during STOP. The default is 1.

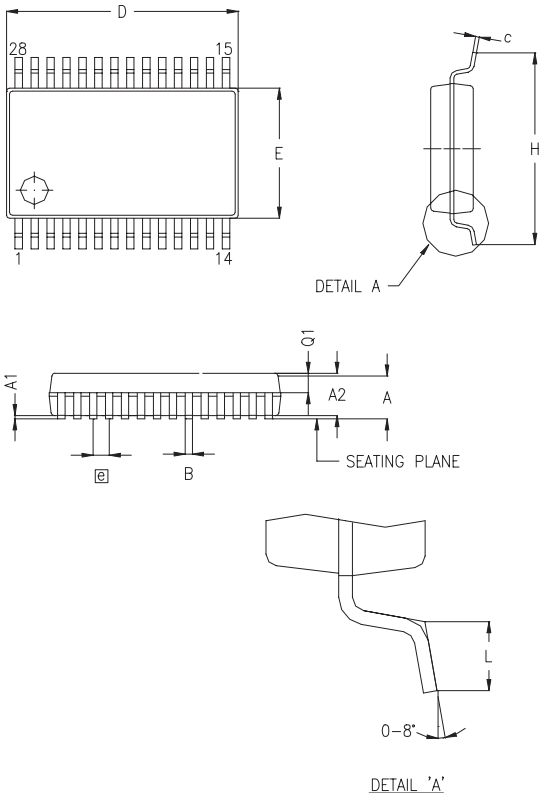
Clock Source for WDT (D4)

This bit determines which oscillator source is used to clock the internal POR and WDT counter chain. If the bit is a 1, the internal RC oscillator is bypassed, and the POR and WDT clock source is driven from the external pin, XTAL1. The default configuration of this bit is 0, which selects the RC oscillator. See Figure 51.



*$\overline{CLR1}$ and $\overline{CLR2}$ enable the WDT/POR and 18 Clock Reset timers upon a Low-to-High input translation.

Figure 51. Resets and WDT



SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.73	1.86	1.99	0.068	0.073	0.078
A1	0.05	0.13	0.21	0.002	0.005	0.008
A2	1.68	1.73	1.78	0.066	0.068	0.070
B	0.25		0.38	0.010		0.015
C	0.09	–	0.20	0.004	0.006	0.008
D	10.07	10.20	10.33	0.397	0.402	0.407
E	5.20	5.30	5.38	0.205	0.209	0.212
e	0.65 TYP			0.0256 TYP		
H	7.65	7.80	7.90	0.301	0.307	0.311
L	0.63	0.75	0.95	0.025	0.030	0.037

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Figure 54. 28-Pin SSOP Package Diagram

Z86L82/85/88

8.0 MHz 28-Pin DIP

Z86L8208PSC
Z86L8508PSC
Z86L8808PSC

28-Pin SOIC

Z86L8208SSC
Z86L8508SSC
Z86L8808SSC

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Provide a complete description of the problem or your suggestion. If you are reporting a specific problem, include all steps leading up to the occurrence of the problem. Attach additional pages as necessary.

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