Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

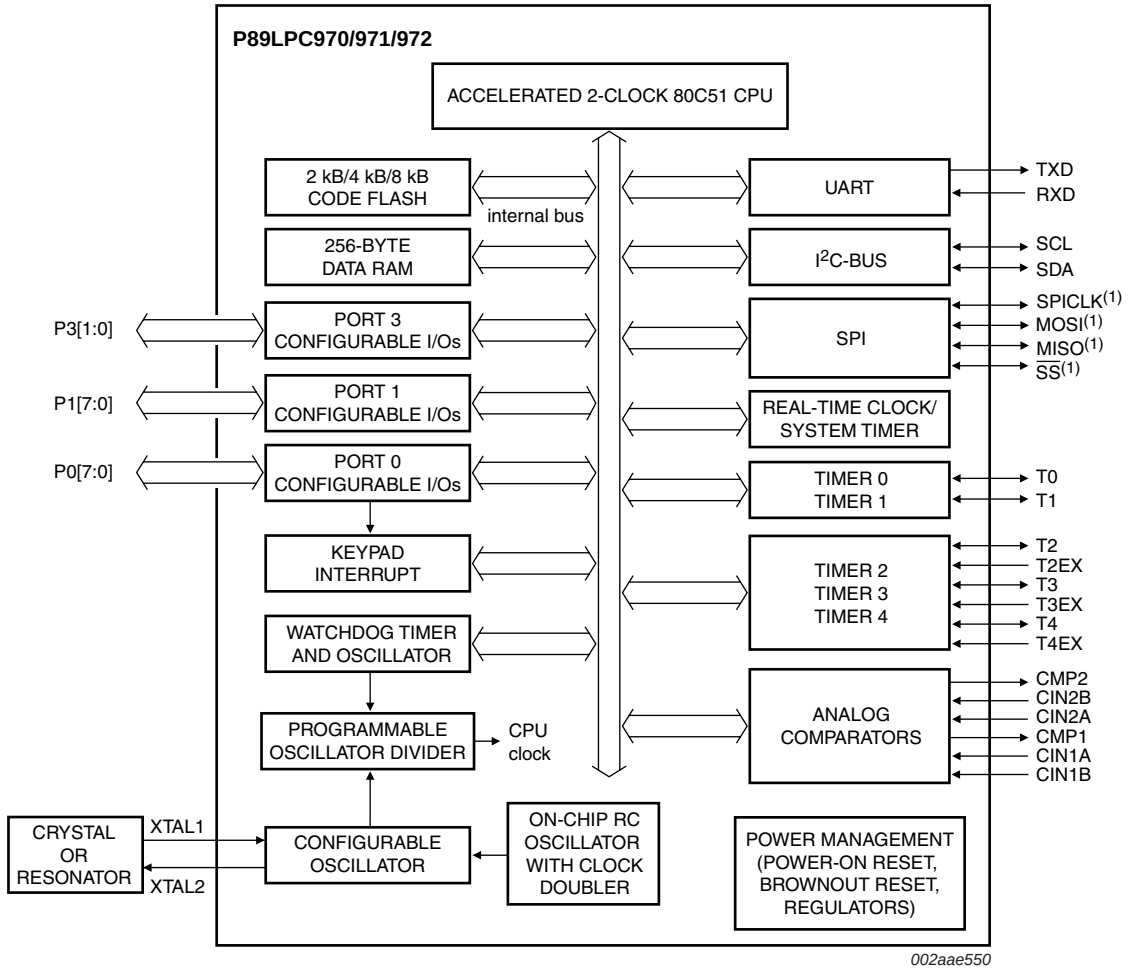
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	18MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	18
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89lpc971fdh-129

2.2 Additional features

- A high performance 80C51 CPU provides instruction cycle times of 111 ns to 222 ns for all instructions except multiply and divide when executing at 18 MHz. This is six times the performance of the standard 80C51 running at the same clock frequency. A lower clock frequency for the same performance results in power savings and reduced EMI.
- Serial flash In-Circuit Programming (ICP) allows simple production coding with commercial EPROM programmers. Flash security bits prevent reading of sensitive application programs.
- Serial flash In-System Programming (ISP) allows coding while the device is mounted in the end application.
- In-Application Programming (IAP) of the flash code memory. This allows changing the code in a running application.
- Clock switching on the fly among internal RC oscillator, watchdog oscillator, external clock source provides optimal support of minimal power active mode with fast switching to maximum performance.
- Idle and two different power-down reduced power modes. Improved wake-up from Power-down mode (a LOW interrupt input starts execution). Typical power-down current is 1 μA (total power-down with voltage comparators disabled).
- Integrated PMU (Power Management Unit) automatically adjusts internal regulators to minimize power consumption during Idle mode, Power-down mode and total Power-down mode. In addition, the power consumption can be further reduced in Normal or Idle mode through configuring regulators modes according to the applications.
- Active-LOW reset. On-chip power-on reset allows operation without external reset components. A software reset function is also available.
- Configurable on-chip oscillator with frequency range options selected by user programmed flash configuration bits. Oscillator options support frequencies from 20 kHz to the maximum operating frequency of 18 MHz.
- Oscillator fail detect. The watchdog timer has a separate fully on-chip oscillator allowing it to perform an oscillator fail detect function.
- Programmable port output configuration options: quasi-bidirectional, open drain, push-pull, input-only.
- High current sourcing/sinking (20 mA) on eight I/O pins (P0.3 to P0.7, P1.4, P1.6, P1.7). All other port pins have high sinking capability (20 mA). A maximum limit is specified for the entire chip.
- Port ‘input pattern match’ detect. Port 0 may generate an interrupt when the value of the pins match or do not match a programmable pattern.
- Controlled slew rate port outputs to reduce EMI. Outputs have approximately 10 ns minimum ramp times.
- Only power and ground connections are required to operate the P89LPC970/971/972 when internal reset option is selected.
- Four interrupt priority levels.
- Eight keypad interrupt inputs, plus two additional external interrupt inputs.
- Schmitt trigger port inputs.
- Second data pointer.
- Emulation support.

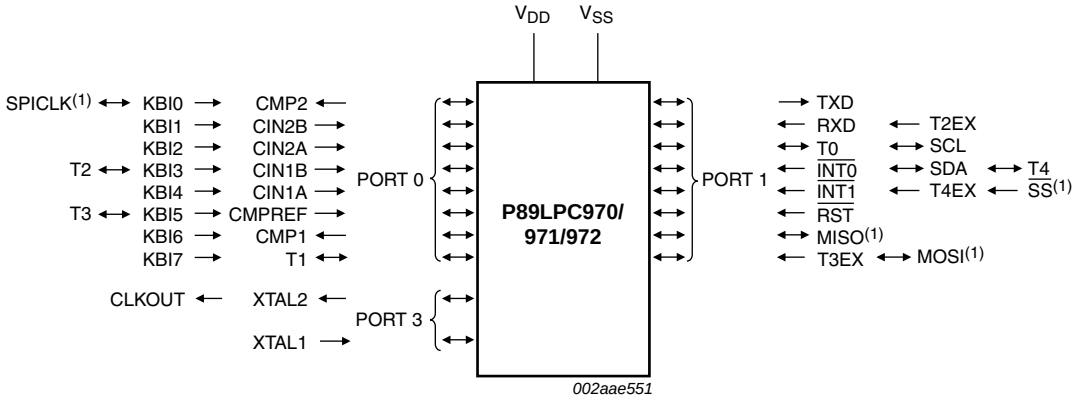
4. Block diagram



(1) For pin remap

Fig 1. Block diagram

5. Functional diagram



(1) For pin remap

Fig 2. Functional diagram

6. Pinning information

6.1 Pinning

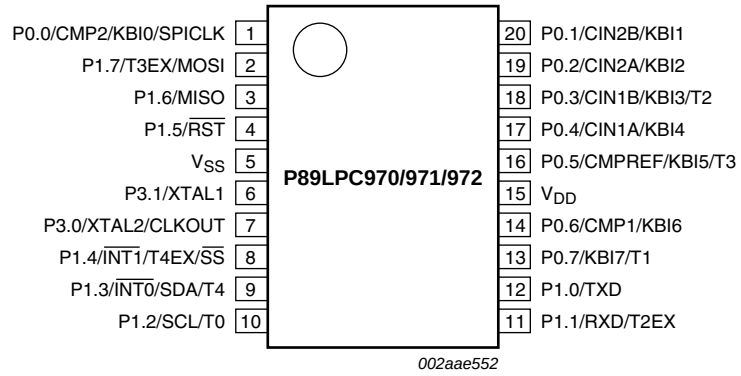


Fig 3. TSSOP20 pin configuration

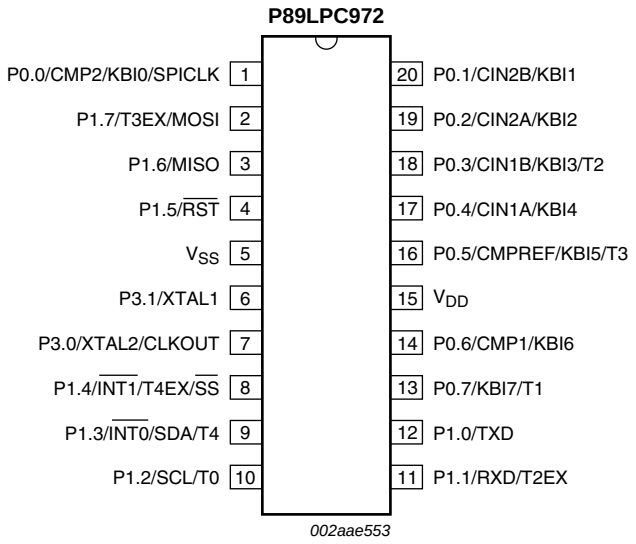


Fig 4. P89LPC972 DIP20 pin configuration

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
	DIP20, TSSOP20		
P0.0 to P0.7		I/O	**Port 0:** Port 0 is an 8-bit I/O port with a user-configurable output type. During reset Port 0 latches are configured in the input-only mode with the internal pull-up disabled. The operation of Port 0 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 7.16.1 “Port configurations” and Table 11 “Static characteristics” for details. The Keypad Interrupt feature operates with Port 0 pins. All pins have Schmitt trigger inputs. Port 0 also provides various special functions as described below:
P0.0/CMP2/KBI0/ SPICLK	1	I/O	**P0.0 —** Port 0 bit 0.
		O	**CMP2 —** Comparator 2 output
		I	**KBI0 —** Keyboard input 0.
		I/O	**SPICLK —** SPI clock. When configured as master, this pin is output; when configured as slave, this pin is input (pin remap).
P0.1/CIN2B/ KBI1	20	I/O	**P0.1 —** Port 0 bit 1.
		I	**CIN2B —** Comparator 2 positive input B.
		I	**KBI1 —** Keyboard input 1.
P0.2/CIN2A/ KBI2	19	I/O	**P0.2 —** Port 0 bit 2.
		I	**CIN2A —** Comparator 2 positive input A.
		I	**KBI2 —** Keyboard input 2.
P0.3/CIN1B/ KBI3/T2	18	I/O	**P0.3 —** Port 0 bit 3. High current source.
		I	**CIN1B —** Comparator 1 positive input B.
		I	**KBI3 —** Keyboard input 3.
		I/O	**T2 —** Timer/counter 2 external count input or overflow output.
P0.4/CIN1A/ KBI4	17	I/O	**P0.4 —** Port 0 bit 4. High current source.
		I	**CIN1A —** Comparator 1 positive input A.
		I	**KBI4 —** Keyboard input 4.
P0.5/CMPREF/ KBI5/T3	16	I/O	**P0.5 —** Port 0 bit 5. High current source.
		I	**CMPREF —** Comparator reference (negative) input.
		I	**KBI5 —** Keyboard input 5.
		I/O	**T3 —** Timer/counter 3 external count input or overflow output.

Table 3. Pin description *…continued*

Symbol	Pin	Type	Description
	DIP20, TSSOP20		
P1.7/T3EX/MOSI	2	I/O	**P1.7 —** Port 1 bit 7. High current source.
		I	**T3EX —** Timer/counter 3 external capture input.
		I/O	**MOSI —** SPI master out slave in. When configured as master, this pin is output; when configured as slave, this pin is input (pin remap).
P3.0 to P3.1		I/O	**Port 3:** Port 3 is a 2-bit I/O port with a user-configurable output type. During reset Port 3 latches are configured in the input-only mode with the internal pull-up disabled. The operation of Port 3 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 7.16.1 “Port configurations” and Table 11 “Static characteristics” for details. All pins have Schmitt trigger inputs. Port 3 also provides various special functions as described below:
P3.0/XTAL2/ CLKOUT	7	I/O	**P3.0 —** Port 3 bit 0.
		O	**XTAL2 —** Output from the oscillator amplifier (when a crystal oscillator option is selected via the flash configuration.
		O	**CLKOUT —** CPU clock divided by 2 when enabled via SFR bit (ENCLK -TRIM.6). It can be used if the CPU clock is the internal RC oscillator, watchdog oscillator or external clock input, except when XTAL1/XTAL2 are used to generate clock source for the RTC/system timer.
P3.1/XTAL1	6	I/O	**P3.1 —** Port 3 bit 1.
		I	**XTAL1 —** Input to the oscillator circuit and internal clock generator circuits (when selected via the flash configuration). It can be a port pin if internal RC oscillator or watchdog oscillator is used as the CPU clock source, **and** if XTAL1/XTAL2 are not used to generate the clock for the RTC/system timer.
V_{SS}	5	I	**Ground:** 0 V reference.
V_{DD}	15	I	**Power supply:** This is the power supply voltage for normal operation as well as Idle and Power-down modes.

[1] Input/output for P1.0 to P1.4, P1.6, P1.7. Input for P1.5.

Table 4. Special function registers *…continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
		Bit address	**FF**	**FE**	**FD**	**FC**	**FB**	**FA**	**F9**	**F8**		
IP1*	Interrupt priority 1	F8H	-	PST	-	PXTIM	PSPI	PC	PKBI	PI2C	00[2]	00x0 0000
IP1H	Interrupt priority 1 high	F7H	-	PSTH	-	PXTIMH	PSPIH	PCH	PKBIH	PI2CH	00[2]	00x0 0000
KBCON	Keypad control register	94H	-	-	-	-	-	-	PATN_SEL	KBIF	00[2]	xxxx xx00
KBMASK	Keypad interrupt mask register	86H									00	0000 0000
KBPATN	Keypad pattern register	93H									FF	1111 1111
		Bit address	**87**	**86**	**85**	**84**	**83**	**82**	**81**	**80**		
P0*	Port 0	80H	T1/KB7	CMP1/ KB6	CMPREF / KB5/T3	CIN1A/ KB4	CIN1B/ KB3/T2	CIN2A/ KB2	CIN2B/ KB1	CMP2/ KB0	[2]	
		Bit address	**97**	**96**	**95**	**94**	**93**	**92**	**91**	**90**		
P1*	Port 1	90H	T3EX	-	$\overline{\text{RST}}$	$\overline{\text{INT1}}$/ T4EX	$\overline{\text{INT0}}$/ SDA/T4	T0/SCL	RXD/ T2EX	TXD	[2]	
		Bit address	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**		
P3*	Port 3	B0H	-	-	-	-	-	-	XTAL1	XTAL2	[2]	
P0M1	Port 0 output mode 1	84H	(P0M1.7)	(P0M1.6)	(P0M1.5)	(P0M1.4)	(P0M1.3)	(P0M1.2)	(P0M1.1)	(P0M1.0)	FF[2]	1111 1111
P0M2	Port 0 output mode 2	85H	(P0M2.7)	(P0M2.6)	(P0M2.5)	(P0M2.4)	(P0M2.3)	(P0M2.2)	(P0M2.1)	(P0M2.0)	00[2]	0000 0000
P1M1	Port 1 output mode 1	91H	(P1M1.7)	(P1M1.6)	-	(P1M1.4)	(P1M1.3)	(P1M1.2)	(P1M1.1)	(P1M1.0)	D3[2]	11x1 xx11
P1M2	Port 1 output mode 2	92H	(P1M2.7)	(P1M2.6)	-	(P1M2.4)	(P1M2.3)	(P1M2.2)	(P1M2.1)	(P1M2.0)	00[2]	00x0 xx00
P3M1	Port 3 output mode 1	B1H	-	-	-	-	-	-	(P3M1.1)	(P3M1.0)	03[2]	xxxx xx11
P3M2	Port 3 output mode 2	B2H	-	-	-	-	-	-	(P3M2.1)	(P3M2.0)	00[2]	xxxx xx00

Table 8. SPI/I2C/UART pin remap

Peripherals	Function	Primary pin out	Alternative pin out
SPI	SPICLK	-	P0.0
	MOSI	-	P1.7
	MISO	-	P1.6
	$\overline{SS}$	-	P1.4
I2C	SDA	P1.3	-
	SCL	P1.2	-
UART	TXD	P1.0	-
	RXD	P1.1	-

7.17 Power management

The P89LPC970/971/972 support a variety of power management features.

Power-on detect and brownout detect are designed to prevent incorrect operation during initial power-up and power loss or reduction during operation.

The P89LPC970/971/972 support three different power reduction modes: Idle mode, Power-down mode, and total Power-down mode. In addition, individual on-chip peripherals can be disabled to eliminate unnecessary dynamic power use in any peripherals that are not required for the application.

Integrated PMU automatically adjusts internal regulators to minimize power consumption during Idle mode, Power-down mode and total Power-down mode. In addition, the power consumption can be further reduced in Normal or Idle mode through configuring regulators mode according to the applications.

7.17.1 Brownout detection

The brownout detect function determines if the power supply voltage drops below a certain level. Enhanced brownout detection has 3 independent functions: BOD reset, BOD interrupt and BOD flash.

These three functions are disabled in Power-down mode and Total Power-down mode. In Normal or Idle mode, BOD reset and BOD flash are always on and can not be disabled in software. BOD interrupt may be enabled or disabled in software.

BOD reset and BOD interrupt, each has 6 levels. BOE0 to BOE2 (UCFG1[3:5]) are used as trip point configuration bits of BOD reset. BOICFG0 to BOICFG2 in register BODCFG are used as trip point configuration bits of BOD interrupt.

BOD reset voltage should be lower than BOD interrupt trip point. BOD flash is used for flash programming/erase protection and has only 1 trip point at 2.4 V. Please refer to *P89LPC970/971/972 User manual* for detail configurations.

If brownout detection works, the brownout condition occurs when V_{DD} falls below the brownout falling trip voltage and is negated when V_{DD} rises above the brownout rising trip voltage.

For correct activation of brownout detect, the V_{DD} rise and fall times must be observed. Please see Table 11 “Static characteristics” for specifications.

7.18 Reset

The P1.5/$\overline{\text{RST}}$ pin can function as either a LOW-active reset input or as a digital input, P1.5. The Reset Pin Enable (RPE) bit in UCFG1, when set to logic 1, enables the external reset input function on P1.5. When cleared, P1.5 may be used as an input pin.

Remark: During a power-up sequence, the RPE selection is overridden and this pin always functions as a reset input. **An external circuit connected to this pin should not hold this pin LOW during a power-on sequence as this will keep the device in reset.** After power-up this pin will function as defined by the RPE bit. Only a power-up reset will temporarily override the selection defined by RPE bit. Other sources of reset will not override the RPE bit.

Reset can be triggered from the following sources:

- External reset pin (during power-up or if user configured via UCFG1)
- Power-on detect
- Brownout detect
- Watchdog timer
- Software reset
- UART break character detect reset

For every reset source, there is a flag in the Reset Register, RSTSRC. The user can read this register to determine the most recent reset source. These flag bits can be cleared in software by writing a logic 0 to the corresponding bit. More than one flag bit may be set:

- During a power-on reset, both POF and BOF are set but the other flag bits are cleared.
- A Watchdog reset is similar to a power-on reset, both POF and BOF are set but the other flag bits are cleared.
- For any other reset, previously set flag bits that have not been cleared will remain set.

7.18.1 Reset vector

Following reset, the P89LPC970/971/972 will fetch instructions from either address 0000H or the Boot address. The Boot address is formed by using the boot vector as the high byte of the address and the low byte of the address = 00H.

The boot address will be used if a UART break reset occurs, or the non-volatile boot status bit (BOOTSTAT.0) = 1, or the device is forced into ISP mode during power-on (see *P89LPC970/971/972 User manual*). Otherwise, instructions will be fetched from address 0000H.

7.19 Timers/counters 0 and 1

The P89LPC970/971/972 has two general purpose counter/timers which are upward compatible with the standard 80C51 Timer 0 and Timer 1. Both can be configured to operate either as timers or event counters. An option to automatically toggle the T0 or T1 pins upon timer overflow has been added.

In the ‘Timer’ function, the register is incremented every machine cycle.

In the ‘Counter’ function, the register is incremented in response to a 1-to-0 transition at its corresponding count input pin, T0 or T1. In this function, the count input is sampled once during every machine cycle.

Timer 0 and Timer 1 have five operating modes (Modes 0, 1, 2, 3 and 6). Modes 0, 1, 2 and 6 are the same for both Timers/Counters. Mode 3 is different.

7.19.1 Mode 0

Putting either Timer into Mode 0 makes it look like an 8048 Timer, which is an 8-bit Counter with a divide-by-32 prescaler. In this mode, the Timer register is configured as a 13-bit register. Mode 0 operation is the same for Timer 0 and Timer 1.

7.19.2 Mode 1

Mode 1 is the same as Mode 0, except that all 16 bits of the timer register are used.

7.19.3 Mode 2

Mode 2 configures the Timer register as an 8-bit Counter with automatic reload. Mode 2 operation is the same for Timer 0 and Timer 1.

7.19.3.1 Mode 3

When Timer 1 is in Mode 3 it is stopped. Timer 0 in Mode 3 forms two separate 8-bit counters and is provided for applications that require an extra 8-bit timer. When Timer 1 is in Mode 3 it can still be used by the serial port as a baud rate generator.

7.19.3.2 Mode 6

In this mode, the corresponding timer can be changed to a PWM with a full period of 256 timer clocks.

7.19.4 Timer overflow toggle output

Timers 0 and 1 can be configured to automatically toggle a port output whenever a timer overflow occurs. The same device pins that are used for the T0 and T1 count inputs are also used for the timer toggle outputs. The port outputs will be a logic 1 prior to the first timer overflow when this mode is turned on.

7.20 Timers/counters 2, 3 and 4

The P89LPC970/971/972 has three external 16-bit timer/counters. All can be configured to operate either as timers or event counters. An option to automatically toggle pin Tx (x = 2, 3 or 4) upon timer overflow has been added.

In the ‘Timer’ function, the register is incremented every PCLK.

In the ‘Counter’ function, the register is incremented in response to a 1-to-0 transition at its corresponding count input pin (T2/T3 /T4). In this function, the count input is sampled once during every machine cycle.

Only external Timer 2/3/4 has the external input pin TxEX (x = 2, 3 or 4). A 1-to-0 transition on this pin can trigger a reload or capture event.

Timer 2, Timer 3 and Timer 4 have three operating modes (Modes 0, 1 and 2).

7.22.7 Break detect

Break detect is reported in the status register (SSTAT). A break is detected when 11 consecutive bits are sensed LOW. The break detect can be used to reset the device and force the device into ISP mode.

7.22.8 Double buffering

The UART has a transmit double buffer that allows buffering of the next character to be written to SnBUF while the first character is being transmitted. Double buffering allows transmission of a string of characters with only one stop bit between any two characters, as long as the next character is written between the start bit and the stop bit of the previous character.

Double buffering can be disabled. If disabled (DBMOD, i.e., SSTAT.7 = 0), the UART is compatible with the conventional 80C51 UART. If enabled, the UART allows writing to SBUF while the previous data is being shifted out. Double buffering is only allowed in Modes 1, 2 and 3. When operated in Mode 0, double buffering must be disabled (DBMOD = 0).

7.22.9 Transmit interrupts with double buffering enabled (modes 1, 2 and 3)

Unlike the conventional UART, in double buffering mode, the TI interrupt is generated when the double buffer is ready to receive new data.

7.22.10 The 9th bit (bit 8) in double buffering (modes 1, 2 and 3)

If double buffering is disabled TB8 can be written before or after SBUF is written, as long as TB8 is updated some time before that bit is shifted out. TB8 must not be changed until the bit is shifted out, as indicated by the TI interrupt.

If double buffering is enabled, TB **must** be updated before SBUF is written, as TB8 will be double-buffered together with SBUF data.

7.23 I^{2}C-bus serial interface

The I^{2}C-bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus, and it has the following features:

- Bidirectional data transfer between masters and slaves
- Multi master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
- The I^{2}C-bus may be used for test and diagnostic purposes.

A typical I^{2}C-bus configuration is shown in Figure 8. The P89LPC970/971/972 device provides a byte-oriented I^{2}C-bus interface that supports data transfers up to 400 kHz.

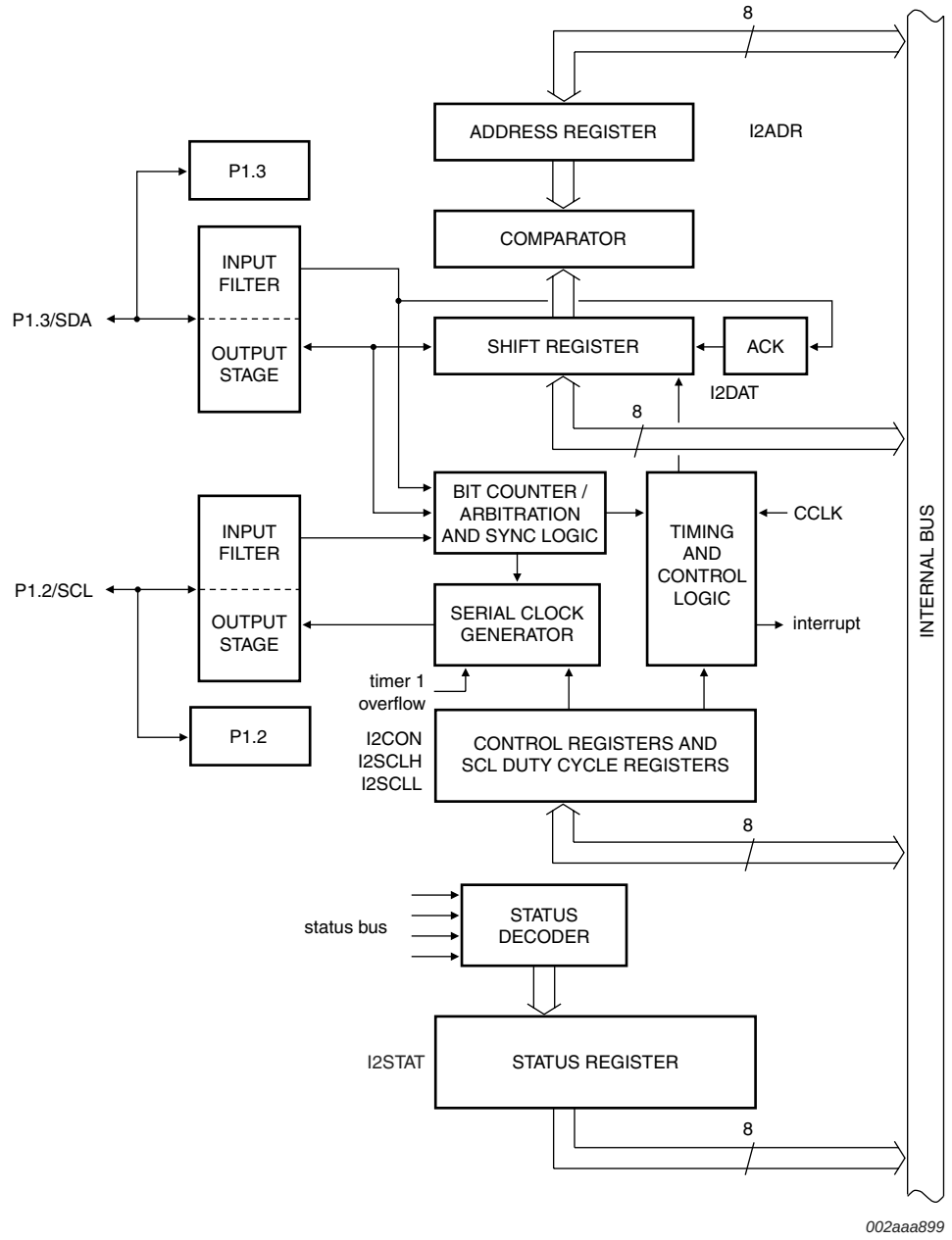
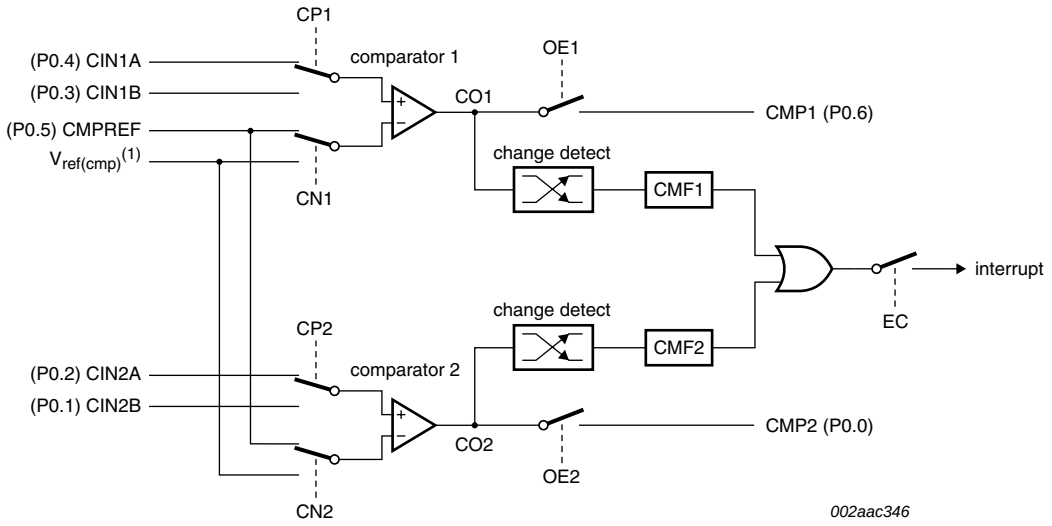


Fig 9. I²C-bus serial interface block diagram



(1) See Section 7.25.1 for more details.

Fig 14. Comparator input and output connections

7.25.1 Selectable internal reference voltage

An internal reference voltage generator may be used to supply a default reference when a single comparator input pin is used. The user may program one of eight different values for the internal reference voltage using the Comparator Reference register (CMPREF). Each of the two comparators may use a different reference voltage.

7.25.2 Comparator interrupt

Each comparator has an interrupt flag contained in its configuration register. This flag is set whenever the comparator output changes state. The flag may be polled by software or may be used to generate an interrupt. The two comparators use one common interrupt vector. If both comparators enable interrupts, after entering the interrupt service routine, the user needs to read the flags to determine which comparator caused the interrupt.

7.25.3 Comparators and power reduction modes

Either or both comparators may remain enabled when Power-down or Idle mode is activated, but both comparators are disabled automatically in Total Power-down mode.

If a comparator interrupt is enabled (except in Total Power-down mode), a change of the comparator output state will generate an interrupt and wake-up the processor. If the comparator output to a pin is enabled, the pin should be configured in the push-pull mode in order to obtain fast switching times while in Power-down mode. The reason is that with the **oscillator** stopped, the temporary strong pull-up that normally occurs during switching on a quasi-bidirectional port pin does not take place.

Comparators consume power in Power-down and Idle modes, as well as in the normal operating mode. This fact should be taken into account when system power consumption is an issue. To minimize power consumption, the user can disable the comparators via PCONA.5, or put the device in Total Power-down mode.

9. Static characteristics

Table 11. Static characteristics

V_{DD} = 2.4 V to 5.5 V unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$I_{DD(oper)}$	operating supply current	V_{DD} = 2.4 V					
		f_{osc} = 12 MHz, High-speed mode of regulators	[2]	-	6	7	mA
		f_{osc} = 12 MHz, Low current mode of regulators	[2]	-	5	6	mA
		V_{DD} = 3.3 V					
		f_{osc} = 12 MHz, High-speed mode of regulators	[2]	-	9	10	mA
		f_{osc} = 12 MHz, Low current mode of regulators	[2]	-	7	8	mA
		V_{DD} = 5.5 V					
		f_{osc} = 12 MHz, High-speed mode of regulators	[2]	-	10	11	mA
		f_{osc} = 12 MHz, Low current mode of regulators	[2]	-	8	9	mA
		f_{osc} = 18 MHz, High-speed mode of regulators	[2]	-	11	12	mA
$I_{DD(idle)}$	Idle mode supply current	V_{DD} = 2.4 V					
		f_{osc} = 12 MHz, High-speed mode of regulators	[2]	-	3.5	4.5	mA
		f_{osc} = 12 MHz, Low current mode of regulators	[2]	-	3	4	mA
		V_{DD} = 3.3 V					
		f_{osc} = 12 MHz, High-speed mode of regulators	[2]	-	5	6	mA
		f_{osc} = 12 MHz, Low current mode of regulators	[2]	-	4	5	mA
		V_{DD} = 5.5 V					
		f_{osc} = 12 MHz, High-speed mode of regulators	[2]	-	6	7	mA
		f_{osc} = 12 MHz, Low current mode of regulators	[2]	-	4	5	mA
		f_{osc} = 18 MHz, High-speed mode of regulators	[2]	-	6.5	7.5	mA
$I_{DD(pd)}$	Power-down mode supply current	V_{DD} = 2.4 V; voltage comparators powered down	[3]	-	28	35	μA
		V_{DD} = 3.3 V; voltage comparators powered down	[3]	-	32	40	μA
		V_{DD} = 5.5 V; voltage comparators powered down	[3]	-	38	45	μA

Table 11. Static characteristics *…continued*
V_{DD} = 2.4 V to 5.5 V unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
BOD reset						
V_{trip}	trip voltage	falling stage				
		BOE2, BOE1, BOE0 = 010	2.15	-	2.35	V
		BOE2, BOE1, BOE0 = 011	2.45	-	2.65	V
		BOE2, BOE1, BOE0 = 100	2.75	-	2.95	V
		BOE2, BOE1, BOE0 = 101	3.05	-	3.25	V
		BOE2, BOE1, BOE0 = 110	3.75	-	3.95	V
		BOE2, BOE1, BOE0 = 111	3.95	-	4.15	V
		rising stage				
		BOE2, BOE1, BOE0 = 010	2.30	-	2.50	V
		BOE2, BOE1, BOE0 = 011	2.60	-	2.80	V
		BOE2, BOE1, BOE0 = 100	2.90	-	3.10	V
		BOE2, BOE1, BOE0 = 101	3.20	-	3.40	V
		BOE2, BOE1, BOE0 = 110	3.85	-	4.05	V
		BOE2, BOE1, BOE0 = 111	4.05	-	4.25	V
BOD flash						
V_{trip}	trip voltage	falling stage	2.30	-	2.55	V
		rising stage	2.40	-	2.65	V
$V_{ref(bg)}$	band gap reference voltage		1.19	1.23	1.27	V
TC_{bg}	band gap temperature coefficient		-	10	20	ppm/°C

[1] Typical ratings are not guaranteed. The values listed are at room temperature, 3 V.

[2] The $I_{DD(oper)}$ and $I_{DD(idle)}$ specifications are measured using an external clock with the following functions disabled: comparators, real-time clock, and watchdog timer.

[3] The $I_{DD(pd)}$ and $I_{DD(tpd)}$ specification is measured using an external clock with the following functions disabled: comparators, real-time clock, brownout detect, and watchdog timer.

[4] See Section 8 “Limiting values” for steady state (non-transient) limits on I_{OL} or I_{OH}. If I_{OL}/I_{OH} exceeds the test condition, V_{OL}/V_{OH} may exceed the related specification.

[5] This specification can be applied to pins which have A/D input or analog comparator input functions when the pin is not being used for those analog functions. When the pin is being used as an analog input pin, the maximum voltage on the pin must be limited to 4.0 V with respect to V_{SS}.

[6] Pin capacitance is characterized but not tested.

[7] Measured with port in quasi-bidirectional mode.

[8] Measured with port in high-impedance mode.

[9] Port pins source a transition current when used in quasi-bidirectional mode and externally driven from logic 1 to logic 0. This current is highest when V_I is approximately 2 V.

Table 12. Dynamic characteristics (12 MHz) *…continued*

V_{DD} = 2.4 V to 5.5 V unless otherwise specified.

T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.[1][2]

Symbol	Parameter	Conditions	Variable clock		f_{osc} = 12 MHz		Unit
			Min	Max	Min	Max	
T_{SPICYC}	SPI cycle time	see Figure 19, 20, 21, 22					
	slave		$^{6}/_{CCLK}$	-	500	-	ns
	master		$^{4}/_{CCLK}$	-	333	-	ns
$t_{SPILEAD}$	SPI enable lead time	see Figure 21, 22					
	slave		250	-	250	-	ns
t_{SPILAG}	SPI enable lag time	see Figure 21, 22					
	slave		250	-	250	-	ns
$t_{SPICLKH}$	SPICLK HIGH time	see Figure 19, 20, 21, 22					
	master		$^{2}/_{CCLK}$	-	165	-	ns
	slave		$^{3}/_{CCLK}$	-	250	-	ns
$t_{SPICLKL}$	SPICLK LOW time	see Figure 19, 20, 21, 22					
	master		$^{2}/_{CCLK}$	-	165	-	ns
	slave		$^{3}/_{CCLK}$	-	250	-	ns
t_{SPIDSU}	SPI data set-up time	see Figure 19, 20, 21, 22					
	master or slave		100	-	100	-	ns
t_{SPIDH}	SPI data hold time	see Figure 19, 20, 21, 22					
	master or slave		100	-	100	-	ns
t_{SPIA}	SPI access time	see Figure 21, 22					
	slave		0	120	0	120	ns
t_{SPIDIS}	SPI disable time	see Figure 21, 22					
	slave		0	240	-	240	ns
t_{SPIDV}	SPI enable to output data valid time	see Figure 19, 20, 21, 22					
	slave		-	240	-	240	ns
	master		-	167	-	167	ns
t_{SPIOH}	SPI output data hold time	see Figure 19, 20, 21, 22	0	-	0	-	ns
t_{SPIR}	SPI rise time	see Figure 19, 20, 21, 22					
	SPI outputs (SPICLK, MOSI, MISO)		-	100	-	100	ns
	SPI inputs (SPICLK, MOSI, MISO, $\overline{SS}$)		-	2000	-	2000	ns
t_{SPIF}	SPI fall time	see Figure 19, 20, 21, 22					
	SPI outputs (SPICLK, MOSI, MISO)		-	100	-	100	ns
	SPI inputs (SPICLK, MOSI, MISO, $\overline{SS}$)		-	2000	-	2000	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Parts are tested to 2 MHz, but are guaranteed to operate down to 0 Hz.

Table 13. Dynamic characteristics (18 MHz)

V_{DD} = 3.6 V to 5.5 V unless otherwise specified.

T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.[1][2]

Symbol	Parameter	Conditions	Variable clock		f_{osc} = 18 MHz		Unit
			Min	Max	Min	Max	
$f_{osc(RC)}$	internal RC oscillator frequency	nominal f = 7.3728 MHz trimmed to ±1 % at T_{amb} = 25 °C; clock doubler option = OFF (default)	7.189	7.557	7.189	7.557	MHz
		nominal f = 14.7456 MHz; clock doubler option = ON	14.378	15.114	14.378	15.114	MHz
$f_{osc(WD)}$	internal watchdog oscillator frequency		360	440	360	440	kHz
f_{osc}	oscillator frequency		0	18	-	-	MHz
$T_{cy(clk)}$	clock cycle time	see Figure 17	55	-	-	-	ns
f_{CLKLP}	low-power select clock frequency		0	8	-	-	MHz
Glitch filter							
t_{gr}	glitch rejection time	P1.5/$\overline{RST}$ pin	-	50	-	50	ns
		any pin except P1.5/$\overline{RST}$	-	15	-	15	ns
t_{sa}	signal acceptance time	P1.5/$\overline{RST}$ pin	125	-	125	-	ns
		any pin except P1.5/$\overline{RST}$	50	-	50	-	ns
External clock							
t_{CHCX}	clock HIGH time	see Figure 17	22	$T_{cy(clk)} - t_{CLCX}$	22	-	ns
t_{CLCX}	clock LOW time	see Figure 17	22	$T_{cy(clk)} - t_{CHCX}$	22	-	ns
t_{CLCH}	clock rise time	see Figure 17	-	5	-	5	ns
t_{CHCL}	clock fall time	see Figure 17	-	5	-	5	ns
Shift register (UART mode 0)							
T_{XLXL}	serial port clock cycle time	see Figure 18	$16T_{cy(clk)}$	-	888	-	ns
t_{QVXH}	output data set-up to clock rising edge time	see Figure 18	$13T_{cy(clk)}$	-	722	-	ns
t_{XHQX}	output data hold after clock rising edge time	see Figure 18	-	$T_{cy(clk)}$ + 20	-	75	ns
t_{XHDX}	input data hold after clock rising edge time	see Figure 18	-	0	-	0	ns
t_{XHDV}	input data valid to clock rising edge time	see Figure 18	150	-	150	-	ns
SPI interface							
f_{SPI}	SPI operating frequency						
	slave		0	$^{CCLK}/_{6}$	0	3.0	MHz
	master		-	$^{CCLK}/_{4}$	-	4.5	MHz
T_{SPICYC}	SPI cycle time	see Figure 19, 20, 21, 22					
	slave		$^{6}/_{CCLK}$	-	333	-	ns
	master		$^{4}/_{CCLK}$	-	222	-	ns

Table 13. Dynamic characteristics (18 MHz) *…continued*
V_{DD} = 3.6 V to 5.5 V unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.[1][2]

Symbol	Parameter	Conditions	Variable clock		f_{osc} = 18 MHz		Unit
			Min	Max	Min	Max	
$t_{SPILEAD}$	SPI enable lead time	see Figure 21, 22					
	slave		250	-	250	-	ns
t_{SPILAG}	SPI enable lag time	see Figure 21, 22					
	slave		250	-	250	-	ns
$t_{SPICLKH}$	SPICLK HIGH time	see Figure 19, 20, 21, 22					
	slave		$^{3}/_{CCLK}$	-	167	-	ns
	master		$^{2}/_{CCLK}$	-	111	-	ns
$t_{SPICLKL}$	SPICLK LOW time	see Figure 19, 20, 21, 22					
	slave		$^{3}/_{CCLK}$	-	167	-	ns
	master		$^{2}/_{CCLK}$	-	111	-	ns
t_{SPIDSU}	SPI data set-up time	see Figure 19, 20, 21, 22					
	master or slave		100	-	100	-	ns
t_{SPIDH}	SPI data hold time	see Figure 19, 20, 21, 22					
	master or slave		100	-	100	-	ns
t_{SPIA}	SPI access time	see Figure 21, 22					
	slave		0	80	0	80	ns
t_{SPIDIS}	SPI disable time	see Figure 21, 22					
	slave		0	160	-	160	ns
t_{SPIDV}	SPI enable to output data valid time	see Figure 19, 20, 21, 22					
	slave		-	160	-	160	ns
	master		-	111	-	111	ns
t_{SPIOH}	SPI output data hold time	see Figure 19, 20, 21, 22	0	-	0	-	ns
t_{SPIR}	SPI rise time	see Figure 19, 20, 21, 22					
	SPI outputs (SPICLK, MOSI, MISO)		-	100	-	100	ns
	SPI inputs (SPICLK, MOSI, MISO, $\overline{SS}$)		-	2000	-	2000	ns
t_{SPIF}	SPI fall time	see Figure 19, 20, 21, 22					
	SPI outputs (SPICLK, MOSI, MISO)		-	100	-	100	ns
	SPI inputs (SPICLK, MOSI, MISO, $\overline{SS}$)		-	2000	-	2000	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Parts are tested to 2 MHz, but are guaranteed to operate down to 0 Hz.

10.1 Waveforms

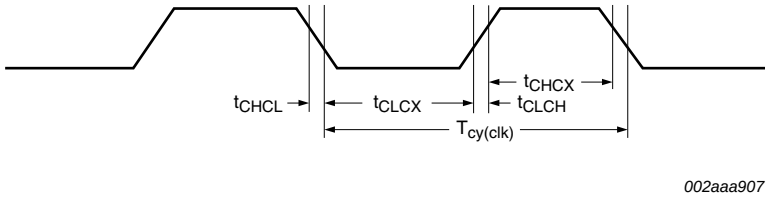


Fig 17. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

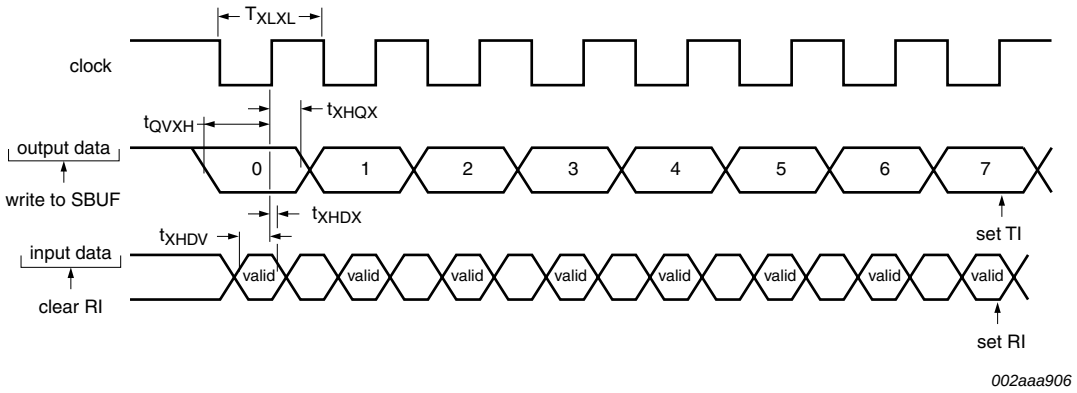


Fig 18. Shift register mode timing

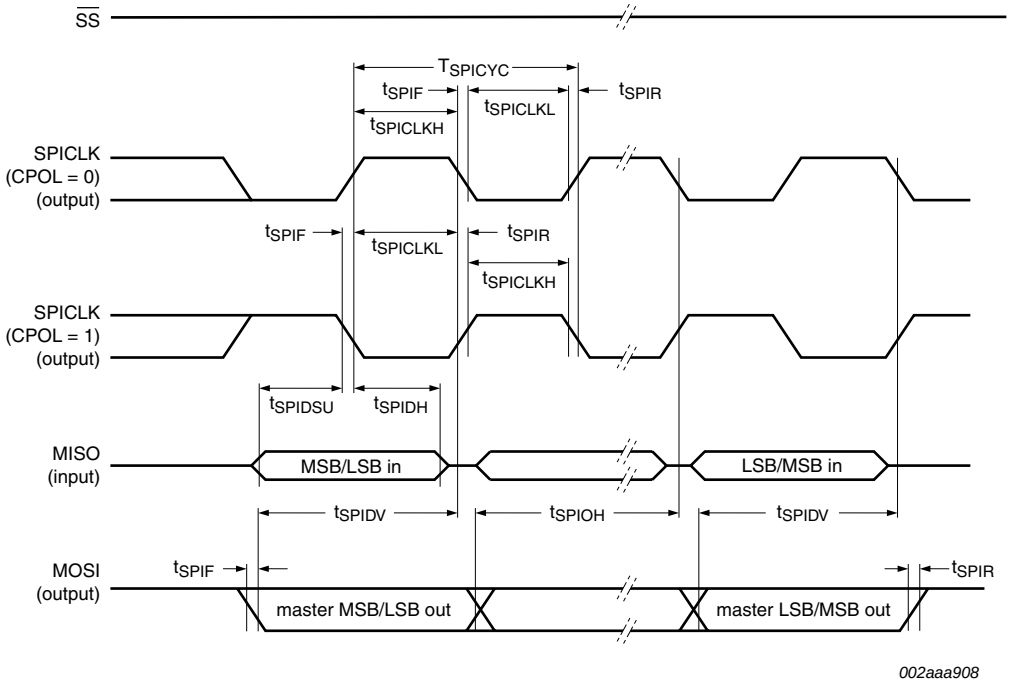


Fig 19. SPI master timing (CPHA = 0)

17. Contents

continued >>