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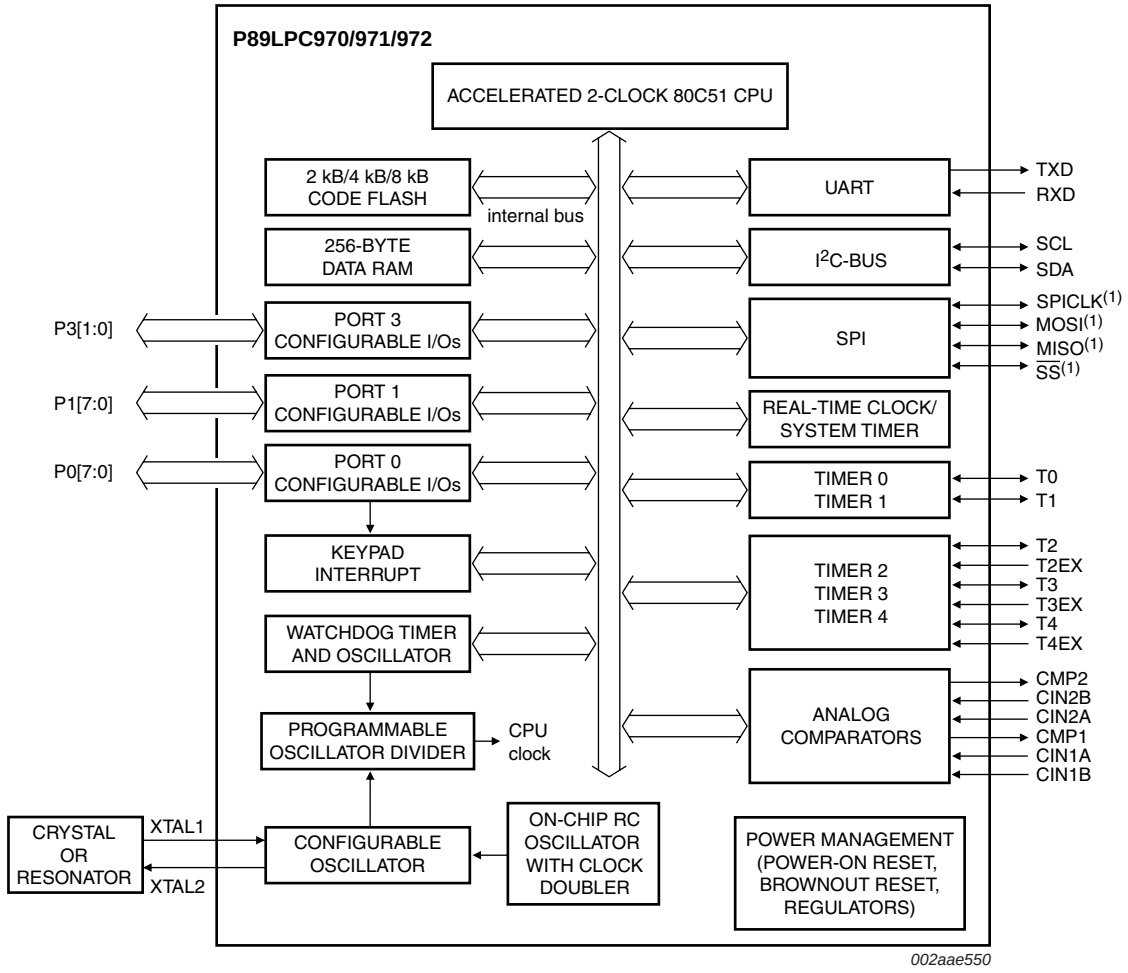
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	18MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	18
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89lpc972fdh-129

4. Block diagram



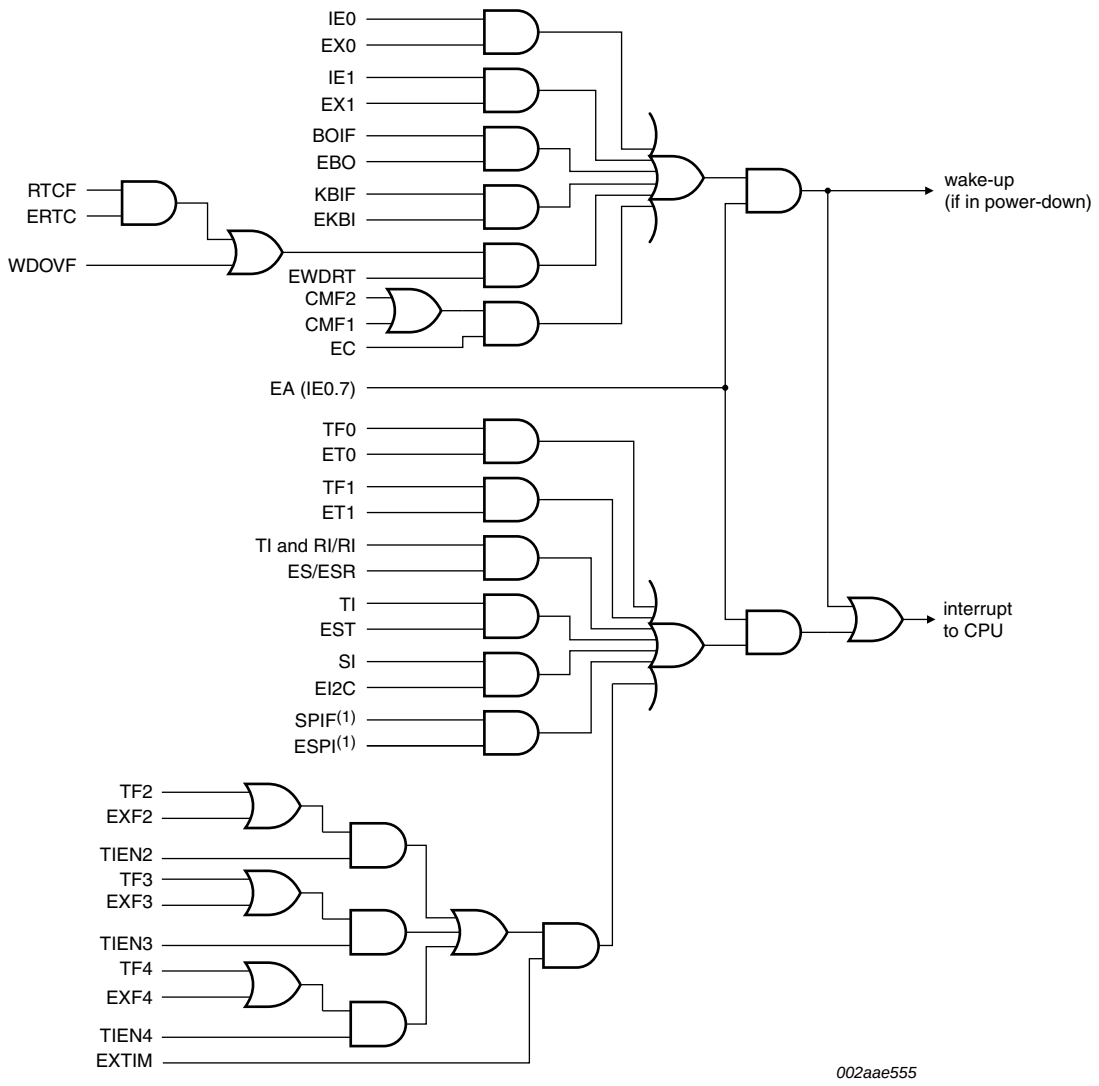
(1) For pin remap

Fig 1. Block diagram

Table 4. Special function registers *…continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
FMCON	Program flash control (Read)	E4H	BUSY	-	-	-	HVA	HVE	SV	OI	70	0111 0000
	Program flash control (Write)	E4H	FMCMD.7	FMCMD.6	FMCMD.5	FMCMD.4	FMCMD.3	FMCMD.2	FMCMD.1	FMCMD.0		
FMDATA	Program flash data	E5H									00	0000 0000
I2ADR	I^2C-bus slave address register	DBH	I2ADR.6	I2ADR.5	I2ADR.4	I2ADR.3	I2ADR.2	I2ADR.1	I2ADR.0	GC	00	0000 0000
		Bit address	**DF**	**DE**	**DD**	**DC**	**DB**	**DA**	**D9**	**D8**		
I2CON*	I^2C-bus control register	D8H	-	I2EN	STA	STO	SI	AA	-	CRSEL	00	x000 00x0
I2DAT	I^2C-bus data register	DAH										
I2SCLH	Serial clock generator/SCL duty cycle register high	DDH									00	0000 0000
I2SCLL	Serial clock generator/SCL duty cycle register low	DCH									00	0000 0000
I2STAT	I^2C-bus status register	D9H	STA.4	STA.3	STA.2	STA.1	STA.0	0	0	0	F8	1111 1000
		Bit address	**AF**	**AE**	**AD**	**AC**	**AB**	**AA**	**A9**	**A8**		
IEN0*	Interrupt enable 0	A8H	EA	EWDRT	EBO	ES/ESR	ET1	EX1	ET0	EX0	00	0000 0000
		Bit address	**EF**	**EE**	**ED**	**EC**	**EB**	**EA**	**E9**	**E8**		
IEN1*	Interrupt enable 1	E8H	-	EST	-	EXTIM	ESPI	EC	EKBI	EI2C	00[2]	00x0 0000
		Bit address	**BF**	**BE**	**BD**	**BC**	**BB**	**BA**	**B9**	**B8**		
IP0*	Interrupt priority 0	B8H	-	PWDRT	PBO	PS/PSR	PT1	PX1	PT0	PX0	00[2]	x000 0000
IP0H	Interrupt priority 0 high	B7H	-	PWDRTH	PBOH	PSH/PSRH	PT1H	PX1H	PT0H	PX0H	00[2]	x000 0000



(1) For pin remap.

Fig 6. Interrupt sources, interrupt enables, and power-down wake-up sources

7.16.1.3 Input-only configuration

The input-only port configuration has no output drivers. It is a Schmitt trigger input that also has a glitch suppression circuit.

7.16.1.4 Push-pull output configuration

The push-pull output configuration has the same pull-down structure as both the open-drain and the quasi-bidirectional output modes, but provides a continuous strong pull-up when the port latch contains a logic 1. The push-pull mode may be used when more source current is needed from a port output. A push-pull port pin has a Schmitt triggered input that also has a glitch suppression circuit. The P89LPC970/971/972 device has high current source on eight pins in push-pull mode. See Table 10 “Limiting values”.

7.16.2 Port 0 analog functions

The P89LPC970/971/972 incorporates two Analog Comparators. In order to give the best analog function performance and to minimize power consumption, pins that are being used for analog functions must have the digital outputs and digital inputs disabled.

Digital outputs are disabled by putting the port output into the input-only (high-impedance) mode.

Digital inputs on Port 0 may be disabled through the use of the PT0AD register, bits 1:5. On any reset, PT0AD[1:5] defaults to logic 0s to enable digital functions.

7.16.3 Additional port features

After power-up, all pins are in input-only mode. **Please note that this is different from the LPC76x series of devices.**

- After power-up, all I/O pins except P1.5, may be configured by software.
- Pin P1.5 is input only. Pins P1.2 and P1.3 are configurable for either input-only or open-drain.

Every output on the P89LPC970/971/972 has been designed to sink typical LED drive current. However, there is a maximum total output current for all ports which must not be exceeded. Please refer to Table 11 “Static characteristics” for detailed specifications.

All ports pins that can function as an output have slew rate controlled outputs to limit noise generated by quickly switching output signals. The slew rate is factory-set to approximately 10 ns rise and fall times.

7.16.4 Pin remap

This feature allows the functions of UART/I2C/SPI to be remapped to other pins. Configuration register controls the multiplexers to allow connection between the pins and the on chip peripherals. See Table 8 “SPI/I2C/UART pin remap”.

UART/I2C/SPI, each has two options of pin configuration: primary pin map and alternative pin map. After reset, UART/I2C/SPI chooses the primary pin map as default. User can adjust to the alternative pin map through configuring PINCON register according to the application.

Please refer to *P89LPC970/971/972 User manual* for detail configurations.

7.17.2 Power-on detection

The Power-on detect has a function similar to the brownout detect, but is designed to work as power comes up initially to ensure that the device is reset from Power-on. The POF flag in the RSTSRC register is set to indicate an initial power-up condition. The POF flag will remain set until cleared by software.

7.17.3 Power reduction modes

The P89LPC970/971/972 supports three different power reduction modes. These modes are Idle mode, Power-down mode, and total Power-down mode.

7.17.3.1 Idle mode

Idle mode leaves peripherals running in order to allow them to activate the processor

when an interrupt is generated. Any enabled interrupt source or reset may terminate Idle mode.

7.17.3.2 Power-down mode

The Power-down mode stops the oscillator in order to minimize power consumption. Brownout detection circuitry is disabled. The P89LPC970/971/972 exits Power-down mode via any reset, or certain interrupts.

Some chip functions continue to operate and draw power during Power-down mode, increasing the total power used during power-down. These include: Brownout detect, watchdog timer, comparators and RTC/system timer (note that watchdog timer, comparators and RTC/system timer can be powered down separately). The internal RC oscillator is disabled unless both the RC oscillator has been selected as the system clock and the RTC is enabled.

7.17.3.3 Total Power-down mode

The total Power-down mode is a deeper power reduction mode. Brownout detection circuitry and analog comparators are disabled, as well as the internal RC oscillator.

Please use an external low frequency clock or 25 kHz watchdog oscillator to achieve low power with the RTC running during power-down.

7.17.4 Regulators

Internal regulators can be adjusted automatically to minimize power consumption during different power reduction modes. In Normal or Idle modes, power consumption can be further reduced by configuring PMUCON register.

In Normal or Idle mode, regulators have two operation modes: High-speed mode and Low current mode.

The regulators can be configured to Low current mode to reduce the power consumption.

After power-on-reset, internal regulators enter into High-speed mode as default. PMUCON register is used to configure the regulators operation modes. LPMOD bit is used to select the regulator’s mode and HCOK bit indicates whether the switch completed or not. When switching back to high speed mode, first clear LPMOD bit to select high speed mode, then check HCOK bit. If HCOK bit turns to ‘1’, it means the switch was completed.

7.18 Reset

The P1.5/$\overline{\text{RST}}$ pin can function as either a LOW-active reset input or as a digital input, P1.5. The Reset Pin Enable (RPE) bit in UCFG1, when set to logic 1, enables the external reset input function on P1.5. When cleared, P1.5 may be used as an input pin.

Remark: During a power-up sequence, the RPE selection is overridden and this pin always functions as a reset input. **An external circuit connected to this pin should not hold this pin LOW during a power-on sequence as this will keep the device in reset.** After power-up this pin will function as defined by the RPE bit. Only a power-up reset will temporarily override the selection defined by RPE bit. Other sources of reset will not override the RPE bit.

Reset can be triggered from the following sources:

- External reset pin (during power-up or if user configured via UCFG1)
- Power-on detect
- Brownout detect
- Watchdog timer
- Software reset
- UART break character detect reset

For every reset source, there is a flag in the Reset Register, RSTSRC. The user can read this register to determine the most recent reset source. These flag bits can be cleared in software by writing a logic 0 to the corresponding bit. More than one flag bit may be set:

- During a power-on reset, both POF and BOF are set but the other flag bits are cleared.
- A Watchdog reset is similar to a power-on reset, both POF and BOF are set but the other flag bits are cleared.
- For any other reset, previously set flag bits that have not been cleared will remain set.

7.18.1 Reset vector

Following reset, the P89LPC970/971/972 will fetch instructions from either address 0000H or the Boot address. The Boot address is formed by using the boot vector as the high byte of the address and the low byte of the address = 00H.

The boot address will be used if a UART break reset occurs, or the non-volatile boot status bit (BOOTSTAT.0) = 1, or the device is forced into ISP mode during power-on (see *P89LPC970/971/972 User manual*). Otherwise, instructions will be fetched from address 0000H.

7.19 Timers/counters 0 and 1

The P89LPC970/971/972 has two general purpose counter/timers which are upward compatible with the standard 80C51 Timer 0 and Timer 1. Both can be configured to operate either as timers or event counters. An option to automatically toggle the T0 or T1 pins upon timer overflow has been added.

In the ‘Timer’ function, the register is incremented every machine cycle.

In the ‘Counter’ function, the register is incremented in response to a 1-to-0 transition at its corresponding count input pin, T0 or T1. In this function, the count input is sampled once during every machine cycle.

Timer 0 and Timer 1 have five operating modes (Modes 0, 1, 2, 3 and 6). Modes 0, 1, 2 and 6 are the same for both Timers/Counters. Mode 3 is different.

7.19.1 Mode 0

Putting either Timer into Mode 0 makes it look like an 8048 Timer, which is an 8-bit Counter with a divide-by-32 prescaler. In this mode, the Timer register is configured as a 13-bit register. Mode 0 operation is the same for Timer 0 and Timer 1.

7.19.2 Mode 1

Mode 1 is the same as Mode 0, except that all 16 bits of the timer register are used.

7.19.3 Mode 2

Mode 2 configures the Timer register as an 8-bit Counter with automatic reload. Mode 2 operation is the same for Timer 0 and Timer 1.

7.19.3.1 Mode 3

When Timer 1 is in Mode 3 it is stopped. Timer 0 in Mode 3 forms two separate 8-bit counters and is provided for applications that require an extra 8-bit timer. When Timer 1 is in Mode 3 it can still be used by the serial port as a baud rate generator.

7.19.3.2 Mode 6

In this mode, the corresponding timer can be changed to a PWM with a full period of 256 timer clocks.

7.19.4 Timer overflow toggle output

Timers 0 and 1 can be configured to automatically toggle a port output whenever a timer overflow occurs. The same device pins that are used for the T0 and T1 count inputs are also used for the timer toggle outputs. The port outputs will be a logic 1 prior to the first timer overflow when this mode is turned on.

7.20 Timers/counters 2, 3 and 4

The P89LPC970/971/972 has three external 16-bit timer/counters. All can be configured to operate either as timers or event counters. An option to automatically toggle pin Tx (x = 2, 3 or 4) upon timer overflow has been added.

In the ‘Timer’ function, the register is incremented every PCLK.

In the ‘Counter’ function, the register is incremented in response to a 1-to-0 transition at its corresponding count input pin (T2/T3 /T4). In this function, the count input is sampled once during every machine cycle.

Only external Timer 2/3/4 has the external input pin TxEX (x = 2, 3 or 4). A 1-to-0 transition on this pin can trigger a reload or capture event.

Timer 2, Timer 3 and Timer 4 have three operating modes (Modes 0, 1 and 2).

7.20.1 Mode 0: 16-bit timer/counter with auto-reload

Mode 0 configures the timer register as an 16-bit Timer/counter with automatic reload. An overflow upon the timer or a 1-to-0 transition at TxEX pin can cause the reload event.

7.20.2 Mode 1: 16-bit timer/counter with input capture

Mode 1 configures the timer register as an 16-bit Timer/counter with input capture. A 1-to-0 transition at TxEX pin can cause the capture event.

7.20.3 Mode 2: 16-bit PWM mode

In this mode, the corresponding timer can be changed to a 16-bit PWM generator with adjustable duty cycle. In this mode, the corresponding timer can be changed to a 16-bit PWM generator with adjustable duty cycle and adjustable full period (from 0, theoretically, to 131072).

7.20.4 Timer overflow toggle output

Timers 2, 3 and 4 can be configured to automatically toggle a port output whenever a timer overflow occurs. The same device pins that are used for the T2, T3 and T4 count inputs are also used for the timer toggle outputs. The port outputs will be a logic 1 prior to the first timer overflow when this mode is turned on.

7.21 RTC/system timer

The P89LPC970/971/972 has a simple RTC that allows a user to continue running an accurate timer while the rest of the device is powered down. The RTC can be a wake-up or an interrupt source. The RTC is a 23-bit down counter comprised of a 7-bit prescaler and a 16-bit loadable down counter. When it reaches all logic 0s, the counter will be reloaded again and the RTCF flag will be set. The clock source for this counter can be either the CPU clock (CCLK) or the XTAL oscillator. Only power-on reset and watchdog reset will reset the RTC and its associated SFRs to the default state.

The 16-bit loadable counter portion of the RTC is readable by reading the RTCDATL and RTCDATH registers.

7.22 UART

The P89LPC970/971/972 has an enhanced UART that is compatible with the conventional 80C51 UART except that Timer 2 overflow cannot be used as a baud rate source. The P89LPC970/971/972 does include an independent baud rate generator. The baud rate can be selected from the oscillator (divided by a constant), Timer 1 overflow, or the independent baud rate generator. In addition to the baud rate generation, enhancements over the standard 80C51 UART include Framing Error detection, automatic address recognition, selectable double buffering and several interrupt options. The UART can be operated in four modes: shift register, 8-bit UART, 9-bit UART, and CPU clock/32 or CPU clock/16.

7.22.1 Mode 0

Serial data enters and exits through RXD. TXD outputs the shift clock. 8 bits are transmitted or received, LSB first. The baud rate is fixed at $^1/_{16}$ of the CPU clock frequency.

7.22.2 Mode 1

10 bits are transmitted (through TXD) or received (through RXD): a start bit (logic 0), 8 data bits (LSB first), and a stop bit (logic 1). When data is received, the stop bit is stored in RB8 in special function register SCON. The baud rate is variable and is determined by the Timer 1 overflow rate or the baud rate generator (described in Section 7.22.5 “Baud rate generator and selection”).

7.22.3 Mode 2

11 bits are transmitted (through TXD) or received (through RXD): start bit (logic 0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logic 1). When data is transmitted, the 9th data bit (TB8 in SCON) can be assigned the value of logic 0 or logic 1. Or, for example, the parity bit (P, in the PSW) could be moved into TB8. When data is received, the 9th data bit goes into RB8 in special function register SCON, while the stop bit is not saved. The baud rate is programmable to either $1/16$ or $1/32$ of the CPU clock frequency, as determined by the SMOD1 bit in PCON.

7.22.4 Mode 3

11 bits are transmitted (through TXD) or received (through RXD): a start bit (logic 0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logic 1). In fact, Mode 3 is the same as Mode 2 in all respects except baud rate. The baud rate in Mode 3 is variable and is determined by the Timer 1 overflow rate or the baud rate generator (described in Section 7.22.5 “Baud rate generator and selection”).

7.22.5 Baud rate generator and selection

The P89LPC970/971/972 enhanced UART has an independent baud rate generator. The baud rate is determined by a baud-rate preprogrammed into the BRGR1 and BRGR0 SFRs which together form a 16-bit baud rate divisor value that works in a similar manner as Timer 1 but is much more accurate. If the baud rate generator is used, Timer 1 can be used for other timing functions.

The UART can use either Timer 1 or the baud rate generator output (see Figure 7). Note that Timer T1 is further divided by 2 if the SMOD1 bit (PCON.7) is cleared. The independent baud rate generators use OSCCLK.

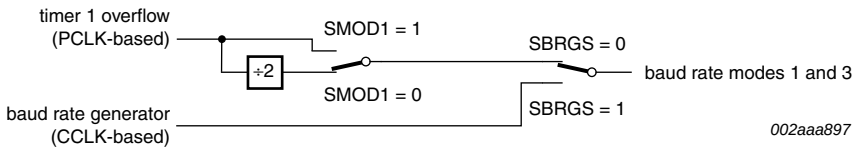


Fig 7. Baud rate sources for UART (Modes 1, 3)

7.22.6 Framing error

Framing error is reported in the status register (SSTAT). In addition, if SMOD0 (PCON.6) is logic 1, framing errors can be made available in SCON.7 respectively. If SMOD0 is logic 0, SCON.7 is SM0. It is recommended that SM0 and SM1 (SCON.7:6) are set up when SMOD0 is logic 0.

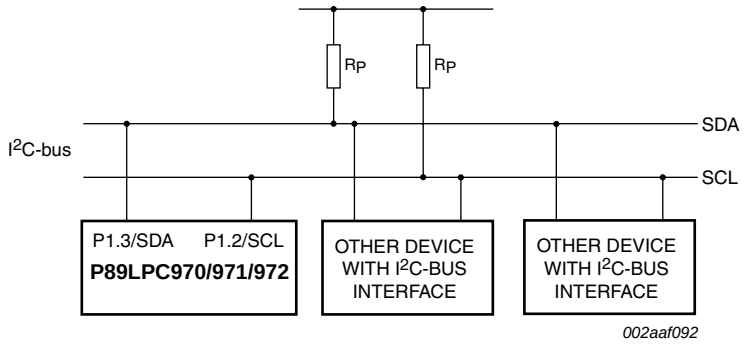
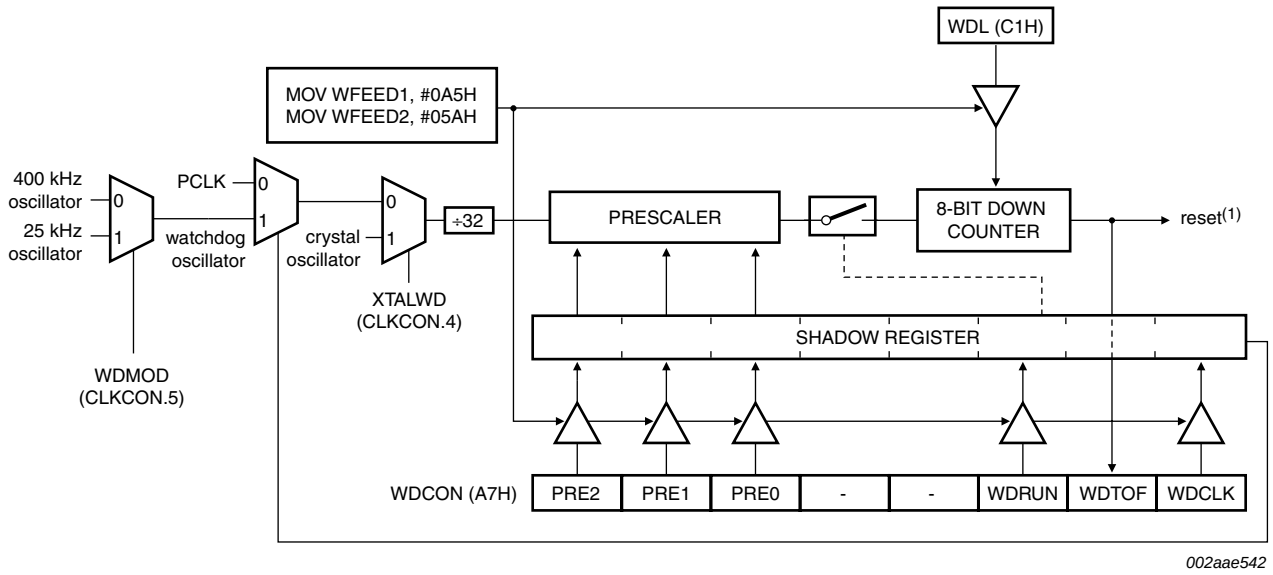


Fig 8. I^2C-bus configuration



(1) Watchdog reset can also be caused by an invalid feed sequence, or by writing to WDCON not immediately followed by a feed sequence.

Fig 15. Watchdog timer in Watchdog mode (WDTE = 1)

7.28 Additional features

7.28.1 Software reset

The SRST bit in AUXR1 gives software the opportunity to reset the processor completely, as if an external reset or watchdog reset had occurred. Care should be taken when writing to AUXR1 to avoid accidental software resets.

7.28.2 Dual data pointers

The dual Data Pointers (DPTR) provides two different Data Pointers to specify the address used with certain instructions. The DPS bit in the AUXR1 register selects one of the two Data Pointers. Bit 2 of AUXR1 is permanently wired as a logic 0 so that the DPS bit may be toggled (thereby switching Data Pointers) simply by incrementing the AUXR1 register, without the possibility of inadvertently altering other bits in the register.

7.29 Flash program memory

7.29.1 General description

The P89LPC970/971/972 flash memory provides in-circuit electrical erasure and programming. The flash can be erased, read, and written as bytes. The Sector and Page Erase functions can erase any flash sector (1 kB) or page (64 bytes). The Chip Erase operation will erase the entire program memory. ICP using standard commercial programmers is available. In addition, IAP and byte-erase allows code memory to be used for non-volatile data storage. On-chip erase and write timing generation contribute to a user-friendly programming interface. The P89LPC970/971/972 flash reliably stores memory contents even after 100000 erase and program cycles. The cell is designed to

Remark: Users who wish to use this loader should take precautions to avoid erasing the 1 kB sector that contains this bootloader. Instead, the page erase function can be used to erase the first eight 64-byte pages located in this sector.

A custom bootloader can be written with the Boot Vector set to the custom bootloader, if desired.

Table 9. Default boot vector values and ISP entry points

Device	Default boot vector	Default bootloader entry point	Default bootloader code range	1 kB sector range
P89LPC970	07H	0700H	0600H to 07FFH	0400H to 07FFH
P89LPC971	0FH	0F00H	0E00H to 1FFFH	0C00H to 0FFFH
P89LPC972	1FH	1F00H	1E00H to 1FFFH	1C00H to 1FFFH

7.29.10 Hardware activation of the bootloader

The bootloader can also be executed by forcing the device into ISP mode during a power-on sequence (see the *P89LPC970/971/972 User manual* for specific information). This has the same effect as having a non-zero status byte. This allows an application to be built that will normally execute user code but can be manually forced into ISP operation. If the factory default setting for the boot is changed, it will no longer point to the factory pre-programmed ISP bootloader code. After programming the flash, the status byte should be programmed to zero in order to allow execution of the user's application code beginning at address 0000H.

7.30 User configuration bytes

Some user-configurable features of the P89LPC970/971/972 must be defined at power-up and therefore cannot be set by the program after start of execution. These features are configured through the use of the flash byte UCFG1 and UCFG2. Please see the *P89LPC970/971/972 User Manual* for additional details.

7.31 User sector security bytes

There are four/eight User Sector Security Bytes on the P89LPC970/971/972. Each byte corresponds to one sector. Please see the *P89LPC970/971/972 User manual* for additional details.

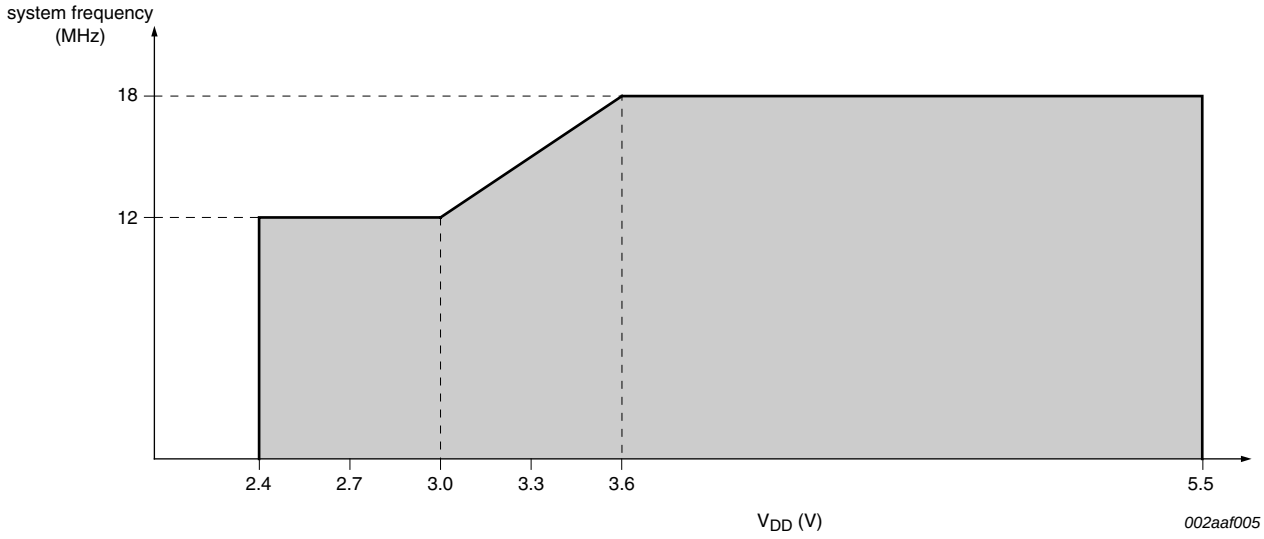


Fig 16. Frequency vs. supply voltage

9. Static characteristics

Table 11. Static characteristics

V_{DD} = 2.4 V to 5.5 V unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$I_{DD(oper)}$	operating supply current	V_{DD} = 2.4 V					
		f_{osc} = 12 MHz, High-speed mode of regulators	[2]	-	6	7	mA
		f_{osc} = 12 MHz, Low current mode of regulators	[2]	-	5	6	mA
		V_{DD} = 3.3 V					
		f_{osc} = 12 MHz, High-speed mode of regulators	[2]	-	9	10	mA
		f_{osc} = 12 MHz, Low current mode of regulators	[2]	-	7	8	mA
		V_{DD} = 5.5 V					
		f_{osc} = 12 MHz, High-speed mode of regulators	[2]	-	10	11	mA
		f_{osc} = 12 MHz, Low current mode of regulators	[2]	-	8	9	mA
		f_{osc} = 18 MHz, High-speed mode of regulators	[2]	-	11	12	mA
$I_{DD(idle)}$	Idle mode supply current	V_{DD} = 2.4 V					
		f_{osc} = 12 MHz, High-speed mode of regulators	[2]	-	3.5	4.5	mA
		f_{osc} = 12 MHz, Low current mode of regulators	[2]	-	3	4	mA
		V_{DD} = 3.3 V					
		f_{osc} = 12 MHz, High-speed mode of regulators	[2]	-	5	6	mA
		f_{osc} = 12 MHz, Low current mode of regulators	[2]	-	4	5	mA
		V_{DD} = 5.5 V					
		f_{osc} = 12 MHz, High-speed mode of regulators	[2]	-	6	7	mA
		f_{osc} = 12 MHz, Low current mode of regulators	[2]	-	4	5	mA
		f_{osc} = 18 MHz, High-speed mode of regulators	[2]	-	6.5	7.5	mA
$I_{DD(pd)}$	Power-down mode supply current	V_{DD} = 2.4 V; voltage comparators powered down	[3]	-	28	35	μA
		V_{DD} = 3.3 V; voltage comparators powered down	[3]	-	32	40	μA
		V_{DD} = 5.5 V; voltage comparators powered down	[3]	-	38	45	μA

Table 11. Static characteristics *…continued*
V_{DD} = 2.4 V to 5.5 V unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
$R_{RST\_N(int)}$	internal pull-up resistance on pin $\overline{RST}$	pin $\overline{RST}$	30	-	120	kΩ
BOD interrupt						
V_{trip}	trip voltage	falling stage				
		BOICFG2, BOICFG1, BOICFG0 = 010	2.45	-	2.65	V
		BOICFG2, BOICFG1, BOICFG0 = 011	2.75	-	2.95	V
		BOICFG2, BOICFG1, BOICFG0 = 100	2.90	-	3.10	V
		BOICFG2, BOICFG1, BOICFG0 = 101	3.35	-	3.55	V
		BOICFG2, BOICFG1, BOICFG0 = 110	4.10	-	4.30	V
		BOICFG2, BOICFG1, BOICFG0 = 111	4.25	-	4.45	V
		rising stage				
		BOICFG2, BOICFG1, BOICFG0 = 010	2.60	-	2.80	V
		BOICFG2, BOICFG1, BOICFG0 = 011	2.90	-	3.10	V
		BOICFG2, BOICFG1, BOICFG0 = 100	3.05	-	3.25	V
		BOICFG2, BOICFG1, BOICFG0 = 101	3.50	-	3.70	V
		BOICFG2, BOICFG1, BOICFG0 = 110	4.15	-	4.35	V
		BOICFG2, BOICFG1, BOICFG0 = 111	4.35	-	4.55	V

Table 13. Dynamic characteristics (18 MHz)

V_{DD} = 3.6 V to 5.5 V unless otherwise specified.

T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.[1][2]

Symbol	Parameter	Conditions	Variable clock		f_{osc} = 18 MHz		Unit
			Min	Max	Min	Max	
$f_{osc(RC)}$	internal RC oscillator frequency	nominal f = 7.3728 MHz trimmed to ±1 % at T_{amb} = 25 °C; clock doubler option = OFF (default)	7.189	7.557	7.189	7.557	MHz
		nominal f = 14.7456 MHz; clock doubler option = ON	14.378	15.114	14.378	15.114	MHz
$f_{osc(WD)}$	internal watchdog oscillator frequency		360	440	360	440	kHz
f_{osc}	oscillator frequency		0	18	-	-	MHz
$T_{cy(clk)}$	clock cycle time	see Figure 17	55	-	-	-	ns
f_{CLKLP}	low-power select clock frequency		0	8	-	-	MHz
Glitch filter							
t_{gr}	glitch rejection time	P1.5/$\overline{RST}$ pin	-	50	-	50	ns
		any pin except P1.5/$\overline{RST}$	-	15	-	15	ns
t_{sa}	signal acceptance time	P1.5/$\overline{RST}$ pin	125	-	125	-	ns
		any pin except P1.5/$\overline{RST}$	50	-	50	-	ns
External clock							
t_{CHCX}	clock HIGH time	see Figure 17	22	$T_{cy(clk)} - t_{CLCX}$	22	-	ns
t_{CLCX}	clock LOW time	see Figure 17	22	$T_{cy(clk)} - t_{CHCX}$	22	-	ns
t_{CLCH}	clock rise time	see Figure 17	-	5	-	5	ns
t_{CHCL}	clock fall time	see Figure 17	-	5	-	5	ns
Shift register (UART mode 0)							
T_{XLXL}	serial port clock cycle time	see Figure 18	$16T_{cy(clk)}$	-	888	-	ns
t_{QVXH}	output data set-up to clock rising edge time	see Figure 18	$13T_{cy(clk)}$	-	722	-	ns
t_{XHQX}	output data hold after clock rising edge time	see Figure 18	-	$T_{cy(clk)}$ + 20	-	75	ns
t_{XHDX}	input data hold after clock rising edge time	see Figure 18	-	0	-	0	ns
t_{XHDV}	input data valid to clock rising edge time	see Figure 18	150	-	150	-	ns
SPI interface							
f_{SPI}	SPI operating frequency						
	slave		0	$^{CCLK}/_{6}$	0	3.0	MHz
	master		-	$^{CCLK}/_{4}$	-	4.5	MHz
T_{SPICYC}	SPI cycle time	see Figure 19, 20, 21, 22					
	slave		$^{6}/_{CCLK}$	-	333	-	ns
	master		$^{4}/_{CCLK}$	-	222	-	ns

10.1 Waveforms

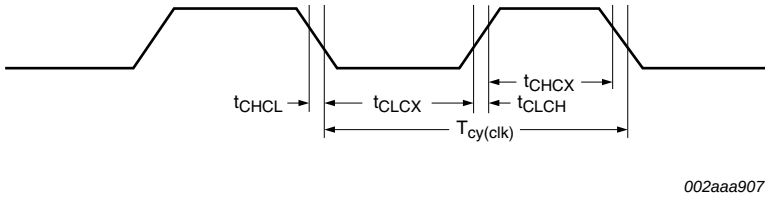


Fig 17. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

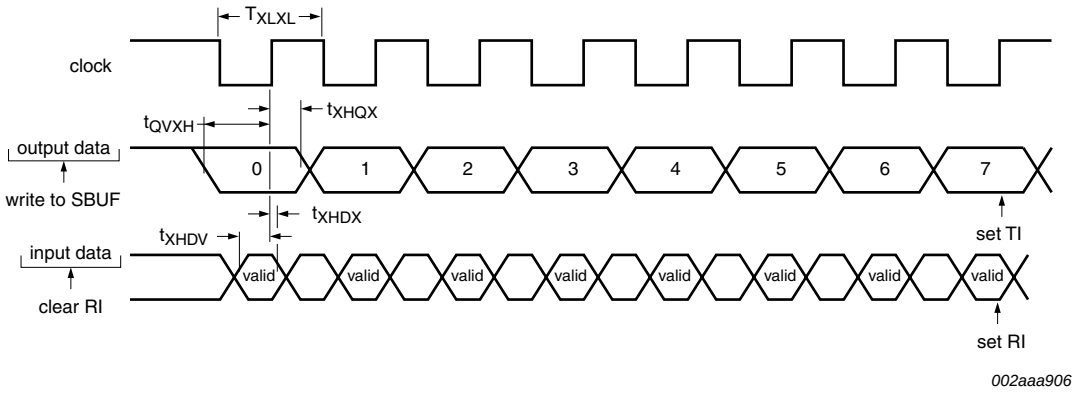


Fig 18. Shift register mode timing

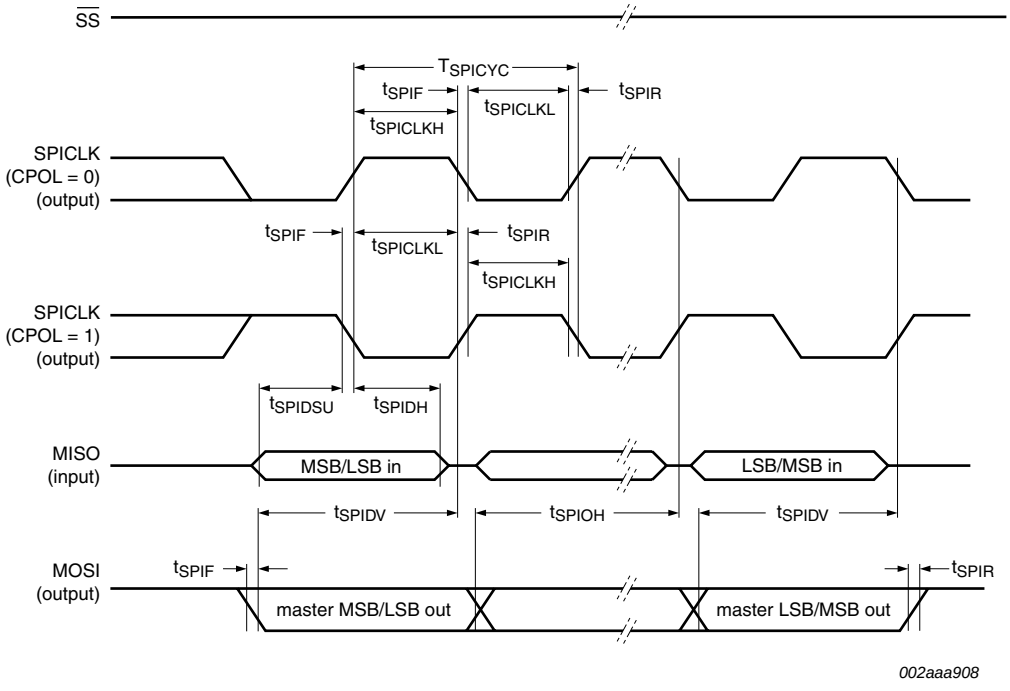
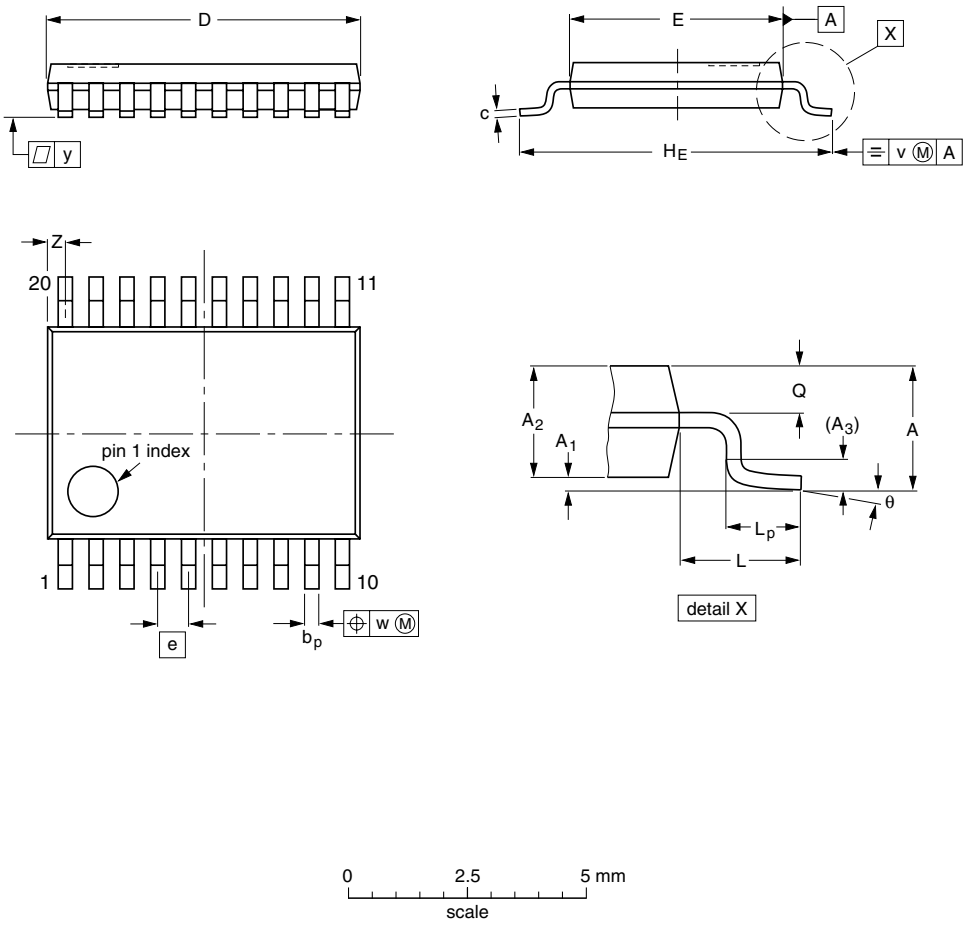


Fig 19. SPI master timing (CPHA = 0)

12. Package outline

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				~~99-12-27~~ 03-02-19

Fig 24. TSSOP20 package outline (SOT360-1)

13. Abbreviations

Table 16. Abbreviations

Acronym	Description
CCU	Capture/Compare Unit
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
DAC	Digital to Analog Converter
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMI	Electro-Magnetic Interference
EPROM	Erasable Programmable Read-Only Memory
GPIO	General Purpose Input/Output
IRC	Internal RC
LSB	Least Significant Bit
MSB	Most Significant Bit
PGA	Programmable Gain Amplifier
PLL	Phase-Locked Loop
PWM	Pulse Width Modulator
RAM	Random Access Memory
RC	Resistance-Capacitance
RTC	Real-Time Clock
SAR	Successive Approximation Register
SFR	Special Function Register
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter
WDT	Watchdog Timer

17. Contents

continued >>