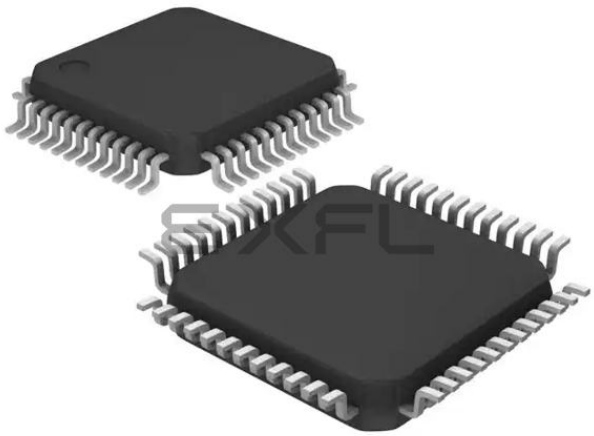

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Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	Automotive
Core Processor	S12
Program Memory Type	FLASH (48kB)
Controller Series	HCS12
RAM Size	2K x 8
Interface	LIN, SCI
Number of I/O	9
Voltage - Supply	2.25V ~ 5.25V
Operating Temperature	-40°C ~ 105°C
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mm912g634cv2ap

Table 64. 0x00D8–0x00DF Die 2 Die Initiator (D2DI) Map 1 of 3

0x00DD	D2DADRLO	R	ADR[7:0]							
		W								
0x00DE	D2DDATAHI	R	DATA[15:8]							
		W								
0x00DF	D2DDATALO	R	DATA[7:0]							
		W								

Table 65. 0x00E0–0x0E7 Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00E0- 0x00E7	Reserved	R	0	0	0	0	0	0	0	0
		W								

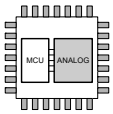
Table 66. 0x00E8–0x00EF Serial Peripheral Interface (SPI)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00E8	SPICR1	R	SPIE	SPE	SPTIE	MSTR	CPOL	CPHA	SSOE	LSBFE
		W								
0x00E9	SPICR2	R	0	XFRW	0	MODFEN	BIDIROE	0	SPISWAI	SPC0
		W								
0x00EA	SPIBR	R	0	SPPR2	SPPR1	SPPR0	0	SPR2	SPR1	SPR0
		W								
0x00EB	SPISR	R	SPIF	0	SPTEF	MODF	0	0	0	0
		W								
0x00EC	SPIDRH	R	R15	R14	R13	R12	R11	R10	R9	R8
		W	T15	T14	T13	T12	T11	T10	T9	T8
0x00ED	SPIDRL	R	R7	R6	R5	R4	R3	R2	R1	R0
		W	T7	T6	T5	T4	T3	T2	T1	T0
0x00EE	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x00EF	Reserved	R	0	0	0	0	0	0	0	0
		W								

Table 67. 0x00F0–0x0FF Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00E0- 0x00FF	Reserved	R	0	0	0	0	0	0	0	0
		W								

5.9 Wake-up / Cyclic Sense



To wake-up the MM912_634 analog die from Stop or Sleep mode, several wake-up sources are implemented. As described in Section 5.4, “Modes of Operation", a wake-up from Stop mode will result in an interrupt (D2DINT) to the MCU combined with a transition to Normal mode. A wake-up from Sleep mode will result in a transition to Reset mode. In any case, the source of the wake-up can be identified by reading the Wake-up Source Register (WSR). The Wake-up Source Register (WSR) has to be read after a wake-up condition in order to execute a new STOP mode command. Two base clock cycles (f_{BASE}) delay are required between the WSR read and MCR write.

In general, there are the following seven main wake-up sources:

- Wake-up by a state change of one of the Lx inputs
- Wake-up by a state change of one of the Lx inputs during a cyclic sense
- Wake-up due to a forced wake-up
- Wake-up by the LIN module
- Wake-up by D2D interface (Stop mode only)
- Wake-up due to internal / external Reset (Stop mode only)
- Wake-up due to loss of supply voltage (Sleep mode only)

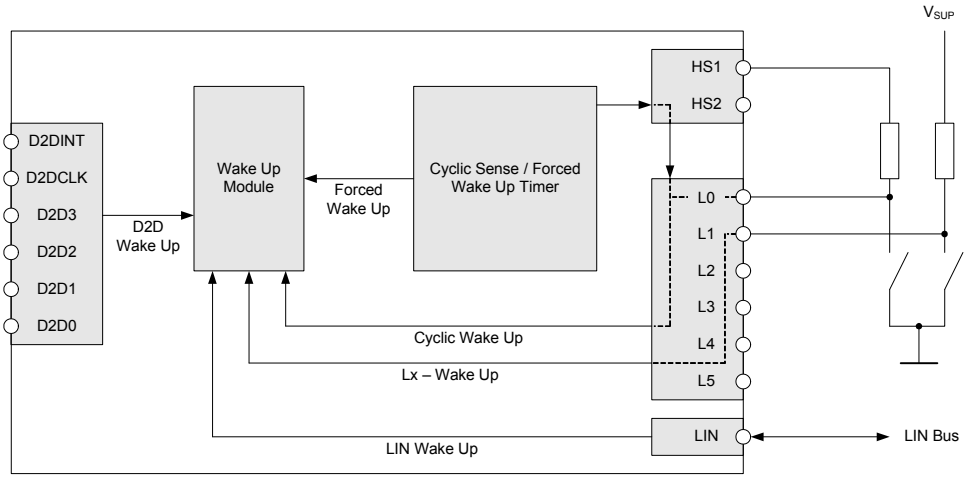


Figure 19. Wake-up Sources

5.9.1 Wake-up Sources

5.9.1.1 Lx - Wake-up (Cyclic Sense Disabled)

Any state digital change on a Wake-up Enabled Lx input will issue a wake-up. In order to select and activate a Wake-up Input (Lx), the Wake-up Control Register (WCR) must be configured with appropriate LxWE inputs enabled or disabled before entering low power mode. The Lx - Wake-up may be combined with the Forced Wake-up.

Note: Selecting a Lx Input for wake-up will disable a selected analog input once entering low power mode.

5.9.1.2 Lx - Cyclic Sense Wake-up

To reduce external power consumption during low power mode a cyclic wake-up has been implemented. Configuring the Timing Control Register (TCR) a specific cycle time can be selected to implement a periodic switching of the HS1 or HS2 output with the corresponding detection of an Lx state change. Any configuration of the HSx in the High Side Control Register (HSCR) will be ignored when entering low power mode. The Lx - Cyclic Sense Wake-up may be combined with the Forced Wake-up. In case both (forced and Lx change) events are present at the same time, the Forced Wake-up will be indicated as Wake-up source.

NOTE

Once Cyclic Sense is configured (CSSEL!=0), the state change is only recognized from one cyclic sense event to the next.

The additional accuracy of the cyclic sense cycle by the WD clock trimming is only active during STOP mode. There is no trimmed clock available during SLEEP mode.

NOTE

Clock SA = Clock A / (2 * PWMSCLA)

When PWMSCLA = $00, PWMSCLA value is considered a full scale value of 256. Clock A is thus divided by 512.

Similarly, clock B is used as an input to an 8-bit down counter followed by a divide by two producing clock SB. Thus, clock SB equals clock B divided by two times the value in the PWMSCLB register.

NOTE

Clock SB = Clock B / (2 * PWMSCLB)

When PWMSCLB = $00, PWMSCLB value is considered a full scale value of 256. Clock B is thus divided by 512.

As an example, consider the case in which the user writes $FF into the PWMSCLA register. Clock A for this case will be E divided by 4. A pulse will occur at a rate of once every 255x4 E cycles. Passing this through the divide by two circuit produces a clock signal at an E divided by 2040 rate. Similarly, a value of $01 in the PWMSCLA register when clock A is E divided by 4 will produce a clock at an E divided by 8 rate.

Writing to PWMSCLA or PWMSCLB causes the associated 8-bit down counter to be re-loaded. Otherwise, when changing rates the counter would have to count down to $01 before counting at the proper rate. Forcing the associated counter to re-load the scale register value every time PWMSCLA or PWMSCLB is written prevents this.

NOTE

Writing to the scale registers while channels are operating can cause irregularities in the PWM outputs.

5.14.4.1.3 Clock Select

Each PWM channel has the capability of selecting one of two clocks. For channels 0 the clock choice is clock A or clock SA. For channels 1 the choice is clock B or clock SB. The clock selection is done with the PCLKx control bits in the PWMCTL register.

NOTE

Changing clock control bits while channels are operating can cause irregularities in the PWM outputs.

5.14.4.2 PWM Channel Timers

The main part of the PWM module are the actual timers. Each of the timer channels has a counter, a period register, and a duty register (each are 8-bit). The waveform output period is controlled by a match between the period register and the value in the counter. The duty is controlled by a match between the duty register and the counter value, and causes the state of the output to change during the period. The starting polarity of the output is also selectable on a per channel basis. Shown in Figure 24 is the block diagram for the PWM timer.

5.16.2.2 SCI Control Register 1 (SCIC1)

This read/write register is used to control various optional features of the SCI system.

Table 138. SCI Control Register 1 (SCIC1)

Offset(101) 0x42 Access: User read/write

	7	6	5	4	3	2	1	0
R	LOOPS	0	RSRC	M	0	ILT	PE	PT
W								
Reset	0	0	0	0	0	0	0	0

Note:
101. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 139. SCIC1 Field Descriptions

Field	Description
7 LOOPS	Loop Mode Select — Selects between loop back modes and normal 2-pin full-duplex modes. When LOOPS = 1, the transmitter output is internally connected to the receiver input. 0 Normal operation — RxD and TxD use separate pins. 1 Loop mode or single-wire mode where transmitter outputs are internally connected to receiver input. (See RSRC bit.) RxD pin is not used by SCI.
5 RSRC	Receiver Source Select — This bit has no meaning or effect unless the LOOPS bit is set to 1. When LOOPS = 1, the receiver input is internally connected to the TxD pin and RSRC determines whether this connection is also connected to the transmitter output. 0 Provided LOOPS = 1, RSRC = 0 selects internal loop back mode and the SCI does not use the RxD pins. 1 Single-wire SCI mode where the TxD pin is connected to the transmitter output and receiver input.
4 M	9-Bit or 8-Bit Mode Select 0 Normal — start + 8 data bits (LSB first) + stop. 1 Receiver and transmitter use 9-bit data characters start + 8 data bits (LSB first) + 9th data bit + stop.
2 ILT	Idle Line Type Select — Setting this bit to 1 ensures that the stop bit and logic 1 bits at the end of a character do not count toward the 10 or 11 bit times of logic high level needed by the idle line detection logic. Refer to Section 5.16.3.3.2.1, “Idle-line Wake-up" for more information. 0 Idle character bit count starts after start bit. 1 Idle character bit count starts after stop bit.
1 PE	Parity Enable — Enables hardware parity generation and checking. When parity is enabled, the most significant bit (MSB) of the data character (eighth or ninth data bit) is treated as the parity bit. 0 No hardware parity generation or checking. 1 Parity enabled.
0 PT	Parity Type — Provided parity is enabled (PE = 1), this bit selects even or odd parity. Odd parity means the total number of 1s in the data character, including the parity bit, is odd. Even parity means the total number of 1s in the data character, including the parity bit, is even. 0 Even parity. 1 Odd parity.

5.16.3 Functional Description

The SCI allows full-duplex, asynchronous, NRZ serial communication among the MCU and remote devices, including other MCUs. The SCI comprises a baud rate generator, transmitter, and receiver block. The transmitter and receiver operate independently, although they use the same baud rate generator. During normal operation, the MCU monitors the status of the SCI, writes the data to be transmitted, and processes received data. The following describes each of the blocks of the SCI.

5.16.3.1 Baud Rate Generation

As shown in Figure 31, the clock source for the SCI baud rate generator is the D2D clock.

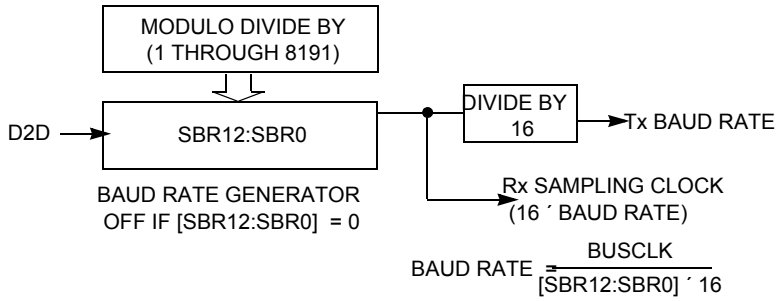


Figure 31. SCI Baud Rate Generation

SCI communications require the transmitter and receiver (which typically derive baud rates from independent clock sources) to use the same baud rate. Allowed tolerance on this baud frequency depends on the details of how the receiver synchronizes to the leading edge of the start bit and how bit sampling is performed.

The MCU resynchronizes to bit boundaries on every high-to-low transition, but in the worst case, there are no such transitions in the full 10- or 11-bit time character frame so any mismatch in baud rate is accumulated for the whole character time. For a Freescale Semiconductor SCI system whose bus frequency is driven by a crystal, the allowed baud rate mismatch is about ±4.5 percent for 8-bit data format and about ±4.0 percent for 9-bit data format. Although baud rate modulo divider settings do not always produce baud rates that exactly match standard rates, it is normally possible to get within a few percent, which is acceptable for reliable communications.

5.16.3.2 Transmitter Functional Description

This section describes the overall block diagram for the SCI transmitter, as well as specialized functions for sending break and idle characters. The transmitter block diagram is shown in Figure 29.

The transmitter output (TxD) idle state defaults to logic high (TXINV = 0 following reset). The transmitter output is inverted by setting TXINV = 1. The transmitter is enabled by setting the TE bit in SCIC2. This queues a preamble character that is one full character frame of the idle state. The transmitter then remains idle until data is available in the transmit data buffer. Programs store data into the transmit data buffer by writing to the SCI data register (SCID).

The central element of the SCI transmitter is the transmit shift register that is either 10 or 11 bits long depending on the setting in the M control bit. For the remainder of this section, we will assume M = 0, selecting the normal 8-bit data mode. In 8-bit data mode, the shift register holds a start bit, eight data bits, and a stop bit. When the transmit shift register is available for a new SCI character, the value waiting in the transmit data register is transferred to the shift register (synchronized with the baud rate clock) and the transmit data register empty (TDRE) status flag is set to indicate another character may be written to the transmit data buffer at SCID.

If no new character is waiting in the transmit data buffer after a stop bit is shifted out the TxD pin, the transmitter sets the transmit complete flag and enters an idle mode, with TxD high, waiting for more characters to transmit.

Writing 0 to TE does not immediately release the pin to be a general-purpose I/O pin. Any transmit activity that is in progress must first be completed. This includes data characters in progress, queued idle characters, and queued break characters.

5.16.3.2.1 Send Break and Queued Idle

The SBK control bit in SCIC2 is used to send break characters which were originally used to gain the attention of old teletype receivers. Break characters are a full character time of logic 0 (10 bit times including the start and stop bits). A longer break of 13 bit times can be enabled by setting BRK13 = 1. Normally, a program would wait for TDRE to become set to indicate the last character of a message has moved to the transmit shifter, then write 1 and then write 0 to the SBK bit. This action queues a break character to be sent as soon as the shifter is available. If SBK is still 1 when the queued break moves into the shifter

5.20.4.2.4 ADC Conversion Complete Status Register (ACCSR)

Table 205. ADC Conversion Complete Status Register (ACCSR)

Offset[142] 0x84 (0x84 and 0x85 for 8-Bit access) Access: User read

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	CC15	CC14	0	CC12	CC11	CC10	CC9	CC8	CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note:
142. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 206. ACCSR - Register Field Descriptions

Field	Description
15-0 CCx	Conversion Complete Flag - Indicates the conversion being complete for channel x. Read operation only.16-bit read recommended. 8-Bit read will return the current status, no latching will be performed.

5.20.4.2.5 ADC Data Result Register x (ADRx)

Table 207. ADC Data Result Register x (ADRx)

Offset[143] 0x86+x (0x86 and 0x87 for 8-Bit access) Access: User read

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	ADRx										0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note:
143. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 208. ADRx - Register Field Descriptions

Field	Description
15-6 ADRx	ADC - Channel X left adjusted Result Register. Reading the register will clear the corresponding CCx register in the ACCSR register. 16-bit read recommended. 8-Bit read: Reading the low byte will latch the high byte for the next read, reading the high byte will clear the cc flag.

5.20.5 Functional Description

5.20.5.1 Analog Channel Definitions

The following analog Channels are routed to the analog multiplexer:

Table 209. Analog Channels

Channel	Description	
0	AD0 - PTB0 Analog Input	AD0
1	AD1 - PTB1 Analog Input	AD1
2	AD2 - PTB2 Analog Input	AD2
3	AD3 - L0 Analog Input	AD3
4	AD4 - L1 Analog Input	AD4
5	AD5 - L2 Analog Input	AD5
6	AD6 - L3 Analog Input	AD6

5.21 Current Sense Module - ISENSE

The Current Sense Module is implemented to amplify the voltage drop across an external shunt resistor to measure the actual application current using the internal Analog Digital Converter Channel 9. Typical application is the motor current in a window lift control module

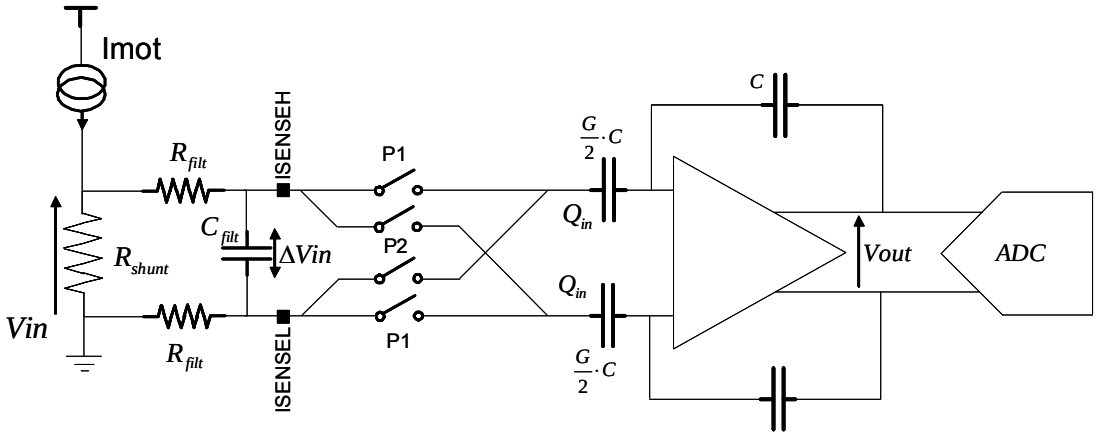


Figure 37. Current Sense Module with External Filter Option

The implementation is based on a switched capacitor solution to eliminate unwanted offset.To fit several application scenarios, eight different GAIN setting are implemented.

5.21.1 Register Definition

5.21.1.1 Current Sense Register (CSR)

Table 210. Current Sense Register (CSR)

Offset[145] 0x3C — Access: User read/write

	7	6	5	4	3	2	1	0
R	CSE	0	0	0	CCD	CSGS		
W								
Reset	0	0	0	0	0	0	0	0

Note:
145. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 219. CTR2 - Register Field Descriptions

Field	Description
4 SLPBGTRE	Sleep Bandgap trim enable 0 no trim can be done 1 trim lock can be done by setting SLPBGTR[2:0] bits and SLPBG_LOCK bit
3 SLPBG_LOCK	bg1p25sleep trim lock bit
2-0 SLPBGTR2…0	bg1p25sleep trim - This trim is used to adjust the internal sleep mode 1.25 V bandgap used as a reference for the VDD and VDDx over-voltage detection. 000: -12.2% (default) 001: -8.2% 010: -4.2% 011: 0% 100: +4.2% 101: +8.3% 110: +12.5% 111: -12.2% (default)

5.26.1.2.4 Trimming Register 3 (CTR3)

Table 220. Trimming Register 3 (CTR3)

Offset[153] 0xF3 — Access: User read/write

	7	6	5	4	3	2	1	0
R W	OFFCTRE	OFFCTR2	OFFCTR1	OFFCTR0	CTR3_E	CTR3_2	CTR3_1	CTR3_0
Reset	0	0	0	0	0	0	0	0

Note:
153. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 229. PORTA Register Field Descriptions

Field	Description
7–4 PA	**Port A general purpose input/output data**—Data RegisterIn output mode the register bit is driven to the pin. If the associated data direction bit of this pin is set to 1, a read returns the value of the port register, otherwise the buffered and synchronized pin input state is read.
3 PA	**Port A general purpose input/output data**—Data Register, SPI $\overline{SS}$ input/output When not used with the alternative function, this pin can be used as general purpose I/O. In general purpose output mode the register bit is driven to the pin. If the associated data direction bit of this pin is set to 1, a read returns the value of the port register, otherwise the buffered pin input state is read. • The SPI function takes precedence over the general purpose I/O function if enabled.
2 PA	**Port A general purpose input/output data**—Data Register, SPI SCK input/output When not used with the alternative function, this pin can be used as general purpose I/O. In general purpose output mode the register bit is driven to the pin. If the associated data direction bit of this pin is set to 1, a read returns the value of the port register, otherwise the buffered pin input state is read. • The SPI function takes precedence over the general purpose I/O function if enabled.
1 PA	**Port A general purpose input/output data**—Data Register, SPI MOSI input/output When not used with the alternative function, this pin can be used as general purpose I/O. In general purpose output mode the register bit is driven to the pin. If the associated data direction bit of this pin is set to 1, a read returns the value of the port register, otherwise the buffered pin input state is read. • The SPI function takes precedence over the general purpose I/O function if enabled.
0 PA	**Port A general purpose input/output data**—Data Register, SPI MISO input/output When not used with the alternative function, this pin can be used as general purpose I/O. In general purpose output mode the register bit is driven to the pin. If the associated data direction bit of this pin is set to 1, a read returns the value of the port register, otherwise the buffered pin input state is read. • The SPI function takes precedence over the general purpose I/O function if enabled.

5.28.2.3 Port E Data Register (PORTE)

Table 230. Port E Data Register (PORTE)

Address 0x0001 Access: User read/write(157)

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	PE1	PE0
W								
CPMU OSC Function	—	—	—	—	—	—	XTAL	EXTAL
Reset	0	0	0	0	0	0	0	0

Note:
157. Read: Anytime.
Write: Anytime.

Table 248. MMC Register Summary

Address	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x000A	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x000B	MODE	R	MODC	0	0	0	0	0	0	0
		W								
0x0010	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0011	DIRECT	R	DP15	DP14	DP13	DP12	DP11	DP10	DP9	DP8
		W								
0x0012	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0013	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0014	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0015	PPAGE	R	0	0	0	0	PIX3	PIX2	PIX1	PIX0
		W								
			= Unimplemented or Reserved							

5.29.3.2 Register Descriptions

This section consists of the S12PMMC control register descriptions in address order.

5.29.3.2.1 Mode Register (MODE)

Table 249. Mode Register (MODE)

Address: 0x000B

	7	6	5	4	3	2	1	0
R	MODC	0	0	0	0	0	0	0
W								
Reset	MODC[168]	0	0	0	0	0	0	0
	= Unimplemented or Reserved							

Note:
168. External signal (see Table 247).

Read: Anytime.

Write: Only if a transition is allowed (see Figure 45).

The MODC bit of the MODE register is used to select the MCU's operating mode.

5.31.3.2.1 BDM Status Register (BDMSTS)

Register Global Address 0x3_FF01

Table 262. BDM Status Register (BDMSTS)

	7	6	5	4	3	2	1	0
R	ENBDM	BDMACT	0	SDV	TRACE	0	UNSEC	0
W								
Reset								
Special Single-Chip Mode	0(175)	1	0	0	0	0	0(176)	0
All Other Modes	0	0	0	0	0	0	0	0

= Unimplemented, Reserved

= Implemented (do not alter)

0 = Always read zero

Note:

175. ENBDM is read as 1 by a debugging environment in special single chip mode when the device is not secured or secured but fully erased (Flash). This is because the ENBDM bit is set by the standard BDM firmware before a BDM command can be fully transmitted and executed.

176. UNSEC is read as 1 by a debugging environment in special single chip mode when the device is secured and fully erased, else it is 0 and can only be read if not secure (see also bit description).

Read: All modes through BDM operation when not secured

Write: All modes through BDM operation when not secured, but subject to the following:

- ENBDM should only be set via a BDM hardware command if the BDM firmware commands are needed. (This does not apply in special single chip mode).
- BDMACT can only be set by BDM hardware upon entry into BDM. It can only be cleared by the standard BDM firmware lookup table upon exit from BDM active mode.
- All other bits, while writable via BDM hardware or standard BDM firmware write commands, should only be altered by the BDM hardware or standard firmware lookup table as part of BDM command execution.

Table 263. BDMSTS Field Descriptions

Field	Description
7 ENBDM	**Enable BDM** — This bit controls whether the BDM is enabled or disabled. When enabled, BDM can be made active to allow firmware commands to be executed. When disabled, BDM cannot be made active but BDM hardware commands are still allowed. 0 BDM disabled 1 BDM enabled Note: ENBDM is set out of reset in special single chip mode. In special single chip mode with the device secured, this bit will not be set until after the Flash erase verify tests are complete.
6 BDMACT	**BDM Active Status** — This bit becomes set upon entering BDM. The standard BDM firmware lookup table is then enabled and put into the memory map. BDMACT is cleared by a carefully timed store instruction in the standard BDM firmware as part of the exit sequence to return to user code and remove the BDM memory from the map. 0 BDM not active 1 BDM active
4 SDV	**Shift Data Valid** — This bit is set and cleared by the BDM hardware. It is set after data has been transmitted as part of a BDM firmware or hardware read command or after data has been received as part of a BDM firmware or hardware write command. It is cleared when the next BDM command has been received or BDM is exited. SDV is used by the standard BDM firmware to control program flow execution. 0 Data phase of command not complete 1 Data phase of command is complete

Table 270. Quick Reference to DBG Registers

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x002E	DBGADHM	R W	Bit 15	14	13	12	11	10	9	Bit 8
0x002F	DBGADLM	R W	Bit 7	6	5	4	3	2	1	Bit 0

Note:

184. This bit is visible at DBGCNT[7] and DBGSR[7]
185. This represents the contents if the Comparator A control register is blended into this address.
186. This represents the contents if the Comparator B control register is blended into this address.
187. This represents the contents if the Comparator C control register is blended into this address.

5.32.3.2 Register Descriptions

This section consists of the DBG control and trace buffer register descriptions in address order. Each comparator has a bank of registers that are visible through an 8-byte window between 0x0028 and 0x002F in the DBG module register address map. When ARM is set in DBGC1, the only bits in the DBG module registers that can be written are ARM, TRIG, and COMRV[1:0]

5.32.3.2.1 Debug Control Register 1 (DBGC1)

Table 271. Debug Control Register (DBGC1)

Address: 0x0020

	7	6	5	4	3	2	1	0
R	ARM	0	0	BDM	DBGBRK	0	COMRV	
W		TRIG						
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Read: Anytime

Write: Bits 7, 1, 0 anytime
Bit 6 can be written anytime but always reads back as 0.
Bits 4:3 anytime DBG is not armed.

NOTE

When disarming the DBG by clearing ARM with software, the contents of bits[4:3] are not affected by the write, since up until the write operation, ARM = 1 preventing these bits from being written. These bits must be cleared using a second write if required.

Table 294. State2 —Sequencer Next State Selection

SC[3:0]	Description (Unspecified matches have no effect)
0010	Match2 to State3
0011	Match1 to State3..... Match0 Final State
0100	Match1 to State1..... Match2 to State3.
0101	Match2 to Final State
0110	Match2 to State1..... Match0 to Final State
0111	Either Match0 or Match1 to Final State
1000	Reserved
1001	Reserved
1010	Reserved
1011	Reserved
1100	Either Match0 or Match1 to Final State.....Match2 to State3
1101	Reserved
1110	Reserved
1111	Either Match0 or Match1 to Final State.....Match2 to State1

The priorities described in Table 324 dictate that in the case of simultaneous matches, a match leading to final state has priority followed by the match on the lower channel number (0,1,2)

5.32.3.2.7.3 Debug State Control Register 3 (DBGSCR3)

Table 295. Debug State Control Register 3 (DBGSCR3)

Address: 0x0027

	7	6	5	4	3	2	1	0
R	0	0	0	0	SC3	SC2	SC1	SC0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Read: If COMRV[1:0] = 10

Write: If COMRV[1:0] = 10 and DBG is not armed.

This register is visible at 0x0027 only with COMRV[1:0] = 10. The state control register three selects the targeted next state whilst in State3. The matches refer to the match channels of the comparator match control logic as depicted in Figure 62 and described in Section 5.32.3.2.8.1, “Debug Comparator Control Register (DBGXCTL)". Comparators must be enabled by setting the comparator enable bit in the associated DBGXCTL control register.

Table 296. DBGSCR3 Field Descriptions

Field	Description
3–0 SC[3:0]	These bits select the targeted next state whilst in State3, based upon the match event.

Table 297. State3 — Sequencer Next State Selection

SC[3:0]	Description (Unspecified matches have no effect)
0000	Match0 to State1
0001	Match2 to State2..... Match1 to Final State
0010	Match0 to Final State..... Match1 to State1

5.35.0.2.2 Special Single Chip Mode (SS)

- BDM firmware commands are disabled.
- BDM hardware commands are restricted to the register space.
- Execution of Flash and EEPROM commands is restricted. Please refer to the NVM block guide for details.
- Tracing code execution using the DBG module is disabled.

Special single chip mode means BDM is active after reset. The availability of BDM firmware commands depends on the security state of the device. The BDM secure firmware first performs a blank check of both the Flash memory and the EEPROM. If the blank check succeeds, security will be temporarily turned off and the state of the security bits in the appropriate Flash memory location can be changed If the blank check fails, security will remain active, only the BDM hardware commands will be enabled, and the accessible memory space is restricted to the peripheral register area. This will allow the BDM to be used to erase the EEPROM and Flash memory without giving access to their contents. After erasing both Flash memory and EEPROM, another reset into special single chip mode will cause the blank check to succeed and the options/security byte can be programmed to “unsecured” state via BDM.

While the BDM is executing the blank check, the BDM interface is completely blocked, which means that all BDM commands are temporarily blocked.

5.35.0.2.3 Executing from Internal Memory in Expanded Mode

The user may choose to operate from internal memory while in expanded mode. To do this the user must start in single chip mode and write to the mode bits selecting expanded operation. In this mode internal visibility and IPIPE are blocked. If the users program tries to execute from outside the program memory space (internal space occupied by the FLASH), the FLASH and EEPROM will be disabled. BDM operations will be blocked.

If the user begins operation in single chip mode with security on, the user is constrained to operate out of internal memory - even if the user changes to expanded mode. To accomplish this the MMC needs to register that the part started in single chip mode and was secured. The CPU will provide the state of the two high-order bits of the Program Counter. All this information, plus the firmware size information is used to determine that the part is executing in the proper space. If the program strays, the selects for FLASH and EEPROM are disabled by the MMC until the part goes through reset.

5.35.0.2.4 Unsecuring the Microcontroller

Unsecuring the microcontroller can be done by three different methods:

1. Backdoor key access
2. Reprogramming the security bits
3. Complete memory erase (special modes)

5.35.0.2.5 Unsecuring the MCU Using the Backdoor Key Access

In normal modes (single chip and expanded), security can be temporarily disabled using the backdoor key access method. This method requires that:

- The backdoor key at 0xFF00–0xFF07 (= global addresses 0x7F_FF00–0x7F_FF07) has been programmed to a valid value.
- The KEYEN[1:0] bits within the Flash options/security byte select ‘enabled’.
- In single chip mode, the application program programmed into the microcontroller must be designed to have the capability to write to the backdoor key locations.

The backdoor key values themselves would not normally be stored within the application data, which means the application program would have to be designed to receive the backdoor key values from an external source (e.g. through a serial port).

The backdoor key access method allows debugging of a secured microcontroller without having to erase the Flash. This is particularly useful for failure analysis.

NOTE

No word of the backdoor key is allowed to have the value 0x0000 or 0xFFFF.

5.35.0.3 Reprogramming the Security Bits

In normal single chip mode (NS), security can also be disabled by erasing and reprogramming the security bits within Flash options/security byte to the unsecured value. Because the erase operation will erase the entire sector from 0xFE00–0xFFFF (0x7F_FE00–0x7F_FFFF), the backdoor key and the interrupt vectors will also be erased; this method is not recommended for normal single chip mode. The application software can only erase and program the Flash options/security byte if the Flash sector

Table 349. CPMUCLKS Descriptions

Field	Description
7 PLLSEL	**PLL Select Bit** This bit selects the PLLCLK as source of the System Clocks (Core Clock and Bus Clock). PLLSEL can only be set to 0, if UPOSC=1. UPOSC= 0 sets the PLLSEL bit. Entering Full Stop Mode sets the PLLSEL bit. 0 System clocks are derived from OSCCLK if oscillator is up (UPOSC=1, $f_{BUS} = f_{OSC} / 2$. 1 System clocks are derived from PLLCLK, $f_{BUS} = f_{PLL} / 2$.
6 PSTP	**Pseudo Stop Bit** This bit controls the functionality of the oscillator during Stop Mode. 0 Oscillator is disabled in Stop Mode (Full Stop Mode). 1 Oscillator continues to run in Stop Mode (Pseudo Stop Mode), option to run RTI and COP. Note: Pseudo Stop Mode allows for faster STOP recovery and reduces the mechanical stress and aging of the resonator in case of frequent STOP conditions at the expense of a slightly increased power consumption. Note: When starting up the external oscillator (either by programming OSCE bit to 1 or on exit from Full Stop Mode with OSCE bit is already 1) the software must wait for a minimum time equivalent to the startup-time of the external oscillator t_{UPOSC} before entering Pseudo Stop Mode.
3 PRE	**RTI Enable During Pseudo Stop Bit** — PRE enables the RTI during Pseudo Stop Mode. 0 RTI stops running during Pseudo Stop Mode. 1 RTI continues running during Pseudo Stop Mode if RTIOSCSEL=1. Note: If PRE=0 or RTIOSCSEL=0 then the RTI will go static while Stop Mode is active. The RTI counter will not be reset.
2 PCE	**COP Enable During Pseudo Stop Bit** — PCE enables the COP during Pseudo Stop Mode. 0 COP stops running during Pseudo Stop Mode 1 COP continues running during Pseudo Stop Mode if COPOSCSEL=1 Note: If PCE=0 or COPOSCSEL=0 then the COP will go static while Stop Mode is active. The COP counter will not be reset.
1 RTIOSCSEL	**RTI Clock Select** — RTIOSCSEL selects the clock source to the RTI. Either IRCCLK or OSCCLK. Changing the RTIOSCSEL bit re-starts the RTI timeout period. RTIOSCSEL can only be set to 1, if UPOSC=1. UPOSC= 0 clears the RTIOSCSEL bit. 0 RTI clock source is IRCCLK. 1 RTI clock source is OSCCLK.
0 COPOSCSEL	**COP Clock Select** — COPOSCSEL selects the clock source to the COP. Either IRCCLK or OSCCLK. Changing the COPOSCSEL bit re-starts the COP timeout period. COPOSCSEL can only be set to 1, if UPOSC=1. UPOSC= 0 clears the COPOSCSEL bit. 0 COP clock source is IRCCLK. 1 COP clock source is OSCCLK

5.38.3.2.7 S12CPMU PLL Control Register (CPMUPLL)

This register controls the PLL functionality.

Table 350. S12CPMU PLL Control Register (CPMUPLL)

0x003A

	7	6	5	4	3	2	1	0
R	0	0	FM1	FM0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

Read: Anytime

Write: Anytime if PROT=0 (CPMUPROT register) and PLLSEL=1 (CPMUCLKS register). Else write has no effect.

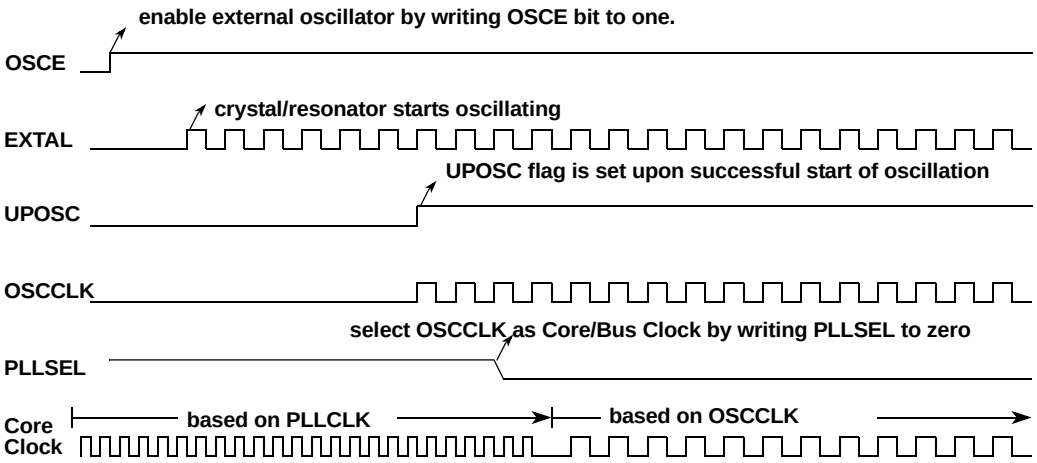


Figure 90. Enabling the External Oscillator

5.38.4.5.2 The Adaptive Oscillator Filter

A spike in the oscillator clock can disturb the function of the modules driven by this clock.

The Adaptive Oscillator Filter includes two features:

1. Filter noise (spikes) from the incoming external oscillator clock. The filter feature is illustrated in Figure 91.

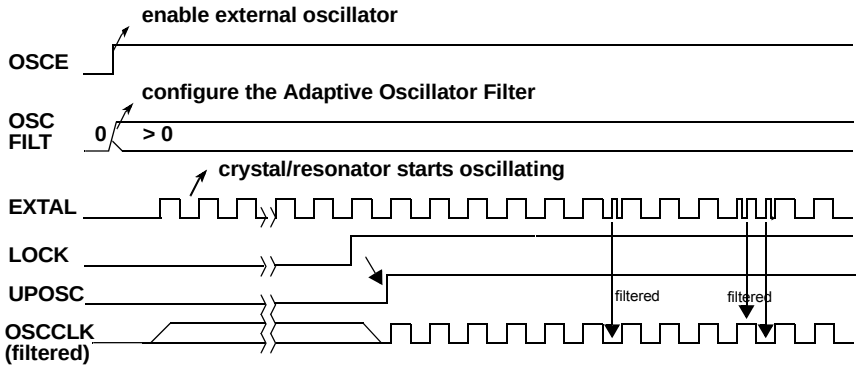


Figure 91. Noise Filtered by the Adaptive Oscillator Filter

2. Detect severe noise disturbance on external oscillator clock which can not be filtered and indicate the critical situation to the software by clearing the UPOSC and LOCK status bit and setting the OSCIF and LOCKIF flag. An example for the detection of critical noise is illustrated in Figure 92

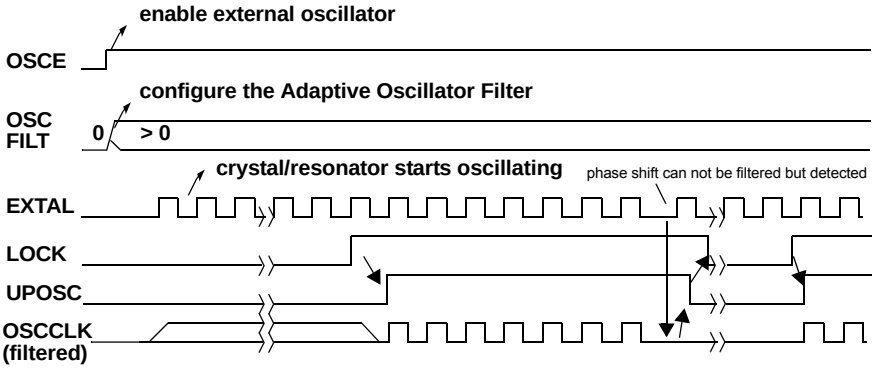


Figure 92. Critical Noise Detected by the Adaptive Oscillator Filter

If the CPHA bit in SPI control register 1 is clear, odd numbered edges on the SCK input cause the data at the serial data input pin to be latched. Even numbered edges cause the value previously latched from the serial data input pin to shift into the LSB or MSB of the SPI shift register, depending on the LSBFE bit.

If the CPHA bit is set, even numbered edges on the SCK input cause the data at the serial data input pin to be latched. Odd numbered edges cause the value previously latched from the serial data input pin to shift into the LSB or MSB of the SPI shift register, depending on the LSBFE bit.

When CPHA is set, the first edge is used to get the first data bit onto the serial data output pin. When CPHA is clear and the $\overline{SS}$ input is low (slave selected), the first bit of the SPI data is driven out of the serial data output pin. After the nth[209] shift, the transfer is considered complete and the received data is transferred into the SPI data register. To indicate transfer is complete, the SPIF flag in the SPI status register is set.

Note:

209. n depends on the selected transfer width, refer to Section 5.39.3.2.2, “SPI Control Register 2 (SPICR2)"

NOTE

A change of the bits CPOL, CPHA, SSOE, LSBFE, MODFEN, SPC0, or BIDIROE with SPC0 set in slave mode will corrupt a transmission in progress and must be avoided.

5.39.4.3 Transmission Formats

During an SPI transmission, data is transmitted (shifted out serially) and received (shifted in serially) simultaneously. The serial clock (SCK) synchronizes shifting and sampling of the information on the two serial data lines. A slave select line allows selection of an individual slave SPI device; slave devices that are not selected do not interfere with SPI bus activities. Optionally, on a master SPI device, the slave select line can be used to indicate multiple-master bus contention.

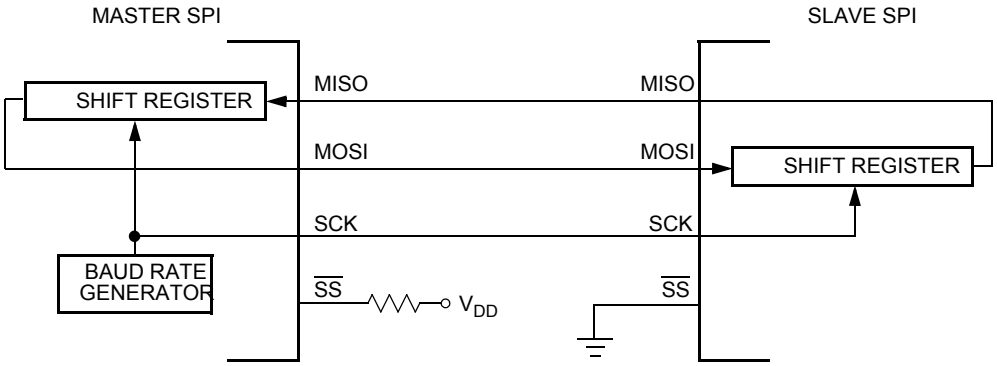


Figure 99. Master/Slave Transfer Block Diagram

5.39.4.3.1 Clock Phase and Polarity Controls

Using two bits in the SPI control register 1, software selects one of four combinations of serial clock phase and polarity.

The CPOL clock polarity control bit specifies an active high or low clock and has no significant effect on the transmission format.

The CPHA clock phase control bit selects one of two fundamentally different transmission formats.

Clock phase and polarity should be identical for the master SPI device and the communicating slave device. In some cases, the phase and polarity are changed between transmissions to allow a master device to communicate with peripheral slaves having different requirements.

5.39.4.3.2 CPHA = 0 Transfer Format

The first edge on the SCK line is used to clock the first data bit of the slave into the master and the first data bit of the master into the slave. In some peripherals, the first bit of the slave’s data is available at the slave’s data out pin as soon as the slave is selected. In this format, the first SCK edge is issued a half cycle after $\overline{SS}$ has become low.

A half SCK cycle later, the second edge appears on the SCK line. When this second edge occurs, the value previously latched from the serial data input pin is shifted into the LSB or MSB of the shift register, depending on LSBFE bit.

After this second edge, the next bit of the SPI master data is transmitted out of the serial data output pin of the master to the serial input pin on the slave. This process continues for a total of 16 edges on the SCK line, with data being latched on odd numbered edges and shifted on even numbered edges.

5.40.3.2.5 Flash Configuration Register (FCNFG)

The FCNFG register enables the Flash command complete interrupt and forces ECC faults on Flash array read access from the CPU.

Table 425. Flash Configuration Register (FCNFG)

	7	6	5	4	3	2	1	0
R	CCIE	0	0	IGNSF	0	0	FDFD	FSFD
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

CCIE, IGNSF, FDFD, and FSFD bits are readable and writable while remaining bits read 0 and are not writable.

Table 426. FCNFG Field Descriptions

Field	Description
7 CCIE	**Command Complete Interrupt Enable** — The CCIE bit controls interrupt generation when a Flash command has completed. 0 Command complete interrupt disabled 1 An interrupt will be requested whenever the CCIF flag in the FSTAT register is set (see Section 5.40.3.2.7, “Flash Status Register (FSTAT)")
4 IGNSF	**Ignore Single Bit Fault** — The IGNSF controls single bit fault reporting in the FERSTAT register (see Section 5.40.3.2.8, “Flash Error Status Register (FERSTAT)"). 0 All single bit faults detected during array reads are reported 1 Single bit faults detected during array reads are not reported and the single bit fault interrupt will not be generated
1 FDFD	**Force Double Bit Fault Detect** — The FDFD bit allows the user to simulate a double bit fault during Flash array read operations and check the associated interrupt routine. The FDFD bit is cleared by writing a 0 to FDFD. The FECCR registers will not be updated during the Flash array read operation with FDFD set unless an actual double bit fault is detected. 0 Flash array read operations will set the DFDIF flag in the FERSTAT register only if a double bit fault is detected 1 Any Flash array read operation will force the DFDIF flag in the FERSTAT register to be set (see Section 5.40.3.2.7, “Flash Status Register (FSTAT)") and an interrupt will be generated as long as the DFDIE interrupt enable in the FERCNFG register is set (see Section 5.40.3.2.6, “Flash Error Configuration Register (FERCNFG)")
0 FSFD	**Force Single Bit Fault Detect** — The FSFD bit allows the user to simulate a single bit fault during Flash array read operations and check the associated interrupt routine. The FSFD bit is cleared by writing a 0 to FSFD. The FECCR registers will not be updated during the Flash array read operation with FSFD set unless an actual single bit fault is detected. 0 Flash array read operations will set the SFDIF flag in the FERSTAT register only if a single bit fault is detected 1 Flash array read operation will force the SFDIF flag in the FERSTAT register to be set (see Section 5.40.3.2.7, “Flash Status Register (FSTAT)") and an interrupt will be generated as long as the SFDIE interrupt enable in the FERCNFG register is set (see Section 5.40.3.2.6, “Flash Error Configuration Register (FERCNFG)")

5.40.3.2.6 Flash Error Configuration Register (FERCNFG)

The FERCNFG register enables the Flash error interrupts for the FERSTAT flags.

Table 427. Flash Error Configuration Register (FERCNFG)

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	DFDIE	SFDIE
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

All assigned bits in the FERCNFG register are readable and writable.

Table 480. Verify Backdoor Access Key Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x0C	Not required
001	Key 0	
010	Key 1	
011	Key 2	
100	Key 3	

Upon clearing CCIF to launch the Verify Backdoor Access Key command, the Memory Controller will check the FSEC KEYEN bits to verify that this command is enabled. If not enabled, the Memory Controller sets the ACCERR bit in the FSTAT register and terminates. If the command is enabled, the Memory Controller compares the key provided in FCCOB to the backdoor comparison key in the Flash configuration field with Key 0 compared to 0x3_FF00, etc. If the backdoor keys match, security will be released. If the backdoor keys do not match, security is not released and all future attempts to execute the Verify Backdoor Access Key command are aborted (set ACCERR) until a reset occurs. The CCIF flag is set after the Verify Backdoor Access Key operation has completed.

Table 481. Verify Backdoor Access Key Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 100 at command launch
		Set if an incorrect backdoor key is supplied
		Set if backdoor key access has not been enabled (KEYEN[1:0] != 10, see Section 5.40.3.2.2, “Flash Security Register (FSEC)")
		Set if the backdoor key has mismatched since the last reset
	FPVIOL	None
	MGSTAT1	None
	MGSTAT0	None

5.40.4.5.12 Set User Margin Level Command

The Set User Margin Level command causes the Memory Controller to set the margin level for future read operations of the P-Flash or D-Flash block.

Table 482. Set User Margin Level Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x0D	Global address [17:16] to identify the Flash block
001	Margin level setting	

Upon clearing CCIF to launch the Set User Margin Level command, the Memory Controller will set the user margin level for the targeted block and then set the CCIF flag.

NOTE

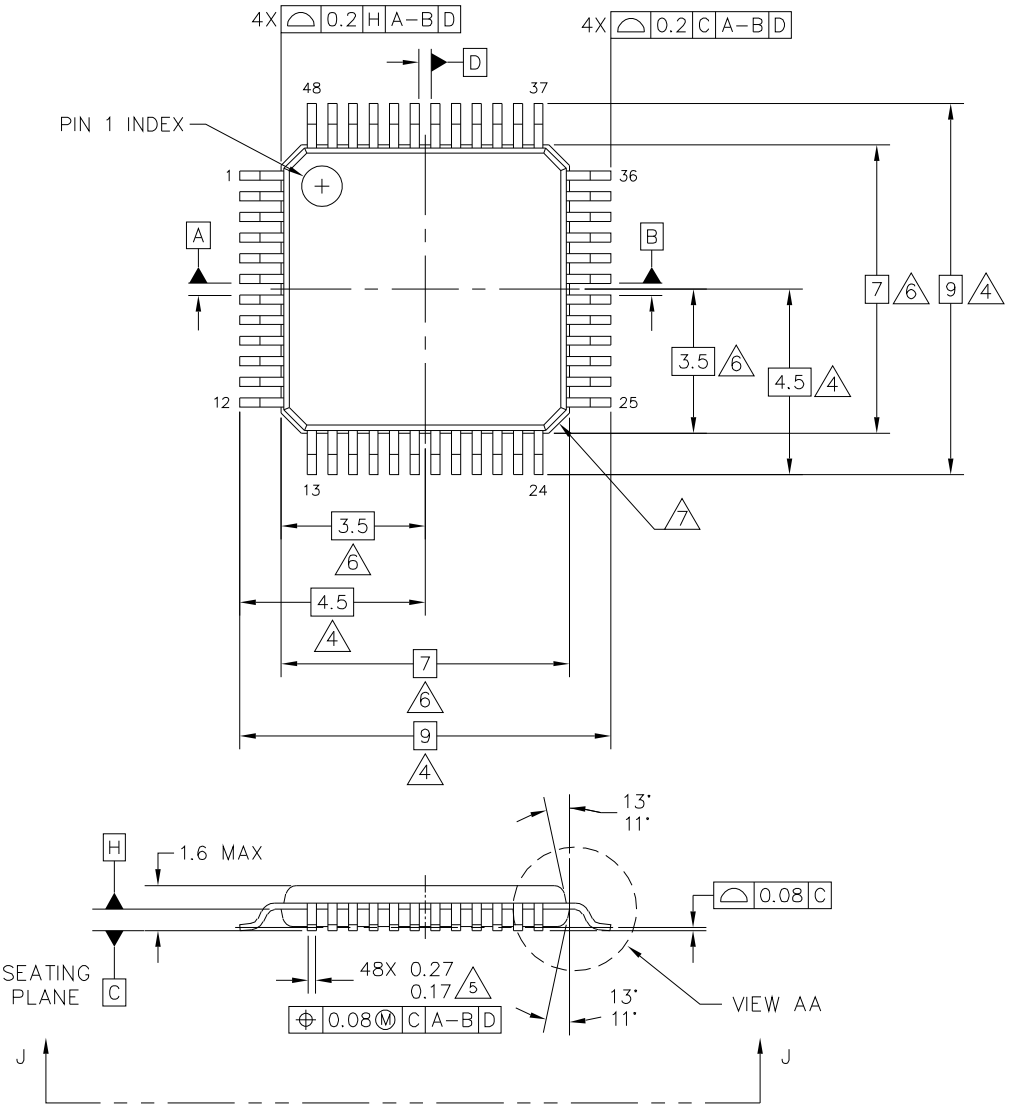
When the D-Flash block is targeted, the D-Flash user margin levels are applied only to the D-Flash reads. However, when the P-Flash block is targeted, the P-Flash user margin levels are applied to both P-Flash and D-Flash reads. It is not possible to apply user margin levels to the P-Flash block only.

Valid margin level settings for the Set User Margin Level command are defined in Table 483.

6 Packaging

6.1 Package Dimensions

For the most current package revision, visit **www.freescale.com** and perform a keyword search using the “98A” listed below.



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TITLE: 48 LEAD LQFP, 7X7X1.4 PKG, 0.5 PITCH, 4.5X4.5 EXPOSED PAD	DOCUMENT NO: 98ASA00173D	REV: O
	CASE NUMBER: 2003-01	01 DEC 2009
	STANDARD: JEDEC MS-026 BBC	

AE SUFFIX
48-PIN
LQFP48
REVISION 0