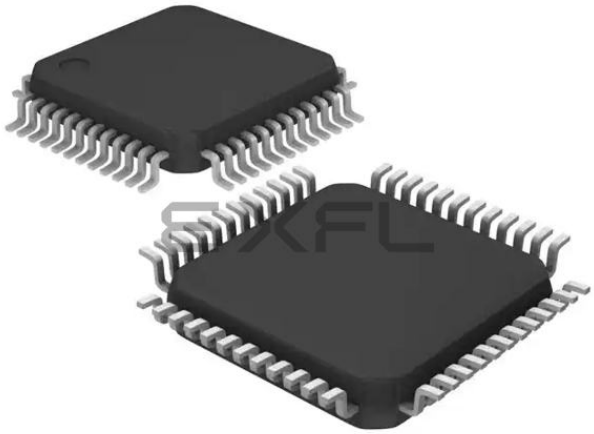

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Details	
Product Status	Obsolete
Applications	Automotive
Core Processor	S12
Program Memory Type	FLASH (48kB)
Controller Series	HCS12
RAM Size	2K x 8
Interface	LIN, SCI
Number of I/O	9
Voltage - Supply	2.25V ~ 5.25V
Operating Temperature	-40°C ~ 105°C
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mm912g634cv2apr2

Table 35. Dynamic Electrical Characteristics - Low Side Drivers - LS

Ratings	Symbol	Min	Typ	Max	Unit
Low Side Operating Frequency	f_{LS}	-	-	10	kHz

Table 36. Dynamic Electrical Characteristics - LIN Physical Layer Interface - LIN

Ratings	Symbol	Min	Typ	Max	Unit
Bus Wake-up Deglitcher (Sleep and Stop mode)	t_{PROPWL}	60	80	100	µs
Fast Bit Rate (Programming mode)	BR_{FAST}	-	-	100	kBit/s
Propagation Delay of Receiver, t_{REC_PD} = MAX (t_{REC_PDR}, t_{REC_PDF})	t_{REC_PD}	-	-	6.0	µs
Symmetry of Receiver Propagation Delay, t_{REC_PDF} - t_{REC_PDR}	t_{REC_SYM}	-2.0	-	2.0	µs
LIN Driver - 20.0 kBit/s; Bus load conditions (C_{BUS}; R_{BUS}): 1.0 nF; 1.0 kΩ / 6,8 nF;660 Ω / 10 nF;500 Ω. Measurement thresholds: 50% of TXD signal to LIN signal threshold defined at each parameter. See Figure 5 and Figure 6.					
Duty Cycle 1: $TH_{REC(MAX)}$ = 0.744 x V_{SUP} $TH_{DOM(MAX)}$ = 0.581 x V_{SUP} 7.0 V ≤ V_{SUP} ≤ 18 V; t_{Bit} = 50 µs; D1 = $t_{BUS\_REC(MIN)}$/(2 x t_{Bit})	D1	0.396	-	-	
Duty Cycle 2: $TH_{REC(MIN)}$ = 0.422 x V_{SUP} $TH_{DOM(MIN)}$ = 0.284 x V_{SUP} 7.6 V ≤ V_{SUP} ≤ 18 V; t_{BIT} = 50 µs D2 = $t_{BUS\_REC(MAX)}$/(2 x t_{BIT})	D2	-	-	0.581	
LIN Driver - 10.0 kBit/s; Bus load conditions (C_{BUS}; R_{BUS}): 1.0 nF; 1.0 kΩ / 6,8 nF;660 Ω / 10 nF;500 Ω. Measurement thresholds: 50% of TXD signal to LIN signal threshold defined at each parameter. See Figure 5 and Figure 7.					
Duty Cycle 3: $TH_{REC(MAX)}$ = 0.778 x V_{SUP} $TH_{DOM(MAX)}$ = 0.616 x V_{SUP} 7.0 V ≤ V_{SUP} ≤ 18 V; t_{BIT} = 96 µs D3 = $T_{BUS\_REC(MIN)}$/(2 x t_{BIT})	D3	0.417	-	-	
Duty Cycle 4: $TH_{REC(MIN)}$ = 0.389 x V_{SUP} $TH_{DOM(MIN)}$ = 0.251 x V_{SUP} 7.6 V ≤ V_{SUP} ≤ 18 V; t_{BIT} = 96 µs D4 = $t_{BUS\_REC(MAX)}$/(2 x t_{BIT})	D4	-	-	0.590	
LIN Transmitter Timing, (V_{SUP} from 7.0 to 18 V) - See Figure 9					
Transmitter Symmetry ttran_sym < MAX(ttran_sym60%, ttran_sym40%) tran_sym60% = ttran_pdf60% - ttran_pdr60% tran_sym40% = ttran_pdf40% - ttran_pdr40%	ttran_sym	-7.25	0	7.25	µs

4.6.2.4 Electrical Characteristics for the Oscillator (OSCLCP)

Table 43. OSCLCP Characteristics

Rating	Symbol	Min	Typ	Max	Unit
Crystal Oscillator Range	f_{OSC}	4.0	—	16	MHz
Startup Current	i_{OSC}	100	—	—	μA
Oscillator Start-up time (LCP, 4MHz)(54)	t_{UPOSC}	—	2.0	10	ms
Oscillator Start-up time (LCP, 8MHz)(54)	t_{UPOSC}	—	1.6	8.0	ms
Oscillator Start-up time (LCP, 16MHz)(54)	t_{UPOSC}	—	1.0	5.0	ms
Clock Monitor Failure Assert Frequency	f_{CMFA}	200	450	1200	KHz
Input Capacitance (EXTAL, XTAL pins)	C_{IN}	—	7.0	—	pF
EXTAL Pin Input Hysteresis	$V_{HYS,EXTAL}$	—	120	—	mV
EXTAL Pin Oscillation Amplitude (loop controlled Pierce)	$V_{PP,EXTAL}$	—	0.9	—	V

Note:
54. These values apply for carefully designed PCB layouts with capacitors that match the crystal/resonator requirements.
55. Only applies if EXTAL is externally driven.

4.6.2.5 Reset Characteristics

Table 44. Reset and Stop Characteristics

Rating	Symbol	Min	Typ	Max	Unit
Reset Input Pulse Width, Minimum Input Time	PW_{RSTL}	2.0	—	—	t_{VCORST}
Startup from Reset	n_{RST}	—	768	—	t_{VCORST}
STOP Recovery Time	t_{STP_REC}	—	50	—	μs

4.6.2.6 SPI Timing

This section provides electrical parametrics and ratings for the SPI. In Table 45 the measurement conditions are listed.

Table 45. Measurement Conditions

Description	Value	Unit
Drive mode	Full drive mode	—
Load capacitance C_{LOAD}(56), on all outputs	50	pF
Thresholds for delay measurement points	(20% / 80%) V_{DDRX}	V

Note:
56. Timing specified for equal load on all SPI output pins. Avoid asymmetric load.

4.6.2.6.1 Master Mode

In Figure 12 the timing diagram for master mode with transmission format CPHA = 0 is depicted.

Table 73. 0x0200–0x03FF Die-To-Die Initiator Blocking and Non-Blocking Access Window

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0200-0x02FF	Blocking Access Window	R								
		W								
0x0300-0x03FF	Non-Blocking Access Window	R								
		W								

Table 74 shows the detailed module maps of the MM912_634 analog die.

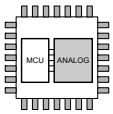
Table 74. Analog die Registers(63) - 0x0200–0x02FF D2D Blocking Access (D2DI) 2 of 3/ 0x0300–0x03FF D2D Non Blocking Access (D2DI) 3 of 3

Offset	Name		7	6	5	4	3	2	1	0
0x00	ISR (hi)	R	0	0	HOT	LSOT	HSOT	LINOT	SCI	RX
	Interrupt Source Register	W								
0x01	ISR (lo)	R	TX	ERR	TOV	CH3	CH2	CH1	CH0	VSI
	Interrupt Source Register	W								
0x02	IVR	R	0	0	IRQ					
	Interrupt Vector Register	W								
0x04	VCR	R	0	0	0	VROVIE	HTIE	HVIE	LVIE	LBIE
	Voltage Control Register	W								
0x05	VSR	R	0	0	0	VROVC	HTC	HVC	LVC	LBC
	Voltage Status Register	W								
0x08	LXR	R	0	0	L5	L4	L3	L2	L1	L0
	Lx Status Register	W								
0x09	LXCR	R	0	0	L5DS	L4DS	L3DS	L2DS	L1DS	L0DS
	Lx Control Register	W								
0x10	WDR	R	WDOFF	WDWO	0	0	0	WDTO		
	Watchdog Register	W								
0x11	WDSR	R	WDSR							
	Watchdog Service Register	W								
0x12	WCR	R	CSSEL		L5WE	L4WE	L3WE	L2WE	L1WE	L0WE
	Wake Up Control Register	W								
0x13	TCR	R	FWM				CST			
	Timing Control Register	W								
0x14	WSR	R	FWU	LINWU	L5WU	L4WU	L3WU	L2WU	L1WU	L0WU
	Wake Up Source Register	W								
0x15	RSR	R	0	0	WDR	EXR	WUR	LVRX	LVR	POR
	Reset Status Register	W								
0x16	MCR	R	0	0	0	0	0	0	MODE	
	Mode Control Register	W								
0x18	LINR	R	LINOTIE	LINOTC	RX	TX	LVSD	LINEN	LINSR	
	LIN Register	W								
0x20	PTBC1	R	0	PUEB2	PUEB1	PUEB0	0	DDRB2	DDRB1	DDRB0
	Port B Configuration Register 1	W								

Table 74. Analog die Registers[63] - 0x0200–0x02FF D2D Blocking Access (D2DI) 2 of 3/ 0x0300–0x03FF D2D Non Blocking Access (D2DI) 3 of 3

Offset	Name		7	6	5	4	3	2	1	0
0xA5	ADR15 (lo)	R	adr15 1	adr15 0	0	0	0	0	0	0
	ADC Data Result Reg 15	W								
0xC0	TIOS	R	0	0	0	0	IOS3	IOS2	IOS1	IOS0
	TIM InCap/OutComp Select	W								
0xC1	CFORC	R	0	0	0	0	0	0	0	0
	Timer Compare Force Reg	W					FOC3	FOC2	FOC1	FOC0
0xC2	OC3M	R	0	0	0	0	OC3M3	OC3M2	OC3M1	OC3M0
	Output Comp 3 Mask Reg	W								
0xC3	OC3D	R	0	0	0	0	OC3D3	OC3D2	OC3D1	OC3D0
	Output Comp 3 Data Reg	W								
0xC4	TCNT (hi)	R	tcnt 15	tcnt 14	tcnt 13	tcnt 12	tcnt 11	tcnt 10	tcnt 9	tcnt 8
	Timer Count Register	W								
0xC5	TCNT (lo)	R	tcnt 7	tcnt 6	tcnt 5	tcnt 4	tcnt 3	tcnt 2	tcnt 1	tcnt 0
	Timer Count Register	W								
0xC6	TSCR1	R	TEN	0	0	TFFCA	0	0	0	0
	Timer System Control Reg 1	W								
0xC7	TTOV	R	0	0	0	0	TOV3	TOV2	TOV1	TOV0
	Timer Toggle Overflow Reg	W								
0xC8	TCTL1	R	OM3	OL3	OM2	OL2	OM1	OL1	OM0	OL0
	Timer Control Register 1	W								
0xC9	TCTL2	R	EDG3B	EDG3A	EDG2B	EDG2A	EDG1B	EDG1A	EDG0B	EDG0A
	Timer Control Register 2	W								
0xCA	TIE	R	0	0	0	0	C3I	C2I	C1I	C0I
	Timer Interrupt Enable Reg	W								
0xCB	TSCR2	R	TOI	0	0	0	TCRE	PR2	PR1	PR0
	Timer System Control Reg 2	W								
0xCC	TFLG1	R	0	0	0	0	C3F	C2F	C1F	C0F
	Main Timer Interrupt Flag 1	W								
0xCD	TFLG2	R	TOF	0	0	0	0	0	0	0
	Main Timer Interrupt Flag 2	W								
0xCE	TC0 (hi)	R	tc0 15	tc0 14	tc0 13	tc0 12	tc0 11	tc0 10	tc0 9	tc0 8
	TIM InCap/OutComp Reg 0	W								
0xCF	TC0 (lo)	R	tc0 7	tc0 6	tc0 5	tc0 4	tc0 3	tc0 2	tc0 1	tc0 0
	TIM InCap/OutComp Reg 0	W								
0xD0	TC1 (hi)	R	tc1 15	tc1 14	tc1 13	tc1 12	tc1 11	tc1 10	tc1 9	tc1 8
	TIM InCap/OutComp Reg 1	W								
0xD1	TC1 (lo)	R	tc1 7	tc1 6	tc1 5	tc1 4	tc1 3	tc1 2	tc1 1	tc1 0
	TIM InCap/OutComp Reg 1	W								
0xD2	TC2 (hi)	R	tc2 15	tc2 14	tc2 13	tc2 12	tc2 11	tc2 10	tc2 9	tc2 8
	TIM InCap/OutComp Reg 2	W								
0xD3	TC2 (lo)	R	tc2 7	tc2 6	tc2 5	tc2 4	tc2 3	tc2 2	tc2 1	tc2 0
	TIM InCap/OutComp Reg 2	W								

5.3 MM912_634 - Analog Die Overview



5.3.1 Introduction

The MM912_634 analog die implements all system base functionality to operate the integrated microcontroller, and delivers application specific actuator control as well as input capturing.

5.3.2 System Registers

5.3.2.1 Silicon Revision Register (SRR)

Table 75. Silicon Revision Register (SRR)

Offset[64] 0xF4 — Access: User read

	7	6	5	4	3	2	1	0
R	0	0	0	0	FMREV		MMREV	
W								

Note:
64. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 76. SRR - Register Field Descriptions

Field	Description
3-2 FMREV	MM912F634 analog die Silicon Revision Register - These bits represent the revision of Silicon of the analog die. They are incremented for every full mask or metal mask issued of the device. One number is set for one revision of the silicon of the analog die.
1-0 MMREV	

NOTE

Please refer to the MM912F634ER - Mask set errata document for details on the analog die mask revisions.

5.3.3 Analog Die Options

The following section describes the differences between analog die options 1 and 2.

Table 77. Analog Die Options

Feature	Option 1	Option 2
Current Sense Module	YES	NO
Wake Up Inputs (Lx)	L0…L5	L0.L3

NOTE

This document will describe the features and functions of option 1 (all modules available and tested). Beyond this chapter, there will be no additional note or differentiation between the different implementations.

The Reset Status Register (RSR) will indicate the source of the reset by individual flags.

- POR - Power On Reset
- LVR - Low Voltage Reset VDD
- LVRX - Low Voltage Reset VDDX
- WDR - Watchdog Reset
- EXR - External Reset
- WUR - Wake-up Sleep Reset

See also Section 5.8, “Resets".

5.4.3 Normal Mode

In Normal mode, all MM912_634 analog die user functions are active and can be controlled by the D2D Interface. Both regulators (VDD and VDDX) are active and operate with full current capability.

Once entered in Normal mode, the Watchdog will operate as a simple non-window watchdog with an initial timeout (tIWDTO) to be reset via the D2D Interface. After the initial reset, the watchdog will operate in standard window mode. See Section 5.10, “Window Watchdog" for details.

5.4.4 Stop Mode

The Stop mode will allow reduced current consumption with fast startup time. In this mode, both voltage regulators (VDD and VDDX) are active, with limited current drive capability. In this condition, the MCU is supposed to operate in Low Power mode (STOP).

NOTE

To avoid any pending analog die interrupts prevent the MCU from entering MCU stop resulting in unexpected system behavior, the analog die IRQ sources should be disabled and the corresponding flags be cleared before entering stop.

The device can enter in Stop mode by configuring the Mode Control Register (MCR) via the D2D Interface. The MCU has to enter a Low Power mode immediately afterwards executing the STOP instruction. The Wake-up Source Register (WSR) has to be read after a wake-up condition in order to execute a new STOP mode command. Two base clock cycles (fBASE) delay are required between WSR read and MCR write.

While in Stop mode, the MM912_634 analog die will wake up on the following sources:

- Lx - Wake-up (maskable with selectable cyclic sense)
- Forced Wake-up (configurable timeout)
- LIN Wake-up
- D2D Wake-up (special command)

After Wake-up from the sources listed above, the device will transit to Normal mode.

Reset will wake up the device directly to Reset mode.

See Section 5.9, “Wake-up / Cyclic Sense" for details.

5.4.5 Sleep Mode

The Sleep mode will allow very low current consumption. In this mode, both voltage regulators (VDD and VDDX) are inactive.

The device can enter into Sleep mode by configuring the Mode Control Register (MCR) via the D2D- Interface. During Sleep mode, all unused internal blocks are deactivated to allow the lowest possible consumption. Power consumption will decrease further if the Cyclic Sense or Forced Wake-up feature are disabled. While in Sleep mode, the MM912_634 analog die will wake up on the following sources:

- Lx - Wake-up (maskable with selectable cyclic sense)
- Forced Wake-up (configurable timeout)
- LIN Wake-up

After Wake-up from the sources listed above or a reset condition, the device will transit to Reset mode.

See Section 5.9, “Wake-up / Cyclic Sense" for details.

5.14 PWM Control Module (PWM8B2C)

5.14.1 Introduction

To control the High Side (HS1, HS2) and the Low Side (LS1, LS2) duty cycle as well as the PTB2 output, the PWM module is implemented. Refer to the individual driver section for details on the use of the internal PWM1 and PWM0 signal (Section 5.12, “High Side Drivers - HS", Section 5.13, “Low Side Drivers - LSx" and Section 5.18, “General Purpose I/O - PTB[0…2]")

The PWM definition is based on the HC12 PWM definitions with some of the simplifications incorporated. The PWM module has two channels with independent controls of left and center aligned outputs on each channel.

Each of the two channels has a programmable period and duty cycle as well as a dedicated counter. A flexible clock select scheme allows a total of four different clock sources to be used with the counters. Each of the modulators can create independent continuous waveforms with software-selectable duty rates from 0% to 100%.

5.14.1.1 Features

The PWM block includes these distinctive features:

- Two independent PWM channels with programmable periods and duty cycles
- Dedicated counter for each PWM channel
- Programmable PWM enable/disable for each channel
- Software selection of PWM duty pulse polarity for each channel
- Period and duty cycle are double buffered. Change takes effect when the end of the effective period is reached (PWM counter reaches zero), or when the channel is disabled
- Programmable center or left aligned outputs on individual channels
- Four clock sources (A, B, SA, and SB) provide for a wide range of frequencies
- Programmable clock select logic

5.14.1.2 Modes of Operation

The PWM8B2C module does operate in Normal mode only.

5.14.1.3 Block Diagram

Figure 22 shows the block diagram for the 8-bit 2-channel PWM block.

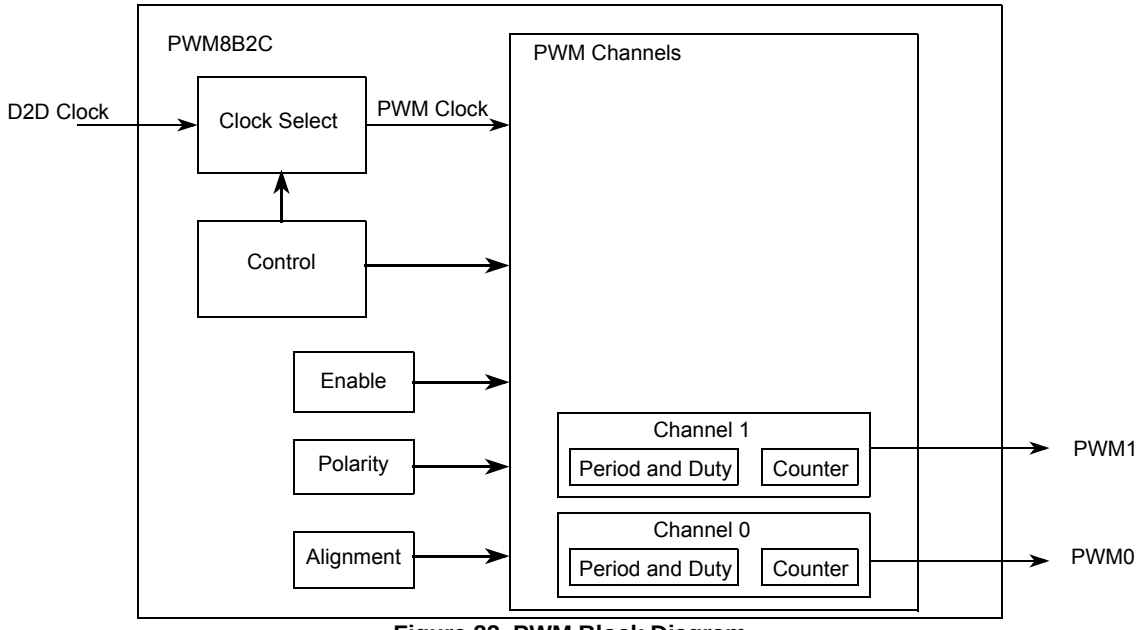


Figure 22. PWM Block Diagram

Table 129. PWM Channel Duty Registers (PWMDTYx)

Offset[96] 0x68/0x69 Access: User read/write

	7	6	5	4	3	2	1	0
R W	Bit 7	6	5	4	3	2	1	Bit 0
Reset	0	0	0	0	0	0	0	0

Note:

96. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

5.14.4 Functional Description

5.14.4.1 PWM Clock Select

There are four available clocks: clock A, clock B, clock SA (scaled A), and clock SB (scaled B). These four clocks are based on the D2D clock.

Clock A and B can be software selected to be 1, 1/2, 1/4, 1/8,..., 1/64, 1/128 times the D2D clock. Clock SA uses clock A as an input and divides it further with a reloadable counter. Similarly, clock SB uses clock B as an input and divides it further with a reloadable counter. The rates available for clock SA are software selectable to be clock A divided by 2, 4, 6, 8,..., or 512 in increments of divide by 2. Similar rates are available for clock SB. Each PWM channel has the capability of selecting one of two clocks, either the pre-scaled clock (clock A or B) or the scaled clock (clock SA or SB).

The block diagram in Figure 23 shows the four different clocks and how the scaled clocks are created.

5.14.4.1.1 Prescale

The input clock to the PWM prescaler is the D2D clock. The input clock can also be disabled when both PWM channels are disabled (PWME1-0 = 0). This is useful for reducing power by disabling the prescale counter.

Clock A and clock B are scaled values of the input clock. The value is software selectable for both clock A and clock B and has options of 1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, or 1/128 times the D2D clock. The value selected for clock A is determined by the PCKA2, PCKA1, PCKA0 bits in the PWMPRCLK register. The value selected for clock B is determined by the PCKB2, PCKB1, PCKB0 bits also in the PWMPRCLK register.

5.14.4.1.2 Clock Scale

The scaled A clock uses clock A as an input and divides it further with a user programmable value and then divides this by 2. The scaled B clock uses clock B as an input and divides it further with a user programmable value and then divides this by 2. The rates available for clock SA are software selectable to be clock A divided by 2, 4, 6, 8,..., or 512 in increments of divide by 2. Similar rates are available for clock SB.

NOTE

Clock SA = Clock A / (2 * PWMSCLA)

When PWMSCLA = $00, PWMSCLA value is considered a full scale value of 256. Clock A is thus divided by 512.

Similarly, clock B is used as an input to an 8-bit down counter followed by a divide by two producing clock SB. Thus, clock SB equals clock B divided by two times the value in the PWMSCLB register.

NOTE

Clock SB = Clock B / (2 * PWMSCLB)

When PWMSCLB = $00, PWMSCLB value is considered a full scale value of 256. Clock B is thus divided by 512.

As an example, consider the case in which the user writes $FF into the PWMSCLA register. Clock A for this case will be E divided by 4. A pulse will occur at a rate of once every 255x4 E cycles. Passing this through the divide by two circuit produces a clock signal at an E divided by 2040 rate. Similarly, a value of $01 in the PWMSCLA register when clock A is E divided by 4 will produce a clock at an E divided by 8 rate.

Writing to PWMSCLA or PWMSCLB causes the associated 8-bit down counter to be re-loaded. Otherwise, when changing rates the counter would have to count down to $01 before counting at the proper rate. Forcing the associated counter to re-load the scale register value every time PWMSCLA or PWMSCLB is written prevents this.

NOTE

Writing to the scale registers while channels are operating can cause irregularities in the PWM outputs.

5.14.4.1.3 Clock Select

Each PWM channel has the capability of selecting one of two clocks. For channels 0 the clock choice is clock A or clock SA. For channels 1 the choice is clock B or clock SB. The clock selection is done with the PCLKx control bits in the PWMCTL register.

NOTE

Changing clock control bits while channels are operating can cause irregularities in the PWM outputs.

5.14.4.2 PWM Channel Timers

The main part of the PWM module are the actual timers. Each of the timer channels has a counter, a period register, and a duty register (each are 8-bit). The waveform output period is controlled by a match between the period register and the value in the counter. The duty is controlled by a match between the duty register and the counter value, and causes the state of the output to change during the period. The starting polarity of the output is also selectable on a per channel basis. Shown in Figure 24 is the block diagram for the PWM timer.

5.15.6 Register Definition

5.15.6.1 LIN Register (LINR)

Table 132. LIN Register (LINR)

Offset[98] 0x18 Access: User read

	7	6	5	4	3	2	1	0
R	LINOTIE	LINOTC	RX	TX	LVSD	LINEN	LINSR	
W								
Reset	0	0	0	0	0	0	0	0

Note:
98. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 133. LINR - Register Field Descriptions

Field	Description
7 - LINOTIE	LIN - Over-temperature Interrupt Enable
6 - LINOTC	LIN - Over-temperature condition present. LIN driver is shut down. Reading this bit will clear the LINOT interrupt flag.
5 - RX	LIN - Receiver (Rx) Status. 0 - LIN Bus Dominant 1 - LIN Bus Recessive
4 - TX	LIN - Direct Transmitter Control. The inverted signal is OR 0 - Transmitter not controlled 1 - Transmitter Dominant
3 - LVSD	LIN - Low Voltage Shutdown Disable (J2602 Compliance Control) 0 - LIN will be set to recessive state in case of VS1 under-voltage condition 1 - LIN will stay functional even with a VS1 under-voltage condition
2 - LINEN	LIN Module Enable 0 - LIN Module Disabled 1 - LIN Module Enabled
1-0 - LINSR	LIN - Slew Rate Select 00 - Normal Slew Rate (20 kBit) 01 - Slow Slew Rate (10.4 kBit) 10 - Fast Slew Rate (100 kBit) 11 - Normal Slew Rate (20 kBit)

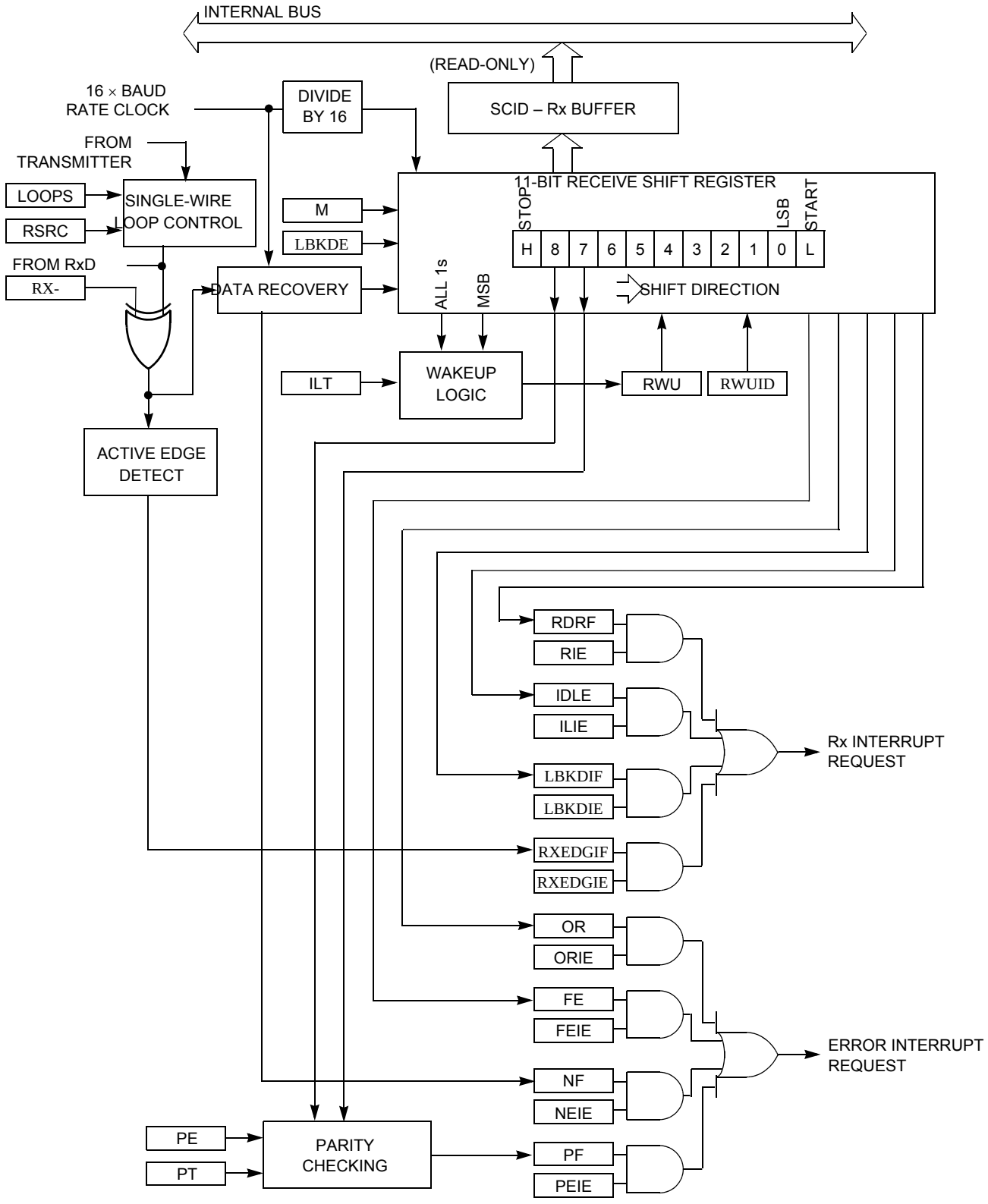


Figure 30. SCI Receiver Block Diagram

Table 165. CFORC - Register Field Descriptions

Field	Description
3-0 FOC[3-0]	Force Output Compare Action for Channel 3-0 0 - Force Output Compare Action disabled. Input Capture or Output Compare Channel Configuration 1 - Force Output Compare Action enabled

A write to this register with the corresponding (FOC 3:0) data bit(s) set causes the action programmed for output compare on channel “n” to occur immediately.The action taken is the same as if a successful comparison had just taken place with the TCn register except the interrupt flag does not get set.

NOTE

A successful channel 3 output compare overrides any channel 2:0 compares. If forced output compare on any channel occurs at the same time as the successful output compare then forced output compare action will take precedence and interrupt flag will not get set.

5.19.3.3.3 Output Compare 3 Mask Register (OC3M)

Table 166. Output Compare 3 Mask Register (OC3M)

Offset(119) 0xC2 — Access: User read/write

	7	6	5	4	3	2	1	0
R	0	0	0	0	OC3M3	OC3M2	OC3M1	OC3M0
W								
Reset	0	0	0	0	0	0	0	0

Note:
119. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 167. OC3M - Register Field Descriptions

Field	Description
3-0 OC3M[3-0]	Output Compare 3 Mask "n" Channel bit 0 - Does not set the corresponding port to be an output port 1 - Sets the corresponding port to be an output port when this corresponding TIOS bit is set to be an output compare

Setting the OC3Mn (n ranges from 0 to 2) will set the corresponding port to be an output port when the corresponding TIOSn (n ranges from 0 to 2) bit is set to be an output compare.

NOTE

A successful channel 3 output compare overrides any channel 2:0 compares. For each OC3M bit that is set, the output compare action reflects the corresponding OC3D bit.

5.19.3.3.4 Output Compare 3 Data Register (OC3D)

Table 168. Output Compare 3 Data Register (OC3D)

Offset(120) 0xC3 — Access: User read/write

	7	6	5	4	3	2	1	0
R	0	0	0	0	OC3D3	OC3D2	OC3D1	OC3D0
W								
Reset	0	0	0	0	0	0	0	0

Note:
120. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 186. Timer Clock Selection

PR2	PR1	PR0	Timer Clock
0	0	0	D2D Clock / 1
0	0	1	D2D Clock / 2
0	1	0	D2D Clock / 4
0	1	1	D2D Clock / 8
1	0	0	D2D Clock / 16
1	0	1	D2D Clock / 32
1	1	0	D2D Clock / 64
1	1	1	D2D Clock / 128

5.19.3.3.12 Main Timer Interrupt Flag 1 (TFLG1)

Table 187. Main Timer Interrupt Flag 1 (TFLG1)

Offset[128] 0xCC — Access: User read/write

	7	6	5	4	3	2	1	0
R	0	0	0	0	C3F	C2F	C1F	C0F
W								
Reset	0	0	0	0	0	0	0	0

Note:
128. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 188. TFLG1 - Register Field Descriptions

Field	Description
3-0 C[3:0]F	Input Capture/Output Compare Channel Flag. 1 = Input Capture or Output Compare event occurred 0 = No event (Input Capture or Output Compare event) occurred.

NOTE

These flags are set when an input capture or output compare event occurs. Flag set on a particular channel is cleared by writing a one to that corresponding CnF bit. Writing a zero to CnF bit has no effect on its status. When TFFCA bit in TSCR register is set, a read from an input capture or a write into an output compare channel will cause the corresponding channel flag CnF to be cleared.

5.19.3.3.13 Main Timer Interrupt Flag 2 (TFLG2)

Table 189. Main Timer Interrupt Flag 2 (TFLG2)

Offset[119] 0xCD — Access: User read/write

	7	6	5	4	3	2	1	0
R	TOF	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

Note:
129. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

5.29.1.4.2 Security

S12I derives can be secured to prohibit external access to the on-chip P-Flash. The S12PMMC module determines the access permissions to the on-chip memories in secured and unsecured state.

5.29.1.5 Block Diagram

Figure 44 shows a block diagram of the S12PMMC.

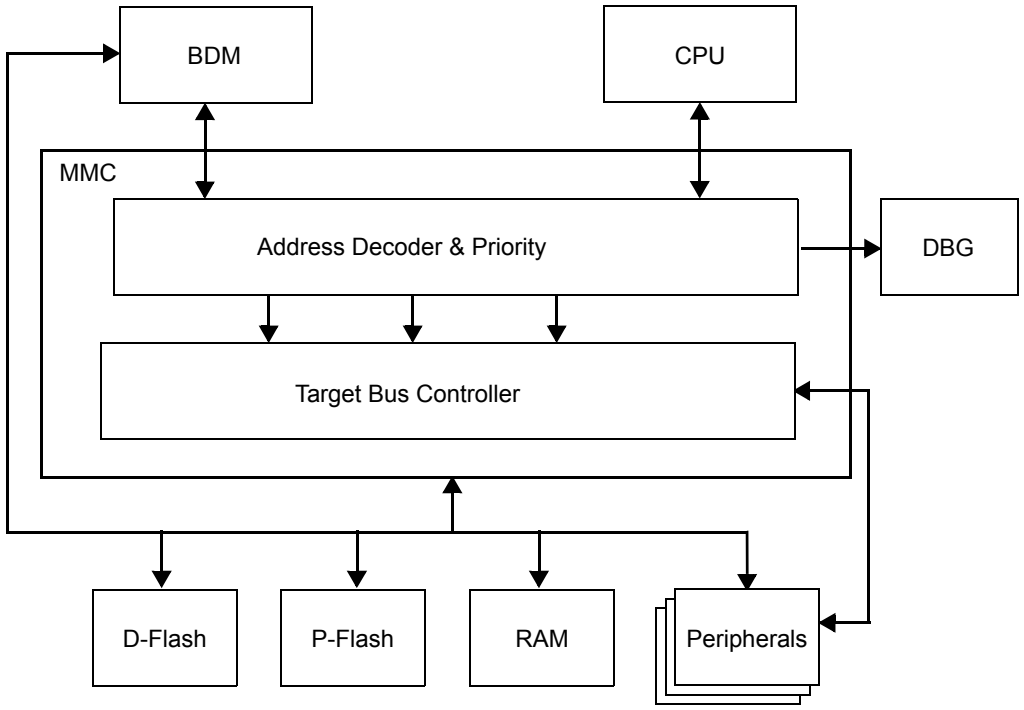


Figure 44. S12PMMC Block Diagram

5.29.2 External Signal Description

The S12PMMC uses two external pins to determine the devices operating mode: RESET and MODC (Table 247) See Device User Guide (DUG) for the mapping of these signals to device pins.

Table 247. External System Pins Associated With S12PMMC

Pin Name	Pin Functions	Description
$\overline{\text{RESET}}$ (See DUG)	$\overline{\text{RESET}}$	The $\overline{\text{RESET}}$ pin is used the select the MCU's operating mode.
$\overline{\text{MODC}}$ (See DUG)	MODC	The MODC pin is captured at the rising edge of the $\overline{\text{RESET}}$ pin. The captured value determines the MCU's operating mode.

5.29.3 Memory Map and Registers

5.29.3.1 Module Memory Map

A summary of the registers associated with the S12PMMC block is shown in Table 248. Detailed descriptions of the registers and bits are given in the subsections that follow.

Table 315. DBGADL Field Descriptions

Field	Description
7–0 Bits[7:0]	**Comparator Data Low Compare Bits** — The Comparator data low compare bits control whether the selected comparator compares the data bus bits [7:0] to a logic one or logic zero. The comparator data compare bits are only used in comparison if the corresponding data mask bit is logic 1. This register is available only for comparator A. Data bus comparisons are only performed if the TAG bit in DBGACTL is clear 0 Compare corresponding data bit to a logic zero 1 Compare corresponding data bit to a logic one

5.32.3.2.8.7 Debug Comparator Data High Mask Register (DBGADHM)

Table 316. Debug Comparator Data High Mask Register (DBGADHM)

Address: 0x002E

	7	6	5	4	3	2	1	0
R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reset	0	0	0	0	0	0	0	0

Read: If COMRV[1:0] = 00

Write: If COMRV[1:0] = 00 and DBG not armed.

Table 317. DBGADHM Field Descriptions

Field	Description
7–0 Bits[15:8]	**Comparator Data High Mask Bits** — The Comparator data high mask bits control whether the selected comparator compares the data bus bits [15:8] to the corresponding comparator data compare bits. Data bus comparisons are only performed if the TAG bit in DBGACTL is clear 0 Do not compare corresponding data bit Any value of corresponding data bit allows match. 1 Compare corresponding data bit

5.32.3.2.8.8 Debug Comparator Data Low Mask Register (DBGADLM)

Table 318. Debug Comparator Data Low Mask Register (DBGADLM)

Address: 0x002F

	7	6	5	4	3	2	1	0
R W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset	0	0	0	0	0	0	0	0

Read: If COMRV[1:0] = 00

Write: If COMRV[1:0] = 00 and DBG not armed.

Table 319. DBGADLM Field Descriptions

Field	Description
7–0 Bits[7:0]	**Comparator Data Low Mask Bits** — The Comparator data low mask bits control whether the selected comparator compares the data bus bits [7:0] to the corresponding comparator data compare bits. Data bus comparisons are only performed if the TAG bit in DBGACTL is clear 0 Do not compare corresponding data bit. Any value of corresponding data bit allows match 1 Compare corresponding data bit

Table 382. TC Trimming of the Frequency of the IRC1M

TCTRIM[4:0]	IRC1M indicative relative TC variation	IRC1M indicative frequency drift for relative TC variation
01110	-3.91%	-5.6%
01111	-4.18%	-5.9%
10000	0 (nominal TC of the IRC)	0%
10001	+0.27%	+0.5%
10010	+0.54%	+0.9%
10011	+0.81%	+1.3%
10100	+1.07%	+1.7%
10101	+1.34%	+2.0%
10110	+1.59%	+2.2%
10111	+1.86%	+2.5%
11000	+2.11%	+3.0%
11001	+2.38%	+3.4%
11010	+2.62%	+3.9%
11011	+2.89%	+4.3%
11100	+3.12%	+4.7%
11101	+3.39%	+5.1%
11110	+3.62%	+5.6%
11111	+3.89%	+5.9%

NOTE

Since the IRC1M frequency is not a linear function of the temperature, but more like a parabola, the above relative variation is only an indication and should be considered with care.

Be aware that the output frequency varies with the TC trimming. A frequency trimming correction is therefore necessary. The values provided in Table 382 are typical values at ambient temperature which can vary from device to device.

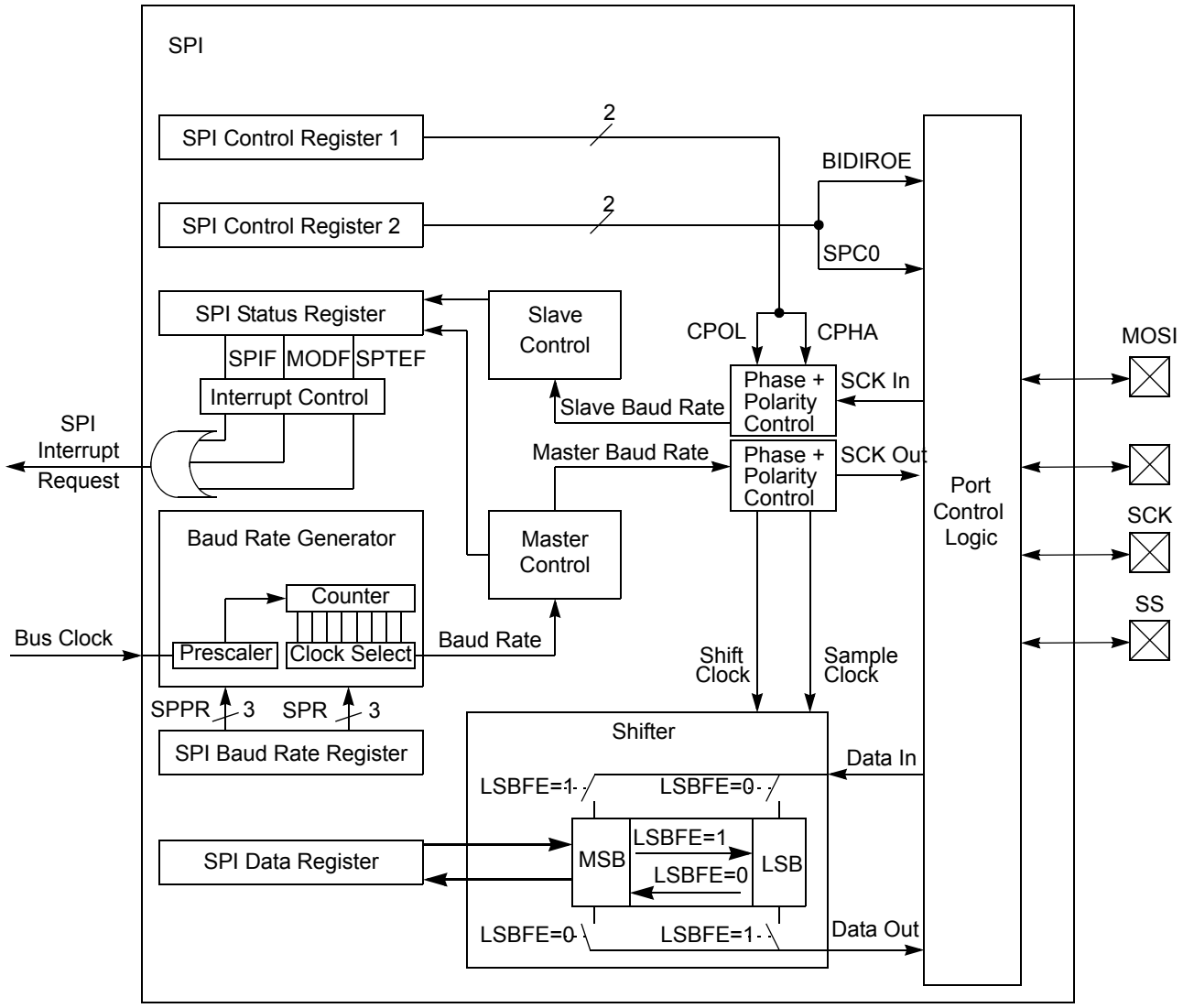


Figure 94. SPI Block Diagram

5.39.2 External Signal Description

This section lists the name and description of all ports including inputs and outputs that do, or may, connect off chip. The SPI module has a total of four external pins.

5.39.2.1 MOSI — Master Out/Slave In Pin

This pin is used to transmit data out of the SPI module when it is configured as a master and receive data when it is configured as slave.

5.39.2.2 MISO — Master In/Slave Out Pin

This pin is used to transmit data out of the SPI module when it is configured as a slave and receive data when it is configured as master.

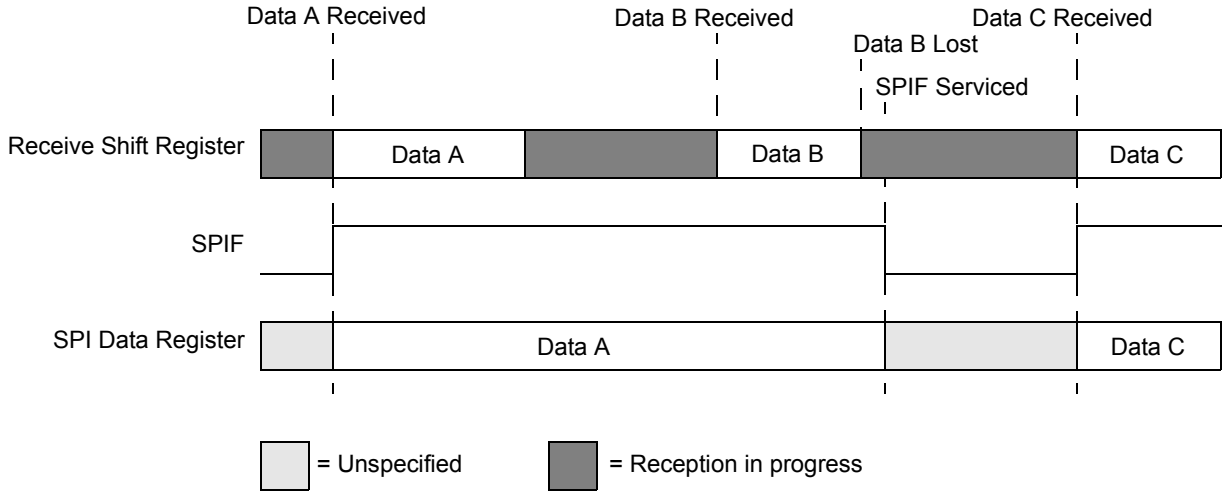


Figure 98. Reception with SPIF Serviced Too Late

5.39.4 Functional Description

The SPI module allows a duplex, synchronous, serial communication between the MCU and peripheral devices. Software can poll the SPI status flags or SPI operation can be interrupt driven.

The SPI system is enabled by setting the SPI enable (SPE) bit in SPI control register 1. While SPE is set, the four associated SPI port pins are dedicated to the SPI function as:

- Slave select ($\overline{SS}$)
- Serial clock (SCK)
- Master out/slave in (MOSI)
- Master in/slave out (MISO)

The main element of the SPI system is the SPI data register. The n-bit(208) data register in the master and the n-bit(208) data register in the slave are linked by the MOSI and MISO pins to form a distributed 2n-bit(208) register. When a data transfer operation is performed, this 2n-bit(208) register is serially shifted n(208) bit positions by the S-clock from the master, so data is exchanged between the master and the slave. Data written to the master SPI data register becomes the output data for the slave, and data read from the master SPI data register after a transfer operation is the input data from the slave.

A read of SPISR with SPTEF = 1 followed by a write to SPIDR puts data into the transmit data register. When a transfer is complete and SPIF is cleared, received data is moved into the receive data register. This data register acts as the SPI receive data register for reads and as the SPI transmit data register for writes. A common SPI data register address is shared for reading data from the read data buffer and for writing data to the transmit data register.

The clock phase control bit (CPHA) and a clock polarity control bit (CPOL) in the SPI control register 1 (SPICR1) select one of four possible clock formats to be used by the SPI system. The CPOL bit simply selects a non-inverted or inverted clock. The CPHA bit is used to accommodate two fundamentally different protocols by sampling data on odd numbered SCK edges or on even numbered SCK edges (see Section 5.39.4.3, “Transmission Formats").

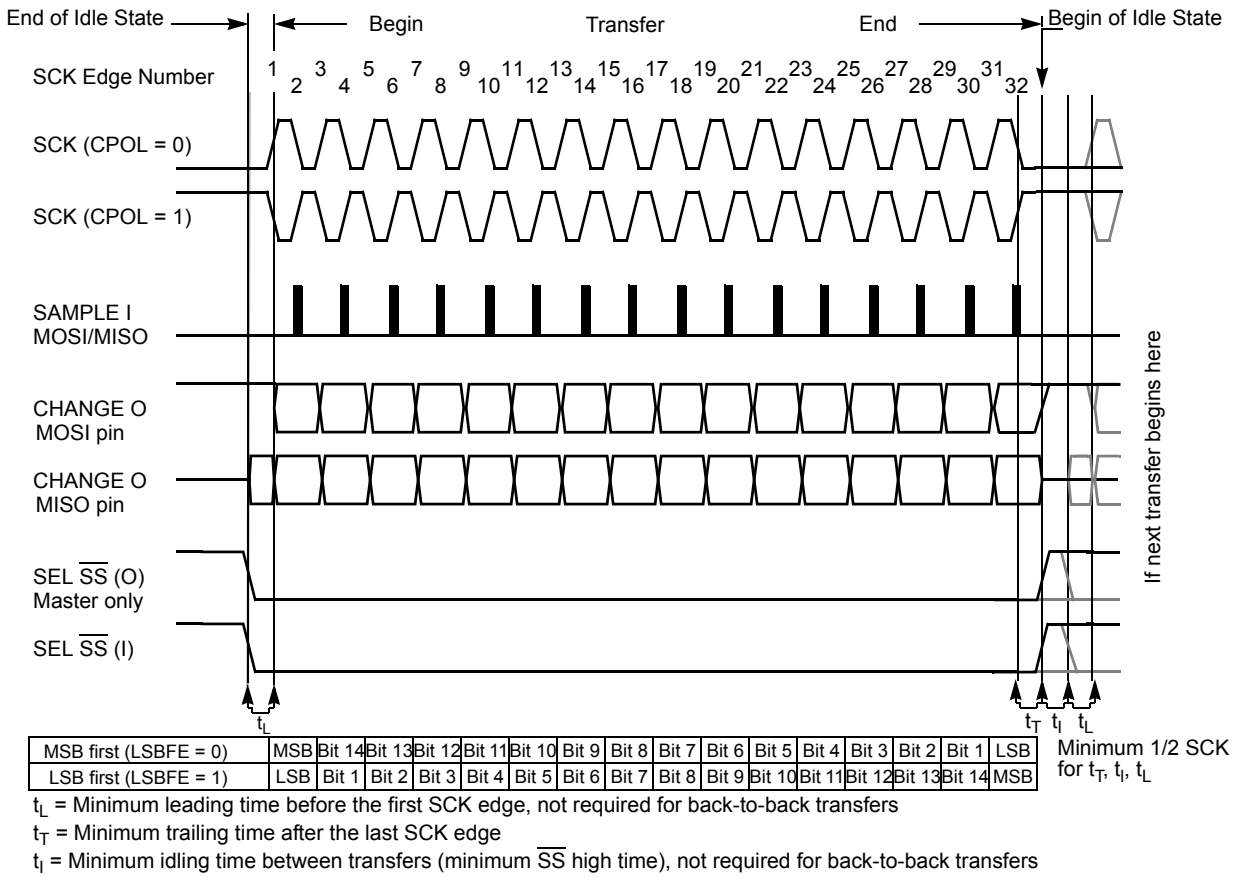
The SPI can be configured to operate as a master or as a slave. When the MSTR bit in SPI control register1 is set, master mode is selected, when the MSTR bit is clear, slave mode is selected.

Note:

208. n depends on the selected transfer width, refer to Section 5.39.3.2.2, “SPI Control Register 2 (SPICR2)"

NOTE

A change of CPOL or MSTR bit while there is a received byte pending in the receive shift register will destroy the received byte and must be avoided.



t_L = Minimum leading time before the first SCK edge, not required for back-to-back transfers

t_T = Minimum trailing time after the last SCK edge

t_I = Minimum idling time between transfers (minimum $\overline{SS}$ high time), not required for back-to-back transfers

Figure 103. SPI Clock Format 1 (CPHA = 1), with 16-Bit Transfer Width Selected (XFRW = 1)

The $\overline{SS}$ line can remain active low between successive transfers (can be tied low at all times). This format is sometimes preferred in systems having a single fixed master and a single slave that drive the MISO data line.

Back-to-back transfers in master mode

In master mode, if a transmission has completed and new data is available in the SPI data register, this data is sent out immediately without a trailing and minimum idle time.

The SPI interrupt request flag (SPIF) is common to both the master and slave modes. SPIF gets set one half SCK cycle after the last SCK edge.

5.39.4.4 SPI Baud Rate Generation

Baud rate generation consists of a series of divider stages. Six bits in the SPI baud rate register (SPPR2, SPPR1, SPPR0, SPR2, SPR1, and SPR0) determine the divisor to the SPI module clock which results in the SPI baud rate.

The SPI clock rate is determined by the product of the value in the baud rate preselection bits (SPPR2–SPPR0) and the value in the baud rate selection bits (SPR2–SPR0). The module clock divisor equation is shown in Equation 104.

$$\text{BaudRateDivisor} = (\text{SPPR} + 1) \bullet 2^{(\text{SPR} + 1)} \qquad \textit{Eqn. 104}$$

When all bits are clear (the default condition), the SPI module clock is divided by 2. When the selection bits (SPR2–SPR0) are 001 and the preselection bits (SPPR2–SPPR0) are 000, the module clock divisor becomes 4. When the selection bits are 010, the module clock divisor becomes 8, etc.

When the preselection bits are 001, the divisor determined by the selection bits is multiplied by 2. When the preselection bits are 010, the divisor is multiplied by 3, etc. See Table 403 for baud rate calculations for all bit conditions, based on a 25 MHz bus clock. The two sets of selects allows the clock to be divided by a non-power of two to achieve other baud rates such as divide by 6, divide by 10, etc.

5.40.3.2.10 P-Flash Protection Restrictions

The general guideline is that P-Flash protection can only be added and not removed. Table 438 specifies all valid transitions between P-Flash protection scenarios. Any attempt to write an invalid scenario to the FPROT register will be ignored. The contents of the FPROT register reflect the active protection scenario. See the FPHS and FPLS bit descriptions for additional restrictions.

Table 438. P-Flash Protection Scenario Transitions

From Protection Scenario	To Protection Scenario (222)							
	0	1	2	3	4	5	6	7
0	X	X	X	X				
1		X		X				
2			X	X				
3				X				
4				X	X			
5			X	X	X	X		
6		X		X	X		X	
7	X	X	X	X	X	X	X	X

Note:
222. Allowed transitions marked with X, see Figure 10-14 for a definition of the scenarios.

5.40.3.2.11 D-Flash Protection Register (DFPROT)

The DFPROT register defines which D-Flash sectors are protected against program and erase operations.

Table 439. D-Flash Protection Register (DFPROT)

	7	6	5	4	3	2	1	0
R	DPOPEN	0	0	0	DPS[3:0]			
W								
Reset	F	0	0	0	F	F	F	F

= Unimplemented or Reserved

The (unreserved) bits of the DFPROT register are writable with the restriction that protection can be added but not removed. Writes must increase the DPS value and the DPOPEN bit can only be written from 1 (protection disabled) to 0 (protection enabled). If the DPOPEN bit is set, the state of the DPS bits is irrelevant.

During the reset sequence, the DFPROT register is loaded with the contents of the D-Flash protection byte in the Flash configuration field at global address 0x3_FF0D located in P-Flash memory (see Table 411) as indicated by reset condition F in Figure 439. To change the D-Flash protection that will be loaded during the reset sequence, the P-Flash sector containing the D-Flash protection byte must be unprotected, then the D-Flash protection byte must be programmed. If a double bit fault is detected while reading the P-Flash phrase containing the D-Flash protection byte during the reset sequence, the DPOPEN bit will be cleared and DPS bits will be set to leave the D-Flash memory fully protected.

Trying to alter data in any protected area in the D-Flash memory will result in a protection violation error and the FPVIOL bit will be set in the FSTAT register. Block erase of the D-Flash memory is not possible if any of the D-Flash sectors are protected.