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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	Automotive
Core Processor	S12
Program Memory Type	FLASH (48kB)
Controller Series	HCS12
RAM Size	2K x 8
Interface	LIN, SCI
Number of I/O	9
Voltage - Supply	2.25V ~ 5.5V
Operating Temperature	-40°C ~ 105°C
Mounting Type	Surface Mount
Package / Case	48-LQFP Exposed Pad
Supplier Device Package	48-HLQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mm912g634dc1ae

1 Ordering Information

Table 1. ORDERING INFORMATION

Device (Add an R2 suffix for Tape and Reel orders)	Temperature Range (T_A)	Package	Max. Bus Frequency in MHz (f_{BUSMAX})	Flash (kB)	Data Flash (kB)	RAM (kB)	Analog Option[1]	Stop Mode Wake-up
MM912G634CM1AE	-40°C to 125°C	LQFP48-EP	20	48[2]	2[3]	2[4]	A1	[5]
MM912G634DM1AE								Enhanced
MM912G634CV1AE	-40°C to 105°C	LQFP48-EP	20	48[2]	2[3]	2[4]	A1	[5]
MM912G634DV1AE								Enhanced
MM912G634CV2AP	-40°C to 105°C	LQFP48	16	48[2]	2[3]	2[4]	A2	[5]
MM912G634DV2AP								Enhanced
MM912H634CM1AE	-40°C to 125°C	LQFP48-EP	20	64	4	6	A1	[5]
MM912H634DM1AE								Enhanced
MM912H634CV1AE	-40°C to 105°C	LQFP48-EP	20	64	4	6	A1	[5]
MM912H634DV1AE								Enhanced

Note:
1. See Table 2.
2. The 48 kB Flash option (MM912**G**634) using the same S12I64 MCU with the tested FLASHSIZE reduced to 48 kB. This will limit the usable Flash area to the first 48 kB (0x3_4000-0x3_FFFF).
3. The 48 kB Flash option (MM912**G**634) using the same S12I64 MCU with the tested Data - FLASHSIZE reduced to 2.0 kB. This will limit the usable Data Flash area to the first 2.0 kB (0x0_4400-0x0_4BFF).
4. The 48 kB Flash option (MM912**G**634) using the same S12I64 MCU with the tested RAMSIZE reduced to 2.0 kB. This will limit the usable RAM area to the first 2.0 kB (0x0_2800-0x0_2FFF).
5. Refer to MM912_634, Silicon Analog Mask (M91W) / Digital Mask (N53A) Errata

Table 2. Analog Options[6]

Feature	A1	A2
Battery Sense Module	YES	YES
Current Sense Module	YES	NO
2nd High Side Output (HS2)	YES	YES
Wake-up Inputs (Lx)	L0…L5	L0…L3
Hall Supply Output (HSUP)	YES	YES
LIN Module	YES	YES

Note:
6. This table only highlights the analog die differences between the derivatives. Features highlighted as “NO” or the Lx Inputs not mentioned are not available in the specific option and not bonded out and/or not tested. See Section 5.3.3, “Analog Die Options" for detailed information.

2 Part Identification

This section provides an explanation of the part numbers and their alpha numeric breakdown.

2.1 Description

Part numbers for the chips have fields that identify the specific part configuration. You can use the values of these fields to determine the specific part you have received.

2.2 Format and Examples

Part numbers for a given device have the following format, followed by a device example:

Table 3 - Part Numbering - Analog EMBEDDED MCU + POWER:

- MM912G634CM1AE

Table 37. Dynamic Electrical Characteristics - General Purpose I/O - PTB[0…2](40)

Ratings	Symbol	Min	Typ	Max	Unit
GPIO Digital Frequency	f_{PTB}	-	-	10	MHz
Propagation Delay - Rising Edge(41)	t_{PDR}	-	-	20	ns
Rise Time - Rising Edge(40)	t_{RISE}	-	-	17.5	ns
Propagation Delay - Falling Edge(40)	t_{PDF}	-	-	20	ns
Rise Time - Falling Edge(40)	t_{FALL}	-	-	17.5	ns

Note:
40. Guaranteed by design.
41. Load PTBx = 100 pF.

Table 38. Dynamic Electrical Characteristics - Analog Digital Converter - ADC(42)

Ratings	Symbol	Min	Typ	Max	Unit
ADC Operating Frequency	f_{ADC}	1.6	2.0	2.4	MHz
Conversion Time (from ACCR write to CC Flag)	t_{CONV}		26		clk
Sample Frequency Channel 14 (Bandgap)	f_{CH14}	-	-	2.5	kHz

Note:
42. Guaranteed by design.

4.6.2 Dynamic Electrical Characteristics MCU Die

4.6.2.1 NVM

4.6.2.1.1 Timing Parameters

The time base for all NVM program or erase operations is derived from the bus clock using the FCLKDIV register. The frequency of this derived clock must be set within the limits specified as f_{NVMOP}. The NVM module does not have any means to monitor the frequency and will not prevent program or erase operations at frequencies above or below the specified minimum. When attempting to program or erase the NVM module at a lower frequency, a full program or erase transition is not assured.

The following sections provide equations which can be used to determine the time required to execute specific flash commands. All timing parameters are a function of the bus clock frequency, f_{NVMBUS}. All program and erase times are also a function of the NVM operating frequency, f_{NVMOP}. A summary of key timing parameters can be found in Table 39.

4.6.2.1.1.1 Erase Verify All Blocks (Blank Check) (FCMD=0x01)

The time required to perform a blank check on all blocks is dependent on the location of the first non-blank word starting at relative address zero. It takes one bus cycle per phrase to verify plus a setup of the command. Assuming that no non-blank location is found, then the time to erase verify all blocks is given by:

$$t_{check} = 19200 \cdot \frac{1}{f_{NVMBUS}}$$

4.6.2.1.1.2 Erase Verify Block (Blank Check) (FCMD=0x02)

The time required to perform a blank check is dependent on the location of the first non-blank word starting at relative address zero. It takes one bus cycle per phrase to verify plus a setup of the command.

Assuming that no non-blank location is found, then the time to erase verify a P-Flash block is given by:

$$t_{pcheck} = 17200 \cdot \frac{1}{f_{NVMBUS}}$$

Table 49. ESD and Latch-up Protection Characteristics (continued)

Ratings	Symbol	Value	Unit
ESD GUN - LIN Conformance Test Specification[61], unpowered, contact discharge, C_{ZAP}= 150 pF, R_{ZAP} = 330 Ω. - LIN (with or without bus filter C_{BUS}=220 pF) - VS1, VS2 with C_{VS} - Lx with serial R_{LX}		 ±15000 ±20000 ±6000	V
ESD GUN - following IEC 61000-4-2 Test Specification[62], unpowered, contact discharge, C_{ZAP}= 150 pF, R_{ZAP} = 330 Ω - LIN (with or without bus filter C_{BUS}=220 pF) - VSENSE with serial R_{VSENSE}[60] - VS1, VS2 with C_{VS} - Lx with serial R_{LX}		 ±8000 ±8000 ±8000 ±8000	V
ESD GUN - following ISO10605 Test Specification[62], unpowered, contact discharge, C_{ZAP}= 150 pF, R_{ZAP} = 2.0 kΩ - LIN (with or without bus filter C_{BUS}=220pF) - VSENSE with serial R_{VSENSE}[60] - VS1, VS2 with C_{VS} - Lx with serial R_{LX}		 ±6000 ±6000 ±6000 ±6000	V
ESD GUN - following ISO10605 Test Specification[62], powered, contact discharge, C_{ZAP}= 330 pF, R_{ZAP} = 2.0 kΩ - LIN (with or without bus filter C_{BUS}=220 pF) - VSENSE with serial R_{VSENSE}[60] - VS1, VS2 with C_{VS} - Lx with serial R_{LX}		 ±8000 ±8000 ±8000 ±8000	V

Note:
59. Input Voltage Limit = -2.5 to 7.5 V.
60. With C_{VBAT} (10…100 nF) as part of the battery path.
61. Certification available on request
62. Tested internally only; certification pending

4.9 Additional Test Information ISO7637-2

Immunity against transients for the LIN, Lx, and VBAT, is specified according to the LIN Conformance Test Specification - Section LIN EMC Test Specification refer to the LIN Conformance Test Certification Report - available as separate document.

5.7.1.2 Interrupt Vector Emulation by Priority

To allow a vector based interrupt handling by the MCU, the number of the highest prioritized interrupt pending is returned in the Interrupt Vector Register. To allow an offset based vector table, the result is pre-shifted (multiple of 2). Reading this register will not acknowledge an interrupt. An additional D2D access is necessary to serve the specific module.

5.7.1.2.1 Interrupt Vector Register (IVR)

Table 89. Interrupt Vector Register (IVR)

Offset[72] 0x02 Access: User read

	7	6	5	4	3	2	1	0
R	0	0	IRQ					
W								

Note:
72. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 90. IVR - Register Field Descriptions

Field	Description
5:0 IRQ	Represents the highest prioritized interrupt pending. See Table 91 In case no interrupt is pending, the result will be 0.

The following table is listing all MM912_634 analog die interrupt sources with the corresponding priority.

Table 91. Interrupt Source Priority

Interrupt Source	IRQ	Priority
no interrupt pending or wake-up from Stop mode	0x00	1 (highest)
LVI - Low Voltage Interrupt	0x02	2
HTI - Voltage Regulator High Temperature Interrupt	0x04	3
LBI - Low Battery Interrupt	0x06	4
CH0 - TIM Channel 0 Interrupt	0x08	5
CH1 - TIM Channel 1 Interrupt	0x0A	6
CH2 - TIM Channel 2 Interrupt	0x0C	7
CH3 - TIM Channel 3 Interrupt	0x0E	8
TOV - Timer Overflow Interrupt	0x10	9
ERR - SCI Error Interrupt	0x12	10
TX - SCI Transmit Interrupt	0x14	11
RX - SCI Receive Interrupt	0x16	12
SCI - ADC Sequence Complete Interrupt	0x18	13
LINOT - LIN Driver Over-temperature Interrupt	0x1A	14
HSOT - High Side Over-temperature Interrupt	0x1C	15
LSOT - Low Side Over-temperature Interrupt	0x1E	16
HOT - HSUP Over-temperature Interrupt	0x20	17
HVI - High Voltage Interrupt	0x22	18
VROVI - Voltage Regulator Over-voltage Interrupt	0x24	19 (lowest)

5.7.2 Interrupt Sources

5.7.2.1 Voltage Status Interrupt (VSI)

The Voltage Status Interrupt - VSI combines the five interrupt sources of the Voltage Status Register. It is only available in the Interrupt Source Register (ISR). Acknowledge the interrupt by reading the Voltage Status Register - VSR. To issue a new interrupt, the condition has to vanish and occur again. See Section 5.5, “Power Supply" for details on the Voltage Status Register including masking information.

5.7.2.2 Low Voltage Interrupt (LVI)

Acknowledge the interrupt by reading the Voltage Status Register - VSR. To issue a new interrupt, the condition has to vanish and occur again. See Section 5.5, “Power Supply" for details on the Voltage Status Register including masking information.

5.7.2.3 Voltage Regulator High Temperature Interrupt (HTI)

Acknowledge the interrupt by reading the Voltage Status Register - VSR. To issue a new interrupt, the condition has to vanish and occur again. See Section 5.5, “Power Supply" for details on the Voltage Status Register including masking information.

5.7.2.4 Low Battery Interrupt (LBI)

Acknowledge the interrupt by reading the Voltage Status Register - VSR. To issue a new interrupt, the condition has to vanish and occur again. See Section 5.5, “Power Supply" for details on the Voltage Status Register including masking information.

5.7.2.5 TIM Channel 0 Interrupt (CH0)

See Section 5.19, “Basic Timer Module - TIM (TIM16B4C)".

5.7.2.6 TIM Channel 1 Interrupt (CH1)

See Section 5.19, “Basic Timer Module - TIM (TIM16B4C)".

5.7.2.7 TIM Channel 2 Interrupt (CH2)

See Section 5.19, “Basic Timer Module - TIM (TIM16B4C)".

5.7.2.8 TIM Channel 3 Interrupt (CH3)

See Section 5.19, “Basic Timer Module - TIM (TIM16B4C)".

5.7.2.9 TIM Timer Overflow Interrupt (TOV)

See Section 5.19, “Basic Timer Module - TIM (TIM16B4C)".

5.7.2.10 SCI Error Interrupt (ERR)

See Section 5.16, “Serial Communication Interface (S08SCIV4)".

5.7.2.11 SCI Transmit Interrupt (TX)

See Section 5.16, “Serial Communication Interface (S08SCIV4)".

5.7.2.12 SCI Receive Interrupt (RX)

See Section 5.16, “Serial Communication Interface (S08SCIV4)".

5.7.2.13 LIN Driver Over-temperature Interrupt (LINOT)

Acknowledge the interrupt by reading the LIN Register - LINR. To issue a new interrupt, the condition has to vanish and occur again. See Section 5.15, “LIN Physical Layer Interface - LIN" for details on the LIN Register including masking information.

Table 95. WCR - Register Field Descriptions

Field	Description
3 - L3WE	Wake-up Input 3 Enabled - L3 Wake-up Select Bit. 0 - L3Wake-up Disabled 1 - L3 Wake-up Enabled
2- L2WE	Wake-up Input 2 Enabled - L2 Wake-up Select Bit. 0 - L2 Wake-up Disabled 1 - L2 Wake-up Enabled
1 - L1WE	Wake-up Input 1 Enabled - L1 Wake-up Select Bit. 0 - L1 Wake-up Disabled 1 - L1 Wake-up Enabled
0 - L0WE	Wake-up Input 0 Enabled - L0 Wake-up Select Bit. 0 - L0 Wake-up Disabled 1 - L0 Wake-up Enabled

5.9.2.2 Timing Control Register (TCR)

Table 96. Timing Control Register (TCR)

Offset[76] 0x13 — Access: User read/write

	7	6	5	4	3	2	1	0
R W	FWM				CST			
Reset	0	0	0	0	0	0	0	0

Note:
76. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

5.13 Low Side Drivers - LSx

5.13.1 Introduction / Features

These outputs are two low side drivers intended to drive relays (inductive loads) incorporating the following features:

- PWM capability
- Open load detection
- Current limitation
- Over-temperature shutdown (with maskable interrupt)
- Active clamp
- Independent VREG - High Voltage Shutdown

5.13.1.1 Block Diagram

The following Figure shows the basic structure of the LS drivers.

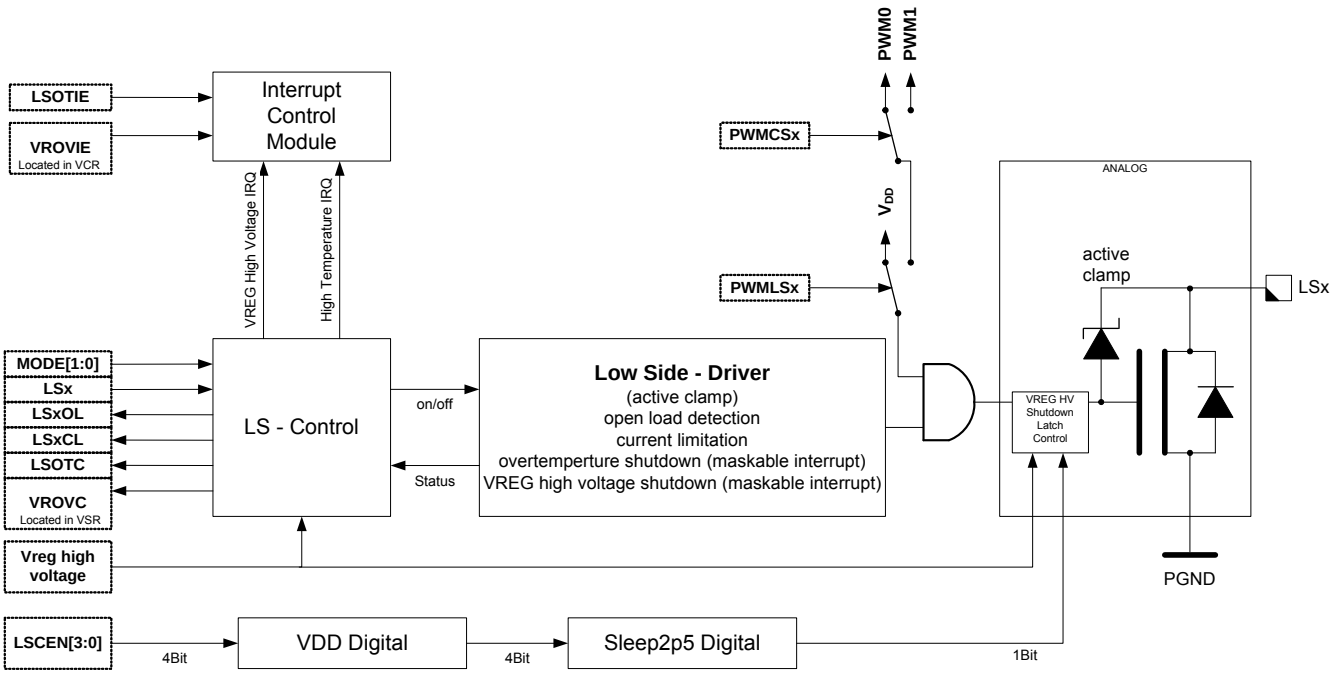


Figure 21. Low Side Drivers - Block Diagram

5.13.1.2 Modes of Operation

The Low Side module is active only in Normal mode; the Low Side drivers are disabled in Sleep and Stop mode.

5.13.2 External Signal Description

This section lists and describes the signals that do connect off-chip.

Table 110 shows all the pins and their functions that are controlled by the Low Side module.

Table 110. Pin Functions and Priorities

Pin Name	Pin Function & Priority	I/O	Description	Pin Function after Reset
LS1	High Voltage Output	O	Low Side Power Output Driver, Active Clamping	LS1
LS2		O		LS2

Table 129. PWM Channel Duty Registers (PWMDTYx)

Offset[96] 0x68/0x69 Access: User read/write

	7	6	5	4	3	2	1	0
R W	Bit 7	6	5	4	3	2	1	Bit 0
Reset	0	0	0	0	0	0	0	0

Note:

96. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

5.14.4 Functional Description

5.14.4.1 PWM Clock Select

There are four available clocks: clock A, clock B, clock SA (scaled A), and clock SB (scaled B). These four clocks are based on the D2D clock.

Clock A and B can be software selected to be 1, 1/2, 1/4, 1/8,..., 1/64, 1/128 times the D2D clock. Clock SA uses clock A as an input and divides it further with a reloadable counter. Similarly, clock SB uses clock B as an input and divides it further with a reloadable counter. The rates available for clock SA are software selectable to be clock A divided by 2, 4, 6, 8,..., or 512 in increments of divide by 2. Similar rates are available for clock SB. Each PWM channel has the capability of selecting one of two clocks, either the pre-scaled clock (clock A or B) or the scaled clock (clock SA or SB).

The block diagram in Figure 23 shows the four different clocks and how the scaled clocks are created.

5.14.4.1.1 Prescale

The input clock to the PWM prescaler is the D2D clock. The input clock can also be disabled when both PWM channels are disabled (PWME1-0 = 0). This is useful for reducing power by disabling the prescale counter.

Clock A and clock B are scaled values of the input clock. The value is software selectable for both clock A and clock B and has options of 1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, or 1/128 times the D2D clock. The value selected for clock A is determined by the PCKA2, PCKA1, PCKA0 bits in the PWMPRCLK register. The value selected for clock B is determined by the PCKB2, PCKB1, PCKB0 bits also in the PWMPRCLK register.

5.14.4.1.2 Clock Scale

The scaled A clock uses clock A as an input and divides it further with a user programmable value and then divides this by 2. The scaled B clock uses clock B as an input and divides it further with a user programmable value and then divides this by 2. The rates available for clock SA are software selectable to be clock A divided by 2, 4, 6, 8,..., or 512 in increments of divide by 2. Similar rates are available for clock SB.

5.14.4.2.7 PWM Boundary Cases

Table 131 summarizes the boundary conditions for the PWM, regardless of the output mode (left aligned or center aligned).

Table 131. PWM Boundary Cases

PWMDTYx	PWMPERx	PPOLx	PWMx Output
$00 (indicates no duty)	>$00	1	Always low
$00 (indicates no duty)	>$00	0	Always high
XX	$00[97] (indicates no period)	1	Always high
XX	$00[97] (indicates no period)	0	Always low
>= PWMPERx	XX	1	Always high

Note:
97. Counter = $00 and does not count.

5.14.5 Resets

The reset state of each individual bit is listed within the Section 5.14.3, “Register Descriptions", which details the registers and their bit-fields. All special functions or modes which are initialized during or just following reset are described within this section.

- The 8-bit up/down counter is configured as an up counter out of reset.
- All the channels are disabled and all the counters do not count.

5.14.6 Interrupts

The PWM module has no Interrupts.

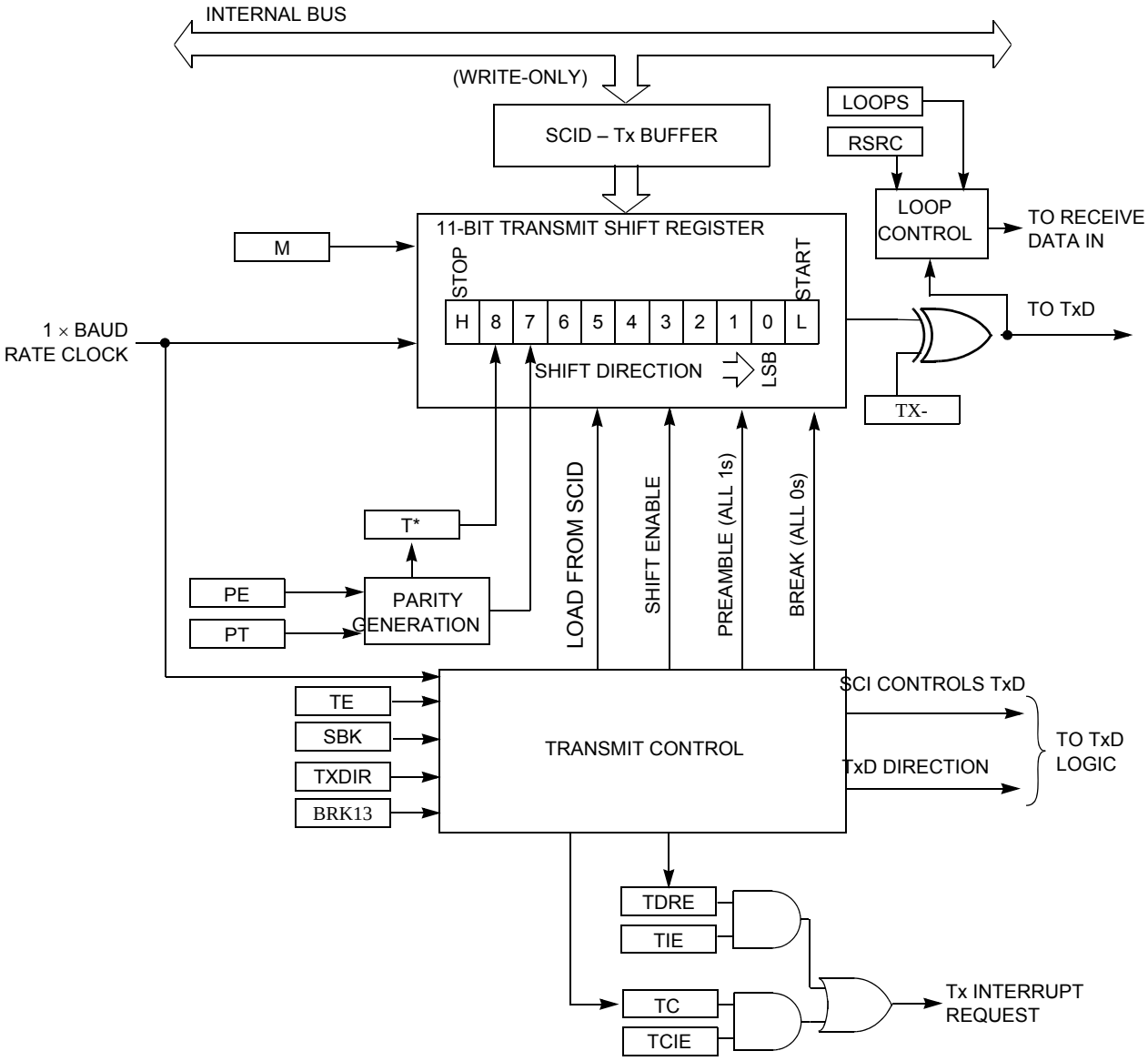


Figure 29. SCI Transmitter Block Diagram

Figure 30 shows the receiver portion of the SCI.

Table 141. SCIC2 Field Descriptions (continued)

Field	Description
1 RWU	Receiver Wake-up Control — This bit can be written to 1 to place the SCI receiver in a standby state where it waits for automatic hardware detection of a selected wake-up condition. The wake-up condition is either an idle line between messages (WAKE = 0, idle-line wake-up), or a logic 1 in the most significant data bit in a character (WAKE = 1, address-mark wake-up). Application software sets RWU and (normally) a selected hardware condition automatically clears RWU. Refer to Section 5.16.3.3.2, “Receiver Wake-up Operation" for more details. 0 Normal SCI receiver operation. 1 SCI receiver in standby waiting for wake-up condition.
0 SBK	Send Break — Writing a 1 and then a 0 to SBK queues a break character in the transmit data stream. Additional break characters of 10 or 11 (13 or 14 if BRK13 = 1) bit times of logic 0 are queued as long as SBK = 1. Depending on the timing of the set and clear of SBK relative to the information currently being transmitted, a second break character may be queued before software clears SBK. Refer to Section 5.16.3.2.1, “Send Break and Queued Idle" for more details. 0 Normal transmitter operation. 1 Queue break character(s) to be sent.

5.16.2.4 SCI Status Register 1 (SCIS1)

This register has eight read-only status flags. Writes have no effect. Special software sequences (which do not involve writing to this register) are used to clear these status flags.

Table 142. SCI Status Register 1 (SCIS1)

Offset(103) 0x44 Access: User read/write

	7	6	5	4	3	2	1	0
R	TDRE	TC	RDRF	IDLE	OR	NF	FE	pF
W								
Reset	1	1	0	0	0	0	0	0

Note:
103. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 143. SCIS1 Field Descriptions

Field	Description
7 TDRE	Transmit Data Register Empty Flag — TDRE is set out of reset and when a transmit data value transfers from the transmit data buffer to the transmit shifter, leaving room for a new character in the buffer. To clear TDRE, read SCIS1 with TDRE = 1 and then write to the SCI data register (SCID). 0 Transmit data register (buffer) full. 1 Transmit data register (buffer) empty.
6 TC	Transmission Complete Flag — TC is set out of reset and when TDRE = 1 and no data, preamble, or break character is being transmitted. 0 Transmitter active (sending data, a preamble, or a break). 1 Transmitter idle (transmission activity complete). TC is cleared automatically by reading SCIS1 with TC = 1 and then doing one of the following three things: • Write to the SCI data register (SCID) to transmit new data • Queue a preamble by changing TE from 0 to 1 • Queue a break character by writing 1 to SBK in SCIC2
5 RDRF	Receive Data Register Full Flag — RDRF becomes set when a character transfers from the receive shifter into the receive data register (SCID). To clear RDRF, read SCIS1 with RDRF = 1 and then read the SCI data register (SCID). 0 Receive data register empty. 1 Receive data register full.

5.19.4 Functional Description

5.19.4.1 General

This section provides a complete functional description of the timer TIM16B4C block. Refer to the detailed timer block diagram in Figure 34 as necessary.

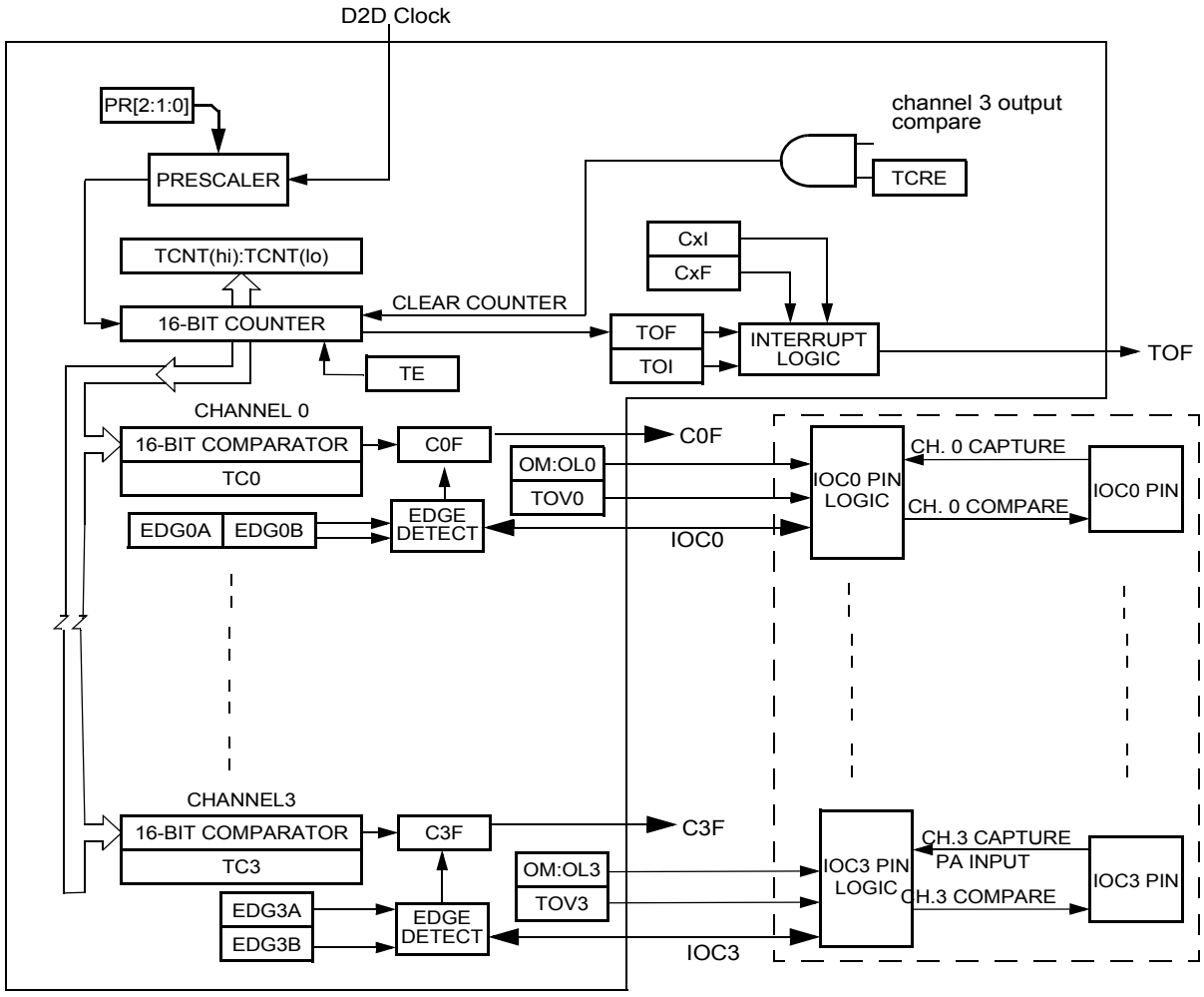


Figure 34. Detailed Timer Block Diagram

5.19.4.2 Prescaler

The prescaler divides the bus clock by 1, 2, 4, 8, 16, 32, 64, or 128. The prescaler select bits, PR[2:0], select the prescaler divisor. PR[2:0] are in the timer system control register 2 (TSCR2).

5.19.4.3 Input Capture

Clearing the I/O (input/output) select bit, IOSn, configures channel n as an input capture channel. The input capture function captures the time at which an external event occurs. When an active edge occurs on the pin of an input capture channel, the timer transfers the value in the timer counter into the timer channel registers, TCn.

The minimum pulse width for the input capture input is greater than two bus clocks.

An input capture on channel n sets the CnF flag. The CnI bit enables the CnF flag to generate interrupt requests.

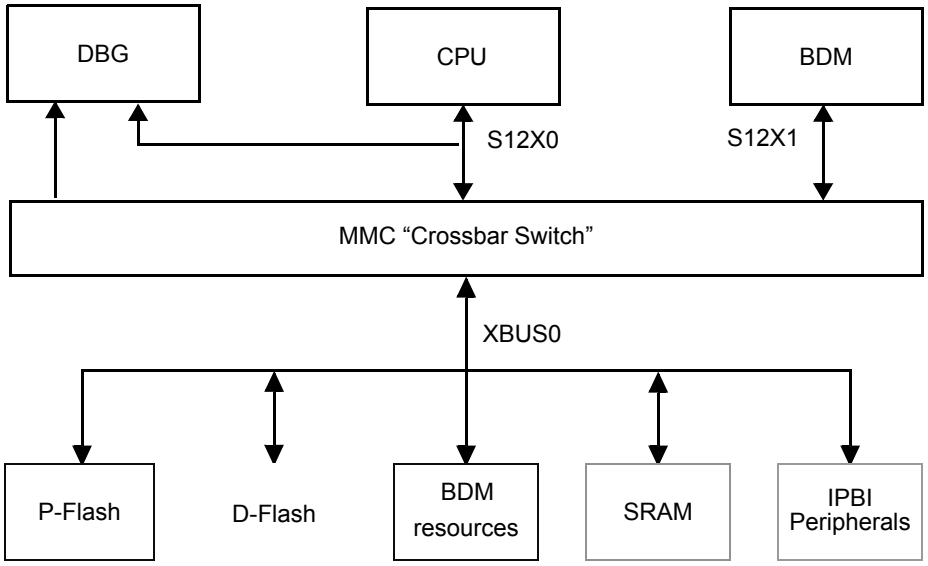


Figure 51. S12I Platform

5.29.5.1.1 Master Bus Prioritization regarding Access Conflicts on Target Buses

The arbitration scheme allows only one master to be connected to a target at any given time. The following rules apply when prioritizing accesses from different masters to the same target bus:

- CPU12 always has priority over BDM.
- BDM has priority over CPU12 when its access is stalled for more than 128 cycles. In the later case the CPU will be stalled after finishing the current operation and the BDM will gain access to the bus.

5.29.5.2 Interrupts

The MMC does not generate any interrupts.

5.29.6 Initialization/Application Information

5.29.6.1 CALL and RTC Instructions

CALL and RTC instructions are uninterruptable CPU instructions that automate page switching in the program page window. The CALL instruction is similar to the JSR instruction, but the subroutine that is called can be located anywhere in the local address space or in any Flash or ROM page visible through the program page window. The CALL instruction calculates and stacks a return address, stacks the current PPAGE value and writes a new instruction-supplied value to the PPAGE register. The PPAGE value controls which of the 256 possible pages is visible through the 16 kbyte program page window in the 64 kbyte local CPU memory map. Execution then begins at the address of the called subroutine.

During the execution of the CALL instruction, the CPU performs the following steps:

1. Writes the current PPAGE value into an internal temporary register and writes the new instruction-supplied PPAGE value into the PPAGE register
2. Calculates the address of the next instruction after the CALL instruction (the return address) and pushes this 16-bit value onto the stack
3. Pushes the temporarily stored PPAGE value onto the stack
4. Calculates the effective address of the subroutine, refills the queue and begins execution at the new address

This sequence is uninterruptable. There is no need to inhibit interrupts during the CALL instruction execution. A CALL instruction can be performed from any address to any other address in the local CPU memory space.

The PPAGE value supplied by the instruction is part of the effective address of the CPU. For all addressing mode variations (except indexed-indirect modes) the new page value is provided by an immediate operand in the instruction. In indexed-indirect variations of the CALL instruction a pointer specifies memory locations where the new page value and the address of the called subroutine are stored. Using indirect addressing for both the new page value and the address within the page allows usage of values calculated at run time rather than immediate values that must be known at the time of assembly.

Table 297. State3 — Sequencer Next State Selection

SC[3:0]	Description (Unspecified matches have no effect)
0011	Match1 to Final State..... Match2 to State1
0100	Match1 to State2
0101	Match1 to Final State
0110	Match2 to State2..... Match0 to Final State
0111	Match0 to Final State
1000	Reserved
1001	Reserved
1010	Either Match1 or Match2 to State1..... Match0 to Final State
1011	Reserved
1100	Reserved
1101	Either Match1 or Match2 to Final State..... Match0 to State1
1110	Match0 to State2..... Match2 to Final State
1111	Reserved

The priorities described in Table 324 dictate that in the case of simultaneous matches, a match leading to final state has priority followed by the match on the lower channel number (0,1,2).

5.32.3.2.7.4 Debug Match Flag Register (DBGMFR)

Table 298. Debug Match Flag Register (DBGMFR)

Address: 0x0027

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	MC2	MC1	MC0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Read: If COMRV[1:0] = 11

Write: Never

DBGMFR is visible at 0x0027 only with COMRV[1:0] = 11. It features 3 flag bits each mapped directly to a channel. Should a match occur on the channel during the debug session, then the corresponding flag is set and remains set until the next time the module is armed by writing to the ARM bit. Thus the contents are retained after a debug session for evaluation purposes. These flags cannot be cleared by software, they are cleared only when arming the module. A set flag does not inhibit the setting of other flags. Once a flag is set, further comparator matches on the same channel in the same session have no affect on that flag.

5.32.3.2.8 Comparator Register Descriptions

Each comparator has a bank of registers that are visible through an 8-byte window in the DBG module register address map. Comparator A consists of 8 register bytes (3 address bus compare registers, two data bus compare registers, two data bus mask registers and a control register). Comparator B consists of four register bytes (three address bus compare registers and a control register). Comparator C consists of four register bytes (three address bus compare registers and a control register).

Each set of comparator registers can be accessed using the COMRV bits in the DBGC1 register. Unimplemented registers (e.g. Comparator B data bus and data bus masking) read as zero and cannot be written. The control register for comparator B differs from those of comparators A and C.

5.38 S12 Clock, Reset and Power Management Unit (S12CPMU)

5.38.1 Introduction

This specification describes the function of the Clock, Reset and Power Management Unit.

- The Pierce oscillator (OSCLCP) provides a robust, low-noise and low-power external clock source. It is designed for optimal start-up margin with typical crystal oscillators.
- The Voltage regulator (IVREG) operates from the range 3.13 to 5.5 V. It provides all the required chip internal voltages and voltage monitors.
- The Phase Locked Loop (PLL) provides a highly accurate frequency multiplier with internal filter.
- The Internal Reference Clock (IRC1M) provides a 1.0 MHz clock.

5.38.1.1 Features

The Pierce Oscillator (OSCLCP) contains circuitry to dynamically control current gain in the output amplitude. This ensures a signal with low harmonic distortion, low power and good noise immunity.

- Supports crystals or resonators from 4.0 to 16 MHz.
- High noise immunity due to input hysteresis and spike filtering.
- Low RF emissions with peak-to-peak swing limited dynamically
- Transconductance (gm) sized for optimum start-up margin for typical crystals
- Dynamic gain control eliminates the need for external current limiting resistor
- Integrated resistor eliminates the need for external bias resistor.
- Low power consumption: Operates from internal 1.8 V (nominal) supply, Amplitude control limits power

The Voltage Regulator (IVREG) has the following features:

- Input voltage range from 3.13 to 5.5 V
- Low-voltage detect (LVD) with low-voltage interrupt (LVI)
- Power-on reset (POR)
- Low-voltage reset (LVR)
- during scan pattern execution option to go to RPM to support IDDq test.
- external voltage reference used for HV-stress test and MIM screen, the external voltage on VDDA, divided by series resistors, will be used as input to the regulating loop of the IVREG

The Phase Locked Loop (PLL) has the following features:

- highly accurate and phase locked frequency multiplier
- Configurable internal filter for best stability and lock time.
- Frequency modulation for defined jitter and reduced emission
- Automatic frequency lock detector
- Interrupt request on entry or exit from locked condition
- Reference clock either external (crystal) or internal square wave (1.0 MHz IRC1M) based.
- PLL stability is sufficient for LIN communication, even if using IRC1M as reference clock

The Internal Reference Clock (IRC1M) has the following features:

- Trimmable in frequency
- Factory trimmed value for 1.0 MHz in Flash Memory, can be overwritten by application if required

Other features of the S12CPMU include

- Clock monitor to detect loss of crystal
- Autonomous periodical interrupt (API)
- Bus Clock Generator
  - Clock switch to select either PLLCLK or external crystal/resonator based Bus Clock
  - PLLCLK divider to adjust system speed
- System Reset generation from the following possible sources:
  - Power-on reset (POR)
  - Low-voltage reset (LVR)
  - Illegal address access
  - COP timeout
  - Loss of oscillation (clock monitor fail)
  - External pin $\overline{\text{RESET}}$

Table 354. CPMURTI Field Descriptions

Field	Description
7 RTDEC	**Decimal or Binary Divider Select Bit** — RTDEC selects decimal or binary based prescaler values. 0 Binary based divider value. See Table 355 1 Decimal based divider value. See Table 356
6–4 RTR[6:4]	**Real Time Interrupt Prescale Rate Select Bits** — These bits select the prescale rate for the RTI. See Table 355 and Table 356.
3–0 RTR[3:0]	**Real Time Interrupt Modulus Counter Select Bits** — These bits select the modulus counter target value to provide additional granularity.Table 355 and Table 356 show all possible divide values selectable by the CPMURTI register.

Table 355. RTI Frequency Divide Rates for RTDEC = 0

RTR[3:0]	RTR[6:4] =							
	000 (OFF)	**001 (2^{10})**	**010 (2^{11})**	**011 (2^{12})**	**100 (2^{13})**	**101 (2^{14})**	**110 (2^{15})**	**111 (2^{16})**
0000 (÷1)	OFF(196)	2^{10}	2^{11}	2^{12}	2^{13}	2^{14}	2^{15}	2^{16}
0001 (÷2)	OFF	$2x2^{10}$	$2x2^{11}$	$2x2^{12}$	$2x2^{13}$	$2x2^{14}$	$2x2^{15}$	$2x2^{16}$
0010 (÷3)	OFF	$3x2^{10}$	$3x2^{11}$	$3x2^{12}$	$3x2^{13}$	$3x2^{14}$	$3x2^{15}$	$3x2^{16}$
0011 (÷4)	OFF	$4x2^{10}$	$4x2^{11}$	$4x2^{12}$	$4x2^{13}$	$4x2^{14}$	$4x2^{15}$	$4x2^{16}$
0100 (÷5)	OFF	$5x2^{10}$	$5x2^{11}$	$5x2^{12}$	$5x2^{13}$	$5x2^{14}$	$5x2^{15}$	$5x2^{16}$
0101 (÷6)	OFF	$6x2^{10}$	$6x2^{11}$	$6x2^{12}$	$6x2^{13}$	$6x2^{14}$	$6x2^{15}$	$6x2^{16}$
0110 (÷7)	OFF	$7x2^{10}$	$7x2^{11}$	$7x2^{12}$	$7x2^{13}$	$7x2^{14}$	$7x2^{15}$	$7x2^{16}$
0111 (÷8)	OFF	$8x2^{10}$	$8x2^{11}$	$8x2^{12}$	$8x2^{13}$	$8x2^{14}$	$8x2^{15}$	$8x2^{16}$
1000 (÷9)	OFF	$9x2^{10}$	$9x2^{11}$	$9x2^{12}$	$9x2^{13}$	$9x2^{14}$	$9x2^{15}$	$9x2^{16}$
1001 (÷10)	OFF	$10x2^{10}$	$10x2^{11}$	$10x2^{12}$	$10x2^{13}$	$10x2^{14}$	$10x2^{15}$	$10x2^{16}$
1010 (÷11)	OFF	$11x2^{10}$	$11x2^{11}$	$11x2^{12}$	$11x2^{13}$	$11x2^{14}$	$11x2^{15}$	$11x2^{16}$
1011 (÷12)	OFF	$12x2^{10}$	$12x2^{11}$	$12x2^{12}$	$12x2^{13}$	$12x2^{14}$	$12x2^{15}$	$12x2^{16}$
1100 (÷13)	OFF	$13x2^{10}$	$13x2^{11}$	$13x2^{12}$	$13x2^{13}$	$13x2^{14}$	$13x2^{15}$	$13x2^{16}$
1101 (÷14)	OFF	$14x2^{10}$	$14x2^{11}$	$14x2^{12}$	$14x2^{13}$	$14x2^{14}$	$14x2^{15}$	$14x2^{16}$
1110 (÷15)	OFF	$15x2^{10}$	$15x2^{11}$	$15x2^{12}$	$15x2^{13}$	$15x2^{14}$	$15x2^{15}$	$15x2^{16}$
1111 (÷16)	OFF	$16x2^{10}$	$16x2^{11}$	$16x2^{12}$	$16x2^{13}$	$16x2^{14}$	$16x2^{15}$	$16x2^{16}$

Note:
196. Denotes the default value out of reset.This value should be used to disable the RTI to ensure future backwards compatibility.

Table 356. RTI Frequency Divide Rates for RTDEC=1

RTR[3:0]	RTR[6:4] =							
	000 ($1x10^3$)	**001 ($2x10^3$)**	**010 ($5x10^3$)**	**011 ($10x10^3$)**	**100 ($20x10^3$)**	**101 ($50x10^3$)**	**110 ($100x10^3$)**	**111 ($200x10^3$)**
0000 (÷1)	$1x10^3$	$2x10^3$	$5x10^3$	$10x10^3$	$20x10^3$	$50x10^3$	$100x10^3$	$200x10^3$
0001 (÷2)	$2x10^3$	$4x10^3$	$10x10^3$	$20x10^3$	$40x10^3$	$100x10^3$	$200x10^3$	$400x10^3$

Table 385. S12CPMU Protection Register (CPMUPROT)

0x02FB

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	PROT
W								
Reset	0	0	0	0	0	0	0	0

Read: Anytime

Write: Anytime

Table 386. Clock Configuration Registers Protection Bit

Field	Description
0	**Clock Configuration Registers Protection Bit —** This bit protects the clock configuration registers from accidental overwrite (see list of protected registers above). Writing 0x26 to the CPMUPROT register clears the PROT bit, other write accesses set the PROT bit. 0 Protection of clock configuration registers is disabled. 1 Protection of clock configuration registers is enabled. (see list of protected registers above)

5.38.3.2.22 Reserved Register CPMUTEST2

NOTE

This reserved register is designed for factory test purposes only, and is not intended for general user access. Writing to this register when in Special Mode can alter the S12CPMU's functionality.

Table 387. Reserved Register CPMUTEST2

0x02FC

	7	6	5	4	3	2	1	0
R	0	0	0 LVRS	0 LVRFS	0 LVRXS	0	0	0RCEXA
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Read: Anytime

Write: Only in Special Mode

The reserved register allows several setting to aid to perform device parametric tests This register can only be written after writing a $E3 before into this register.

Table 480. Verify Backdoor Access Key Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x0C	Not required
001	Key 0	
010	Key 1	
011	Key 2	
100	Key 3	

Upon clearing CCIF to launch the Verify Backdoor Access Key command, the Memory Controller will check the FSEC KEYEN bits to verify that this command is enabled. If not enabled, the Memory Controller sets the ACCERR bit in the FSTAT register and terminates. If the command is enabled, the Memory Controller compares the key provided in FCCOB to the backdoor comparison key in the Flash configuration field with Key 0 compared to 0x3_FF00, etc. If the backdoor keys match, security will be released. If the backdoor keys do not match, security is not released and all future attempts to execute the Verify Backdoor Access Key command are aborted (set ACCERR) until a reset occurs. The CCIF flag is set after the Verify Backdoor Access Key operation has completed.

Table 481. Verify Backdoor Access Key Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 100 at command launch
		Set if an incorrect backdoor key is supplied
		Set if backdoor key access has not been enabled (KEYEN[1:0] != 10, see Section 5.40.3.2.2, “Flash Security Register (FSEC)")
		Set if the backdoor key has mismatched since the last reset
	FPVIOL	None
	MGSTAT1	None
	MGSTAT0	None

5.40.4.5.12 Set User Margin Level Command

The Set User Margin Level command causes the Memory Controller to set the margin level for future read operations of the P-Flash or D-Flash block.

Table 482. Set User Margin Level Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x0D	Global address [17:16] to identify the Flash block
001	Margin level setting	

Upon clearing CCIF to launch the Set User Margin Level command, the Memory Controller will set the user margin level for the targeted block and then set the CCIF flag.

NOTE

When the D-Flash block is targeted, the D-Flash user margin levels are applied only to the D-Flash reads. However, when the P-Flash block is targeted, the P-Flash user margin levels are applied to both P-Flash and D-Flash reads. It is not possible to apply user margin levels to the P-Flash block only.

Valid margin level settings for the Set User Margin Level command are defined in Table 483.

Table 489. Erase Verify D-Flash Section Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 010 at command launch
		Set if command not available in current mode (see Table 456)
		Set if an invalid global address [17:0] is supplied
		Set if a misaligned word address is supplied (global address [0] != 0)
		Set if the requested section breaches the end of the D-Flash block
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the read
	MGSTAT0	Set if any non-correctable errors have been encountered during the read

5.40.4.5.15 Program D-Flash Command

The Program D-Flash operation programs one to four previously erased words in the D-Flash block. The Program D-Flash operation will confirm that the targeted location(s) were successfully programmed upon completion.

A Flash word must be in the erased state before being programmed. Cumulative programming of bits within a Flash word is not allowed.

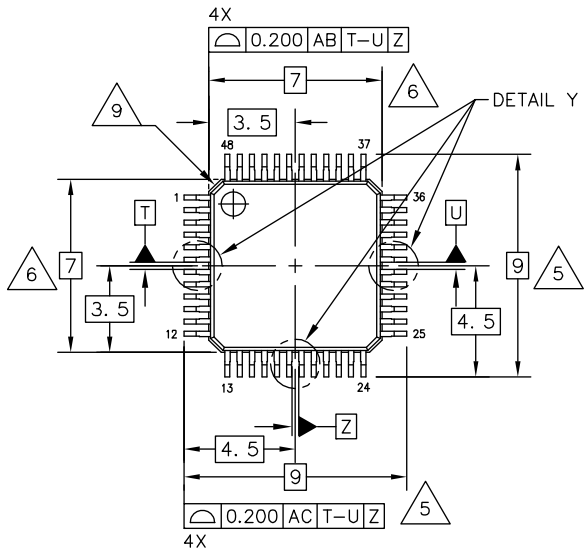
Table 490. Program D-Flash Command FCCOB Requirements

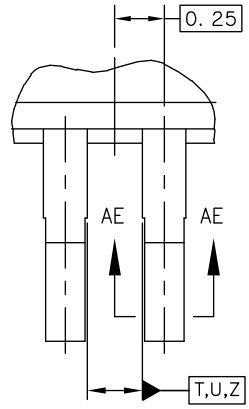
CCOBIX[2:0]	FCCOB Parameters	
000	0x11	Global address [17:16] to identify the D-Flash block
001	Global address [15:0] of word to be programmed	
010	Word 0 program value	
011	Word 1 program value, if desired	
100	Word 2 program value, if desired	
101	Word 3 program value, if desired	

Upon clearing CCIF to launch the Program D-Flash command, the user-supplied words will be transferred to the Memory Controller and be programmed if the area is unprotected. The CCOBIX index value at Program D-Flash command launch determines how many words will be programmed in the D-Flash block. The CCIF flag is set when the operation has completed.

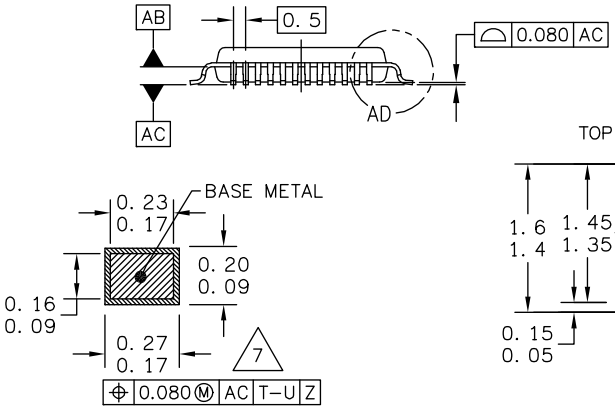
Table 491. Program D-Flash Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] < 010 at command launch
		Set if CCOBIX[2:0] > 101 at command launch
		Set if command not available in current mode (see Table 456)
		Set if an invalid global address [17:0] is supplied
		Set if a misaligned word address is supplied (global address [0] != 0)
		Set if the requested group of words breaches the end of the D-Flash block
	FPVIOL	Set if the selected area of the D-Flash memory is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

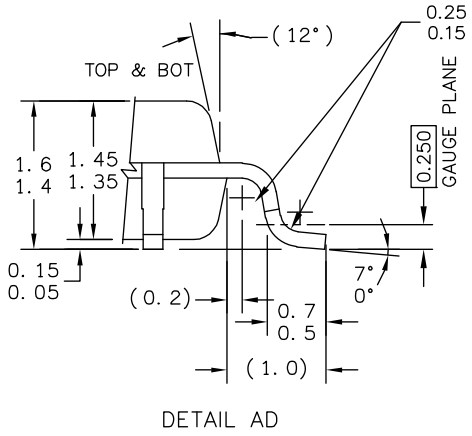




DETAIL Y



SECTION AE–AE



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