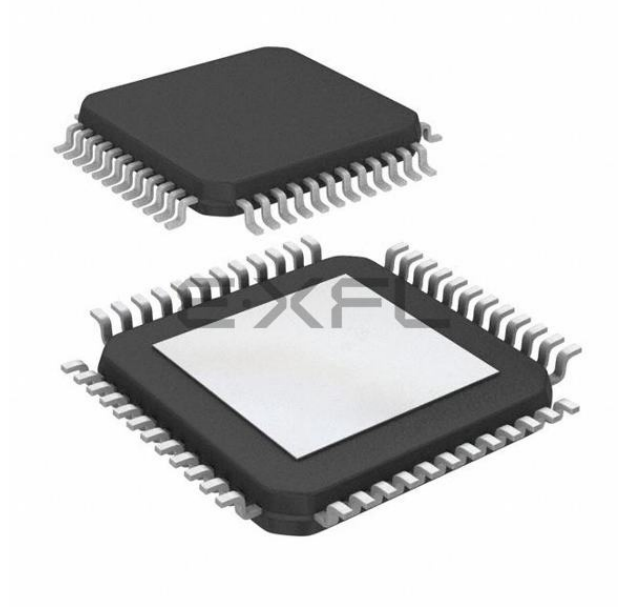

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4.4 Supply Currents

This section describes the current consumption characteristics of the device as well as the conditions for the measurements.

4.4.1 Measurement Conditions

All measurements are without output loads. Currents are measured in MCU special single chip mode and the CPU code is executed from RAM, unless otherwise noted.

Table 10. Supply Currents

Ratings	Symbol	Min	Typ[19]	Max	Unit
Normal Mode analog die only, excluding external loads, LIN Recessive State (5.5 V ≤ V_{SUP} ≤ 18 V, 2.25 V ≤ V_{DD} ≤ 2.75 V, 4.5 V ≤ V_{DDX} ≤ 5.5 V, -40 °C ≤ T_{J_A} ≤ 150 °C).	I_{RUN_A}	-	5.0	8.0	mA
Normal Mode MCU die only (T_{J_M}=150 °C; V_{DDD2D} = 2.75 V, V_{DDRX} = 5.5 V, f_{OSC} = 4.0 MHz, f_{BUS}= f_{BUSMAX}[20][21]	I_{RUN_M}	-	18	20	mA
Stop Mode internal analog die only, excluding external loads, LIN Recessive State, Lx enabled, measured at VS1+VS2 (5.5 V ≤ V_{SUP} ≤ 18 V, 2.25 V ≤ V_{DD} ≤ 2.75 V, 4.5 V ≤ V_{DDX} ≤ 5.5 V) -40 °C ≤ T_{J_A} ≤ 125 °C	I_{STOP_A}	 -	 20	 40	µA
Stop Mode MCU die only (V_{DDD2D} = 2.75 V, V_{DDRX} = 5.5 V, f_{OSC}= 4.0 MHz; MCU in STOP; RTI and COP off)[22] T_{J_M}=150°C T_{J_M}=-40°C T_{J_M}=25°C	I_{STOP_M}	 - - -	 85 31 31	 150 50 50	µA
Sleep Mode (VDD = VDDX = OFF; 5.5 V ≤ V_{SUP} ≤ 18 V; -40 °C ≤ T_{J_A} ≤ 125 °C; 3.0 V > Lx > 1.0 V)	I_{SLEEP}	-	15	28	µA
Cyclic Sense Supply Current Adder (5.0 ms Cycle)	I_{CS}	-	15	20	µA

Note:

19. Typical values noted reflect the approximate parameter mean at T_A = 25 °C
20. f_{BUSMAX} frequency ratings differ by device and is specified in Table 1
21. I_{RUN_M} denotes the sum of the currents flowing into VDD and VDDX.
22. I_{STOP_M} denotes the sum of the currents flowing into VDD and VDDX.

Assuming that no non-blank location is found, then the time to erase verify a D-Flash block is given by:

$$t_{dcheck} = 2800 \cdot \frac{1}{f_{NVMBUS}}$$

4.6.2.1.1.3 Erase Verify P-Flash Section (FCMD=0x03)

The maximum time to erase verify a section of P-Flash depends on the number of phrases being verified (N_{VP}) and is given by:

$$t \approx (450 + N_{VP}) \cdot \frac{1}{f_{NVMBUS}}$$

4.6.2.1.1.4 Read Once (FCMD=0x04)

The maximum read once time is given by:

$$t = 400 \cdot \frac{1}{f_{NVMBUS}}$$

4.6.2.1.1.5 Program P-Flash (FCMD=0x06)

The programming time for a single phrase of four P-Flash words and the two seven-bit ECC fields is dependent on the bus frequency, f_{NVMBUS}, as well as on the NVM operating frequency, f_{NVMOP}.

The typical phrase programming time is given by:

$$t_{ppgm} \approx 164 \cdot \frac{1}{f_{NVMOP}} + 2000 \cdot \frac{1}{f_{NVMBUS}}$$

The maximum phrase programming time is given by:

$$t_{ppgm} \approx 164 \cdot \frac{1}{f_{NVMOP}} + 2500 \cdot \frac{1}{f_{NVMBUS}}$$

4.6.2.1.1.6 Program Once (FCMD=0x07)

The maximum time required to program a P-Flash Program Once field is given by:

$$t \approx 164 \cdot \frac{1}{f_{NVMOP}} + 2150 \cdot \frac{1}{f_{NVMBUS}}$$

4.6.2.1.1.7 Erase All Blocks (FCMD=0x08)

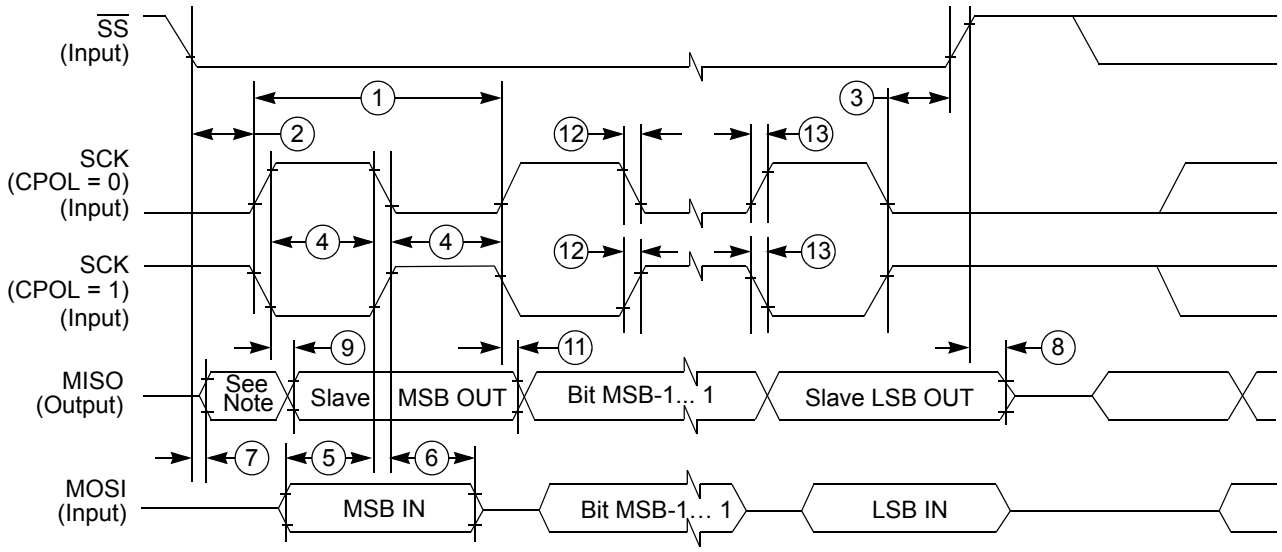
The time required to erase all blocks is given by:

$$t_{mass} \approx 100100 \cdot \frac{1}{f_{NVMOP}} + 38000 \cdot \frac{1}{f_{NVMBUS}}$$

4.6.2.1.1.8 Erase P-Flash Block (FCMD=0x09)

The time required to erase the P-Flash block is given by:

$$t_{pmass} \approx 100100 \cdot \frac{1}{f_{NVMOP}} + 35000 \cdot \frac{1}{f_{NVMBUS}}$$



NOTE: Not defined

Figure 15. SPI Slave Timing (CPHA = 1)

In Table 47 the timing characteristics for slave mode are listed.

Table 47. SPI Slave Mode Timing Characteristics

Characteristic	Symbol	Min	Typ	Max	Unit
SCK Frequency	f_{SCK}	DC	—	1/4	f_{BUS}
SCK Period	t_{SCK}	4	—	∞	t_{BUS}
Enable Lead Time	t_{LEAD}	4	—	—	t_{BUS}
Enable Lag Time	t_{LAG}	4.0	—	—	t_{BUS}
Clock (SCK) High or Low Time	t_{WSCK}	4.0	—	—	t_{BUS}
Data Setup Time (inputs)	t_{SU}	8.0	—	—	ns
Data Hold Time (inputs)	t_{HI}	8.0	—	—	ns
Slave Access Time (time to data active)	t_A	—	—	20	ns
Slave MISO Disable Time	t_{DIS}	—	—	22	ns
Data Valid After SCK Edge	t_{VSCK}	—	—	$29 + 0.5 \cdot t_{BUS}$ (57)	ns
Data Valid After $\overline{SS}$ Fall	t_{VSS}	—	—	$29 + 0.5 \cdot t_{BUS}$ (57)	ns
Data Hold Time (outputs)	t_{HO}	20	—	—	ns
Rise and Fall Time Inputs	t_{RFI}	—	—	8.0	ns
Rise and Fall Time Outputs	t_{RFO}	—	—	8.0	ns

Note:
57. 0.5 t_{BUS} added due to internal synchronization delay

4.7 Thermal Protection Characteristics

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Table 48. Thermal Characteristics - Voltage Regulators VDD (2.5 V) & VDDX (5.0 V)[58]

Ratings	Symbol	Min	Typ	Max	Unit
VDD/VDDX High-temperature Warning (HTI) Threshold Hysteresis	 T_{HTI} T_{HTI_H}	 110 -	 125 10	 140 -	 °C
VDD/VDDX Over-temperature Shutdown Threshold Hysteresis	 T_{SD} T_{SD_H}	 155 -	 170 10	 185 -	 °C
HSUP Over-temperature Shutdown	T_{HSUPSD}	150	165	180	°C
HSUP Over-temperature Shutdown Hysteresis	T_{HSUPSD_HYS}	-	10	-	°C
HS Over-temperature Shutdown	T_{HSSD}	150	165	180	°C
HS Over-temperature Shutdown Hysteresis	T_{HSSD_HYS}	-	10	-	°C
LS Over-temperature Shutdown	T_{LSSD}	150	165	180	°C
LS Over-temperature Shutdown Hysteresis	T_{LSSD_HYS}	-	10	-	°C
LIN Over-temperature Shutdown	T_{LINSD}	150	165	200	°C
LIN Over-temperature Shutdown Hysteresis	T_{LINSD_HYS}	-	20	-	°C

Note:
58. Guaranteed by characterization. Functionality tested.

4.8 ESD Protection and Latch-up Immunity

All ESD testing is in conformity with CDF-AEC-Q100 stress test qualification for automotive grade integrated circuits. During the device qualification, ESD stresses were performed for the Human Body Model (HBM), Machine Model (MM), Charge Device Model (CDM), as well as LIN transceiver specific specifications.

A device will be defined as a failure if after exposure to ESD pulses, the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature, followed by hot temperature, unless specified otherwise in the device specification.

Table 49. ESD and Latch-up Protection Characteristics

Ratings	Symbol	Value	Unit
ESD - Human Body Model (HBM) following AEC-Q100 / JESD22-A114 (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω) - LIN (DGND, PGND, AGND, and LGND shorted) - VS1, VS2, VSENSE, Lx - HSx - All other Pins	V_{HBM}	 ±8000 ±4000 ±3000 ±2000	V
ESD - Charged Device Model (CDM) following AEC-Q100, Corner Pins (1, 12, 13, 24, 25, 36, 37, and 48) All other Pins	V_{CDM}	 ±750 ±500	V
ESD - Machine Model (MM) following AEC-Q100 (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω), All Pins	V_{MM}	±200	V
Latch-up current at T_A = 125 °C[59]	I_{LAT}	±100	mA

Table 69. 0x0120 Port Integration Module (PIM) Map 3 of 3

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0120	PTIA	R	PTIA7	PTIA6	PTIA5	PTIA4	PTIA3	PTIA2	PTIA1	PTIA0
		W								
0x0121	PTIB	R	0	0	0	0	0	0	PTIB1	PTIB0
		W								
0x0122-0x017F	Reserved	R	0	0	0	0	0	0	0	0
		W								

Table 70. 0x0180–0x1EF Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0180-0x01EF	Reserved	R	0	0	0	0	0	0	0	0
		W								

Table 71. 0x01F0–0x01FF Clock and Power Management (CPMU) Map 2 of 2

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x01F0	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x01F1	CPMU LVCTL	R	0	0	0	0	0	LVDS	LVIE	LVIF
		W								
0x01F6	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x01F7	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x01F8	CPMU IRCTRIMH	R	TCTRIM[3:0]				0	0	IRCTRIM[9:8]	
		W								
0x01F9	CPMU IRCTRIML	R	IRCTRIM[7:0]							
		W								
0x01FA	CPMUOSC	R	OSCE	OSCBW	OSCPINS_EN	OSCFILT[4:0]				
		W								
0x01FB	CPMUPROT	R	0	0	0	0	0	0	0	PROT
		W								
0x01FC	Reserved	R	0	0	0	0	0	0	0	0
		W								

Table 72. 0x01FD–0x1FF Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x01FD-0x01FF	Reserved	R	0	0	0	0	0	0	0	0
		W								

5.5.3 Register Definition

5.5.3.1 Voltage Control Register (VCR)

Table 83. Voltage Control Register (VCR)

Offset[69] 0x04 Access: User read/write

	7	6	5	4	3	2	1	0
R	0	0	0	VROVIE	HTIE	HVIE	LVIE	LBIE
W								
Reset	0	0	0	0	0	0	0	0

Note:

69. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 84. VCR - Register Field Descriptions

Field	Description
4 VROVIE	Voltage Regulator Over-voltage Interrupt Enable — Enables the interrupt for the Regulator Over-voltage Condition. 0 - Voltage Regulator Over-voltage Interrupt is disabled 1 - Voltage Regulator Over-voltage Interrupt is enabled
3 HTIE	High Temperature Interrupt Enable — Enables the interrupt for the Voltage Regulator (VDD/VDDX) Temperature Warning. 0 - High Temperature Interrupt is disabled 1 - High Temperature Interrupt is enabled
2 HVIE	High Voltage Interrupt Enable — Enables the interrupt for the VS2 - High Voltage Warning. 0 - High Voltage Interrupt is disabled 1 - High Voltage Interrupt is enabled
1 LVIE	Low Voltage Interrupt Enable — Enables the interrupt for the VS1 - Low Voltage Warning. 0 - Low Voltage Interrupt is disabled 1 - Low Voltage Interrupt is enabled
0 LBIE	Low Battery Interrupt Enable — Enables the interrupt for the VSENSE - Low Battery Voltage Warning. 0 - Low Battery Interrupt is disabled 1 - Low Battery Interrupt is enabled

5.5.3.2 Voltage Status Register (VSR)

Table 85. Voltage Status Register (VSR)

Offset[70] 0x05 Access: User read

	7	6	5	4	3	2	1	0
R	0	0	0	VROVC	HTC	HVC	LVC	LBC
W								
Reset	0	0	0	0	0	0	0	0

Note:

70. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 93. RSR - Register Field Descriptions

Field	Description
5 - WDR	Watchdog Reset - Reset caused by an incorrect serving of the watchdog.
4 - EXR	External Reset - Reset caused by the $\overline{\text{RESET\_A}}$ pin driven low externally for > tRSTDF.
3 - WUR	Wake-up Reset - Reset caused by a wake-up from Sleep mode. To determine the wake-up source, refer to Section 5.9, “Wake-up / Cyclic Sense".
2 - LVRX	Low Voltage Reset VDDX - Reset caused by a low voltage condition monitored at the VDDX output.
1 - LVR	Low Voltage Reset VDD - Reset caused by a low voltage condition monitored at the VDD output.(74)
0 - POR	Power On Reset - Supply Voltage was below V_{POR}.

Note:

74. As the VDD Regulator is shutdown once a LVRX condition is detected, The actual cause could be also a low voltage condition at the VDDX regulator.

Reading the Reset Status register will clear the information inside. Writing has no effect. LVR and LVRX are masked when POR or WUR are set.

5.27.4 Part ID Assignments

The part ID is located in two 8-bit registers PARTIDH and PARTIDL (addresses 0x001A and 0x001B). The read-only value is a unique part ID for each revision of the chip. Table 222 shows the assigned part ID number and Mask Set number.

The Version ID in Table 222 is a word located in a flash information row. The version ID number indicates a specific version of internal NVM controller.

Table 222. Assigned Part ID Numbers

Device	Mask Set Number	Part ID[154]	Version ID
MC9S12I64	0N53A	0x38C0	0x0000

Note:

154. The coding is as follows:
Bit 15-12: Major family identifier
Bit 11-6: Minor family identifier
Bit 5-4: Major mask set revision number including FAB transfers
Bit 3-0: Minor — non full — mask set revision

5.27.5 System Clock Description

For the system clock description please refer to 5.38, “S12 Clock, Reset and Power Management Unit (S12CPMU)”.

5.27.6 Modes of Operation

The MCU can operate in different modes. These are described in Section 5.27.6.1, “Chip Configuration Summary". The MCU can operate in different power modes to facilitate power saving when full system performance is not required. These are described in Section 5.27.6.2, “Low Power Operation". Some modules feature a software programmable option to freeze the module status whilst the background debug module is active to facilitate debugging.

5.27.6.1 Chip Configuration Summary

The different modes and the security state of the MCU affect the debug features (enabled or disabled).

The operating mode out of reset is determined by the state of the MODC signal during reset (see Table 223). The MODC bit in the MODE register shows the current operating mode and provides limited mode switching during operation. The state of the MODC signal is latched into this bit on the rising edge of $\overline{\text{RESET}}$.

Table 223. Chip Modes

Chip Modes	MODC
Normal single chip	1
Special single chip	0

5.27.6.1.1 Normal Single-Chip Mode

This mode is intended for normal device operation. The opcode from the on-chip memory is being executed after reset (requires the reset vector to be programmed correctly). The processor program is executed from internal memory.

5.27.6.1.2 Special Single-Chip Mode

This mode is used for debugging single-chip operation, boot-strapping, or security related operations. The background debug module BDM is active in this mode. The CPU executes a monitor program located in an on-chip ROM. BDM firmware waits for additional serial commands through the BKGD pin.

5.27.6.2 Low Power Operation

The MM912_634 has two static low-power modes Pseudo Stop and Stop Mode. For a detailed description refer to S12CPMU section.

5.27.7 Security

The MCU security mechanism prevents unauthorized access to the Flash memory. Refer to 5.33, “Security (S12X9SECV2)”, Section 5.31.4.1, “Security"", and Section 5.40.5, “Security".

Table 231. PORTE Register Field Descriptions

Field	Description
1 PE	**Port E general purpose input/output data**—Data Register, CPMU OSC XTAL signal When not used with the alternative function, this pin can be used as general purpose I/O. In general purpose output mode the register bit is driven to the pin. If the associated data direction bit of this pin is set to 1, a read returns the value of the port register, otherwise the buffered pin input state is read. • The CPMU OSC function takes precedence over the general purpose I/O function if enabled.
0 PE	**Port E general purpose input/output data**—Data Register, CPMU OSC EXTAL signal When not used with the alternative function, this pin can be used as general purpose I/O. In general purpose output mode the register bit is driven to the pin. If the associated data direction bit of this pin is set to 1, a read returns the value of the port register, otherwise the buffered pin input state is read. • The CPMU OSC function takes precedence over the general purpose I/O function if enabled.

5.28.2.4 Port A Data Direction Register (DDRA)

Table 232. Port A Data Direction Register (DDRA)

Address 0x0002 Access: User read/write(158)

	7	6	5	4	3	2	1	0
R W	DDRA7	DDRA6	DDRA5	DDRA4	DDRA3	DDRA2	DDRA1	DDRA0
Reset	0	0	0	0	0	0	0	0

Note:
158. Read: Anytime.
Write: Anytime.

Table 233. DDRA Register Field Descriptions

Field	Description
7–4 DDRA	**Port A Data Direction**— This bit determines whether the associated pin is an input or output. 1 Associated pin is configured as output. 0 Associated pin is configured as input.
3–0 DDRA	**Port A Data Direction**— This bit determines whether the associated pin is an input or output. Depending on the configuration of the enabled SPI the I/O state will be forced to input or output. In this case the data direction bits will not change. 1 Associated pin is configured as output. 0 Associated pin is configured as input.

5.28.2.5 Port E Data Direction Register (DDRE)

Table 234. Port E Data Direction Register (DDRE)

Address 0x0003 Access: User read/write(159)

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	DDRE1	DDRE0
W								
Reset	0	0	0	0	0	0	0	0

Note:
159. Read: Anytime.
Write: Anytime.

Table 250. MODE Field Descriptions

Field	Description
7 MODC	Mode Select Bit — This bit controls the current operating mode during RESET high (inactive). The external mode pin MODC determines the operating mode during $\overline{\text{RESET}}$ low (active). The state of the pin is registered into the respective register bit after the $\overline{\text{RESET}}$ signal goes inactive (see Figure 45). Write restrictions exist to disallow transitions between certain modes. Figure 45 illustrates all allowed mode changes. Attempting non authorized transitions will not change the MODE bit, but it will block further writes to the register bit except in special modes. Write accesses to the MODE register are blocked when the device is secured.

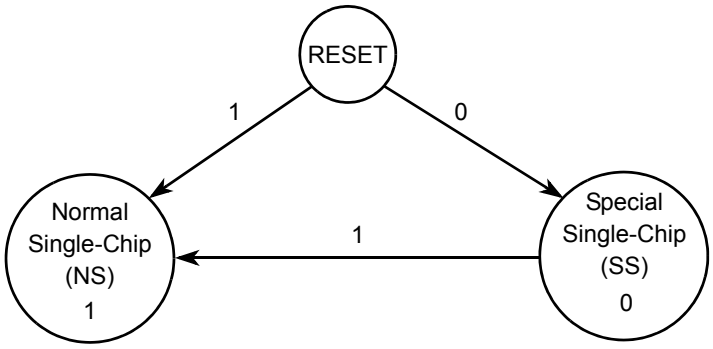


Figure 45. Mode Transition Diagram When MCU is Unsecured

5.29.3.2.2 Direct Page Register (DIRECT)

Table 251. Direct Register (DIRECT)

Address: 0x0011

	7	6	5	4	3	2	1	0
R W	DP15	DP14	DP13	DP12	DP11	DP10	DP9	DP8
Reset	0	0	0	0	0	0	0	0

Read: Anytime

Write: anytime in special SS, write-one in NS.

This register determines the position of the 256 Byte direct page within the memory map.It is valid for both global and local mapping scheme.

Table 252. DIRECT Field Descriptions

Field	Description
7–0 DP[15:8]	Direct Page Index Bits 15–8 — These bits are used by the CPU when performing accesses using the direct addressing mode. These register bits form bits [15:8] of the local address (see Figure 46).

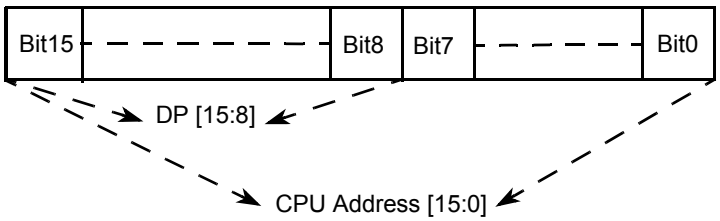


Figure 46. DIRECT Address Mapping

Example 1. This example demonstrates usage of the Direct Addressing Mode

```
MOVB    #$80,DIRECT     ;Set DIRECT register to 0x80. Write once only.
                        ;Global data accesses to the range 0xXX_80XX can be direct.
                        ;Logical data accesses to the range 0x80XX are direct.

LDY     <$00            ;Load the Y index register from 0x8000 (direct access).
                        ;< operator forces direct access on some assemblers but in
                        ;many cases assemblers are “direct page aware” and can
                        ;automatically select direct mode.
```

5.29.3.2.3 Program Page Index Register (PPAGE)

Table 253. Program Page Index Register (PPAGE)

Address: 0x0015

	7	6	5	4	3	2	1	0
R	0	0	0	0	PIX3	PIX2	PIX1	PIX0
W								
Reset	0	0	0	0	1	1	1	0

Read: Anytime

Write: Anytime

These four index bits are used to map 16 kB blocks into the Flash page window located in the local (CPU or BDM) memory map from address 0x8000 to address 0xBFFF (see Figure 47). This supports accessing up to 256 kB of Flash (in the Global map) within the 6 kB Local map. The PPAGE index register is effectively used to construct paged Flash addresses in the Local map format. The CPU has special access to read and write this register directly during execution of CALL and RTC instructions.

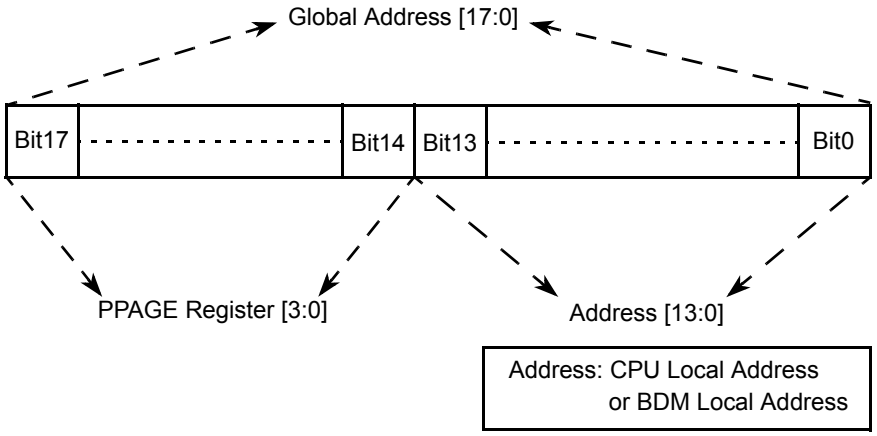


Figure 47. PAGE Address Mapping

NOTE

Writes to this register using the special access of the CALL and RTC instructions will be complete before the end of the instruction execution.

5.30.1.4 Block Diagram

Figure 52 shows a block diagram of the INT module.

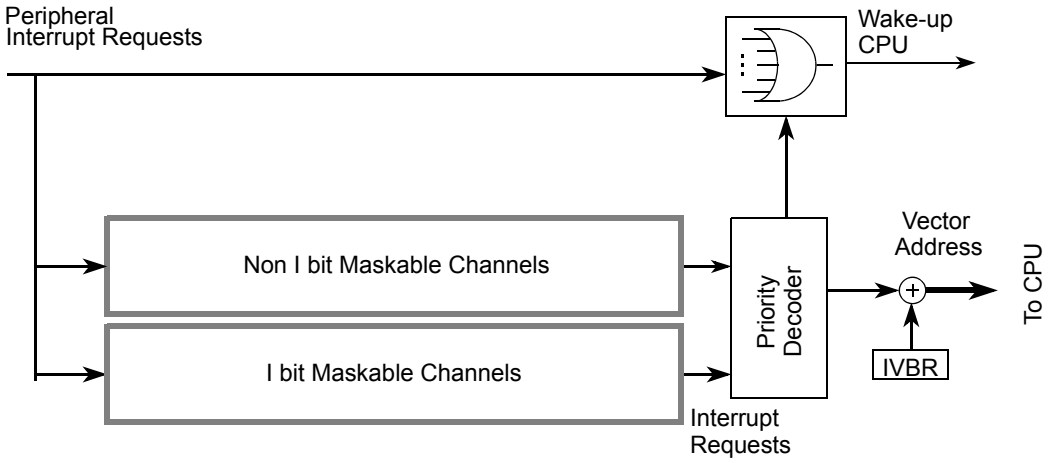


Figure 52. INT Block Diagram

5.30.2 External Signal Description

The INT module has no external signals.

5.30.3 Memory Map and Register Definition

This section provides a detailed description of all registers accessible in the INT module.

5.30.3.1 Register Descriptions

This section describes in address order all the INT registers and their individual bits.

5.30.3.1.1 Interrupt Vector Base Register (IVBR)

Table 257. Interrupt Vector Base Register (IVBR)

Address: 0x001F

	7	6	5	4	3	2	1	0
R W	IVB_ADDR[7:0]							
Reset	1	1	1	1	1	1	1	1

Read: Anytime

Write: Anytime

Table 258. IVBR Field Descriptions

Field	Description
7–0 IVB_ADDR[7:0]	Interrupt Vector Base Address Bits — These bits represent the upper byte of all vector addresses. Out of reset these bits are set to 0xFF (i.e., vectors are located at 0xFF80–0xFFFE) to ensure compatibility to HCS12. Note: A system reset will initialize the interrupt vector base register with “0xFF” before it is used to determine the reset vector address. Therefore, changing the IVBR has no effect on the location of the three reset vectors (0xFFFA–0xFFFE). Note: If the BDM is active (i.e., the CPU is in the process of executing BDM firmware code), the contents of IVBR are ignored and the upper byte of the vector address is fixed as “0xFF”. This is done to enable handling of all non-maskable interrupts in the BDM firmware.

Table 270. Quick Reference to DBG Registers

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x002E	DBGADHM	R W	Bit 15	14	13	12	11	10	9	Bit 8
0x002F	DBGADLM	R W	Bit 7	6	5	4	3	2	1	Bit 0

Note:

184. This bit is visible at DBGCNT[7] and DBGSR[7]
185. This represents the contents if the Comparator A control register is blended into this address.
186. This represents the contents if the Comparator B control register is blended into this address.
187. This represents the contents if the Comparator C control register is blended into this address.

5.32.3.2 Register Descriptions

This section consists of the DBG control and trace buffer register descriptions in address order. Each comparator has a bank of registers that are visible through an 8-byte window between 0x0028 and 0x002F in the DBG module register address map. When ARM is set in DBGC1, the only bits in the DBG module registers that can be written are ARM, TRIG, and COMRV[1:0]

5.32.3.2.1 Debug Control Register 1 (DBGC1)

Table 271. Debug Control Register (DBGC1)

Address: 0x0020

	7	6	5	4	3	2	1	0
R	ARM	0	0	BDM	DBGBRK	0	COMRV	
W		TRIG						
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Read: Anytime

Write: Bits 7, 1, 0 anytime
Bit 6 can be written anytime but always reads back as 0.
Bits 4:3 anytime DBG is not armed.

NOTE

When disarming the DBG by clearing ARM with software, the contents of bits[4:3] are not affected by the write, since up until the write operation, ARM = 1 preventing these bits from being written. These bits must be cleared using a second write if required.

NOTE:

When tracing is terminated using forced breakpoints, latency in breakpoint generation means that opcodes following the opcode causing the breakpoint can be stored to the trace buffer. The number of opcodes is dependent on program flow. This can be avoided by using tagged breakpoints.

5.32.4.5.3 Trace Buffer Organization (Normal, Loop1, Detail modes)

ADRH, ADRM, ADRL denote address high, middle and low byte respectively. The numerical suffix refers to the tracing count. The information format for Loop1 and Normal modes is identical. In Detail mode, the address and data for each entry are stored on consecutive lines, thus the maximum number of entries is 32. In this case DBGCNT bits are incremented twice, once for the address line and once for the data line, on each trace buffer entry. In Detail mode CINF comprises of R/W and size access information (CRW and CSZ respectively).

Single byte data accesses in Detail Mode are always stored to the low byte of the trace buffer (DATAL) and the high byte is cleared. When tracing word accesses, the byte at the lower address is always stored to trace buffer byte1 and the byte at the higher address is stored to byte0.

Table 325. Trace Buffer Organization (Normal,Loop1,Detail modes)

Mode	Entry Number	4-bits	8-bits	8-bits
		Field 2	Field 1	Field 0
Detail Mode	Entry 1	CINF1,ADRH1	ADRM1	ADRL1
		0	DATAH1	DATAL1
	Entry 2	CINF2,ADRH2	ADRM2	ADRL2
		0	DATAH2	DATAL2
Normal/Loop1 Modes	Entry 1	PCH1	PCM1	PCL1
	Entry 2	PCH2	PCM2	PCL2

5.32.4.5.3.1 Information Bit Organization

The format of the bits is dependent upon the active trace mode as described below.

Field2 Bits in Detail Mode

Table 326. Field2 Bits in Detail Mode

Bit 3	Bit 2	Bit 1	Bit 0
CSZ	CRW	ADDR[17]	ADDR[16]

In Detail Mode the CSZ and CRW bits indicate the type of access being made by the CPU.

Table 327. Field Descriptions

Bit	Description
3 CSZ	**Access Type Indicator** — This bit indicates if the access was a byte or word size when tracing in Detail Mode 0 Word Access 1 Byte Access
2 CRW	**Read Write Indicator** — This bit indicates if the corresponding stored address corresponds to a read or write access when tracing in Detail Mode. 0 Write Access 1 Read Access
1 ADDR[17]	**Address Bus bit 17** — Corresponds to system address bus bit 17.
0 ADDR[16]	**Address Bus bit 16** — Corresponds to system address bus bit 16.

following the second M2, before M1 resets to State1 then a trigger is generated. Configuring CompA and CompC the same, it is possible to generate a breakpoint on the third consecutive occurrence of event M0 without a reset M1.

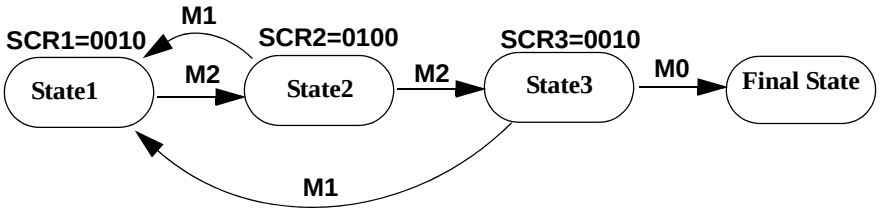


Figure 79. Scenario 10a

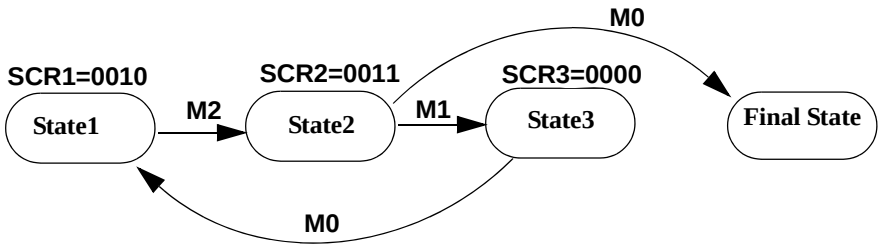


Figure 80. Scenario 10b

Scenario 10b shows the case that after M2 then M1 must occur before M0. Starting from a particular point in code, event M2 must always be followed by M1 before M0. If after any M2, event M0 occurs before M1 then a trigger is generated.

Table 380. S12CPMU IRC1M Trim Low Register (CPMUIRCTRIML)

0x02F9

	7	6	5	4	3	2	1	0
R W	IRCTRIM[7:0]							
Reset	F	F	F	F	F	F	F	F
Reset	1	1	1	1	1	1	1	1

Note:

200. After de-assert of System Reset a factory programmed trim value is automatically loaded from the Flash memory to provide trimmed Internal Reference Frequency f_{IRC1M_TRIM}.

Read: Anytime

Write: Anytime if PROT=0 (CPMUPROT register). Else write has no effect

NOTE

Writes to these registers while PLLSEL=1 clears the LOCK and UPOSC status bits.

Table 381. CPMUIRCTRIMH/L Field Descriptions

Field	Description
15-11 TCTRIM	**IRC1M temperature coefficient Trim Bits** Trim bits for the Temperature Coefficient (TC) of the IRC1M frequency. Figure 86 shows the influence of the bits TCTRIM4:0] on the relationship between frequency and temperature. Figure 86 shows an approximate TC variation, relative to the nominal TC of the IRC1M (i.e. for TCTRIM[4:0]=0x00000 or 0x10000).
9-0 IRCTRIM	**IRC1M Frequency Trim Bits** — Trim bits for Internal Reference Clock After System Reset the factory programmed trim value is automatically loaded into these registers, resulting in an Internal Reference Frequency f_{IRC1M_TRIM}. See device electrical characteristics for value of f_{IRC1M_TRIM}. The frequency trimming consists of two different trimming methods: A rough trimming controlled by bits IRCTRIM[9:6] can be done with frequency leaps of about 6% in average. A fine trimming controlled by the bits IRCTRIM[5:0] can be done with frequency leaps of about 0.3% (this trimming determines the precision of the frequency setting of 0.15%, i.e. 0.3% is the distance between two trimming values). Figure 85 shows the relationship between the trim bits and the resulting IRC1M frequency.

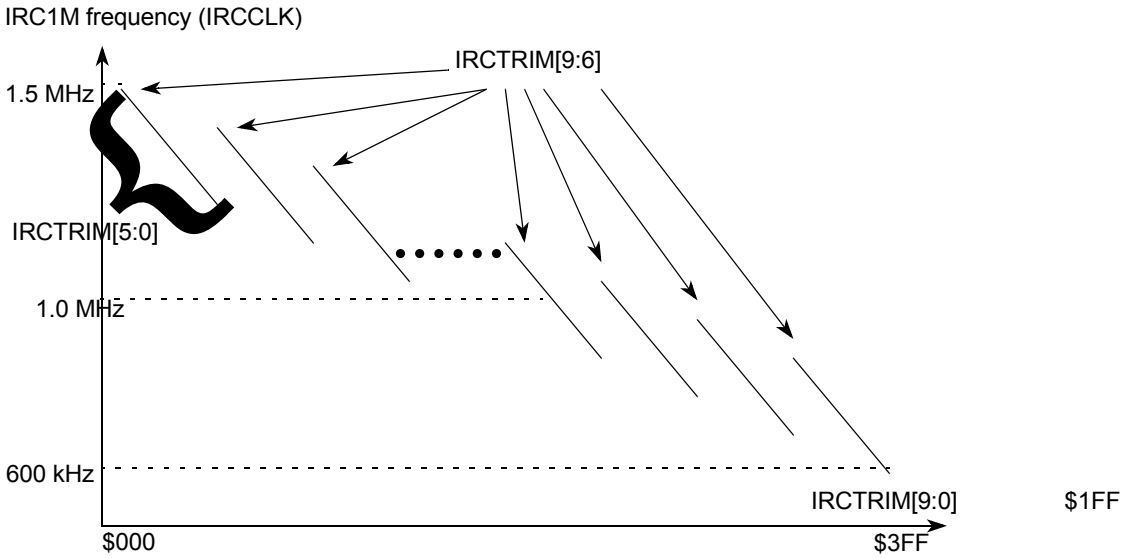


Figure 85. IRC1M Frequency Trimming Diagram

Table 414. FTMRC64K1 Register Summary

Address & Name		7	6	5	4	3	2	1	0
FCLKDIV	R	FDIVLD	FDIVLCK	FDIV5	FDIV4	FDIV3	FDIV2	FDIV1	FDIV0
	W								
FSEC	R	KEYEN1	KEYEN0	RNV5	RNV4	RNV3	RNV2	SEC1	SEC0
	W								
FCCOBIX	R	0	0	0	0	0	CCOBIX2	CCOBIX1	CCOBIX0
	W								
FRSV0	R	0	0	0	0	0	0	0	0
	W								
FCNFG	R	CCIE	0	0	IGNSF	0	0	FDFD	FSFD
	W								
FERCNFG	R	0	0	0	0	0	0	DFDIE	SFDIE
	W								
FSTAT	R	CCIF	0	ACCERR	FPVIOL	MGBUSY	RSVD	MGSTAT1	MGSTAT0
	W								
FERSTAT	R	0	0	0	0	0	0	DFDIF	SFDIF
	W								
DFPROT	R	DPOPEN	0	0	0	DPS3	DPS2	DPS1	DPS0
	W								
FCCOBHI	R	CCOB15	CCOB14	CCOB13	CCOB12	CCOB11	CCOB10	CCOB9	CCOB8
	W								
FCCOBLO	R	CCOB7	CCOB6	CCOB5	CCOB4	CCOB3	CCOB2	CCOB1	CCOB0
	W								
FRSV1	R	0	0	0	0	0	0	0	0
	W								
FRSV2	R	0	0	0	0	0	0	0	0
	W								
FRSV3	R	0	0	0	0	0	0	0	0
	W								
FRSV4	R	0	0	0	0	0	0	0	0
	W								
FOPT	R	NV7	NV6	NV5	NV4	NV3	NV2	NV1	NV0
	W								
FRSV5	R	0	0	0	0	0	0	0	0
	W								
FRSV6	R	0	0	0	0	0	0	0	0
	W								
FRSV7	R	0	0	0	0	0	0	0	0
	W								

= Unimplemented or Reserved

Table 430. FSTAT Field Descriptions (continued)

Field	Description
2 RSVD	**Reserved Bit** — This bit is reserved and always reads 0.
1–0 MGSTAT[1:0]	**Memory Controller Command Completion Status Flag** — One or more MGSTAT flag bits are set if an error is detected during execution of a Flash command or during the Flash reset sequence. See Section 5.40.4.5, “Flash Command Description" and Section 5.40.6, “Initialization" for details.

5.40.3.2.8 Flash Error Status Register (FERSTAT)

The FERSTAT register reflects the error status of internal Flash operations.

Table 431. Flash Error Status Register (FERSTAT)

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	DFDIF	SFDIF
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

All flags in the FERSTAT register are readable and only writable to clear the flag.

Table 432. FERSTAT Field Descriptions

Field	Description
1 DFDIF	**Double Bit Fault Detect Interrupt Flag** — The setting of the DFDIF flag indicates that a double bit fault was detected in the stored parity and data bits during a Flash array read operation, or that a Flash array read operation was attempted on a Flash block that was under a Flash command operation.(220) The DFDIF flag is cleared by writing a 1 to DFDIF. Writing a 0 to DFDIF has no effect on DFDIF. 0 No double bit fault detected 1 Double bit fault detected or an invalid Flash array read operation attempted
0 SFDIF	**Single Bit Fault Detect Interrupt Flag** — With the IGNSF bit in the FCNFG register clear, the SFDIF flag indicates that a single bit fault was detected in the stored parity and data bits during a Flash array read operation, or that a Flash array read operation was attempted on a Flash block that was under a Flash command operation. (220) The SFDIF flag is cleared by writing a 1 to SFDIF. Writing a 0 to SFDIF has no effect on SFDIF. 0 No single bit fault detected 1 Single bit fault detected and corrected or an invalid Flash array read operation attempted

Note:

220. The single bit fault and double bit fault flags are mutually exclusive for parity errors (an ECC fault occurrence can be either single fault or double fault, but never both). A simultaneous access collision (read attempted while command running) is indicated when both SFDIF and DFDIF flags are high.

5.40.3.2.9 P-Flash Protection Register (FPROT)

The FPROT register defines which P-Flash sectors are protected against program and erase operations.

Table 433. P-Flash Protection Register (FPROT)

	7	6	5	4	3	2	1	0
R	FPOPEN	RNV6	FPHDIS	FPHS[1:0]		FPLDIS	FPLS[1:0]	
W								
Reset	F	F	F	F	F	F	F	F

= Unimplemented or Reserved

5.40.4.2 IFR Version ID Word

The version ID word is stored in the IFR at address 0x0_40B6. The contents of the word are defined in Table 455.

Table 455. IFR Version ID Fields

[15:4]	[3:0]
Reserved	VERNUM

VERNUM: Version number. The first version is number 0b_0001 with both 0b_0000 and 0b_1111 meaning ‘none’.

5.40.4.3 Flash Command Operations

Flash command operations are used to modify Flash memory contents.

The next sections describe:

- How to write the FCLKDIV register that is used to generate a time base (FCLK) derived from BUSCLK for Flash program and erase command operations
- The command write sequence used to set Flash command parameters and launch execution
- Valid Flash commands available for execution

5.40.4.3.1 Writing the FCLKDIV Register

Prior to issuing any Flash program or erase command after a reset, the user is required to write the FCLKDIV register to divide BUSCLK down to a target FCLK of 1 MHz. Table 417 shows recommended values for the FDIV field based on BUSCLK frequency.

NOTE

Programming or erasing the Flash memory cannot be performed if the bus clock runs at less than 0.8 MHz. Setting FDIV too high can destroy the Flash memory due to overstress. Setting FDIV too low can result in incomplete programming or erasure of the Flash memory cells.

When the FCLKDIV register is written, the FDIVLD bit is set automatically. If the FDIVLD bit is 0, the FCLKDIV register has not been written since the last reset. If the FCLKDIV register has not been written, any Flash program or erase command loaded during a command write sequence will not execute and the ACCERR bit in the FSTAT register will set.

5.40.4.3.2 Command Write Sequence

The Memory Controller will launch all valid Flash commands entered using a command write sequence.

Before launching a command, the ACCERR and FPVIOL bits in the FSTAT register must be clear (see Section 5.40.3.2.7, “Flash Status Register (FSTAT)") and the CCIF flag should be tested to determine the status of the current command write sequence. If CCIF is 0, the previous command write sequence is still active, a new command write sequence cannot be started, and all writes to the FCCOB register are ignored.

Writes to any Flash register must be avoided while a Flash command is active (CCIF=0) to prevent corruption of Flash register contents and Memory Controller behavior.

5.40.4.3.2.1 Define FCCOB Contents

The FCCOB parameter fields must be loaded with all required parameters for the Flash command being executed. Access to the FCCOB parameter fields is controlled via the CCOBIX bits in the FCCOBIX register (see Section 5.40.3.2.3, “Flash CCOB Index Register (FCCOBIX)").

The contents of the FCCOB parameter fields are transferred to the Memory Controller when the user clears the CCIF command completion flag in the FSTAT register (writing 1 clears the CCIF to 0). The CCIF flag will remain clear until the Flash command has completed. Upon completion, the Memory Controller will return CCIF to 1 and the FCCOB register will be used to communicate any results. The flow for a generic command write sequence is shown in Figure 107.

Table 457. P-Flash Commands

FCMD	Command	Function on P-Flash Memory
0x0B	Unsecure Flash	Supports a method of releasing MCU security by erasing all P-Flash (and D-Flash) blocks and verifying that all P-Flash (and D-Flash) blocks are erased.
0x0C	Verify Backdoor Access Key	Supports a method of releasing MCU security by verifying a set of security keys.
0x0D	Set User Margin Level	Specifies a user margin read level for all P-Flash blocks.
0x0E	Set Field Margin Level	Specifies a field margin read level for all P-Flash blocks (special modes only).

5.40.4.3.5 D-Flash Commands

Table 458 summarizes the valid D-Flash commands along with the effects of the commands on the D-Flash block.

Table 458. D-Flash Commands

FCMD	Command	Function on D-Flash Memory
0x01	Erase Verify All Blocks	Verify that all D-Flash (and P-Flash) blocks are erased.
0x02	Erase Verify Block	Verify that the D-Flash block is erased.
0x08	Erase All Blocks	Erase all D-Flash (and P-Flash) blocks. An erase of all Flash blocks is only possible when the FPLDIS, FPHDIS, and FPOPEN bits in the FPROT register and the DPOPEN bit in the DFPROT register are set prior to launching the command.
0x09	Erase Flash Block	Erase a D-Flash (or P-Flash) block. An erase of the full D-Flash block is only possible when DPOPEN bit in the DFPROT register is set prior to launching the command.
0x0B	Unsecure Flash	Supports a method of releasing MCU security by erasing all D-Flash (and P-Flash) blocks and verifying that all D-Flash (and P-Flash) blocks are erased.
0x0D	Set User Margin Level	Specifies a user margin read level for the D-Flash block.
0x0E	Set Field Margin Level	Specifies a field margin read level for the D-Flash block (special modes only).
0x10	Erase Verify D-Flash Section	Verify that a given number of words starting at the address provided are erased.
0x11	Program D-Flash	Program up to four words in the D-Flash block.
0x12	Erase D-Flash Sector	Erase all bytes in a sector of the D-Flash block.

5.40.4.4 Allowed Simultaneous P-Flash and D-Flash Operations

Only the operations marked ‘OK’ in Table 459 are permitted to be run simultaneously on the Program Flash and Data Flash blocks. Some operations cannot be executed simultaneously because certain hardware resources are shared by the two memories. The priority has been placed on permitting Program Flash reads while program and erase operations execute on the Data Flash, providing read (P-Flash) while write (D-Flash) functionality.

Table 459. Allowed P-Flash and D-Flash Simultaneous Operations

	Data Flash				
Program Flash	**Read**	**Margin Read(227)**	**Program**	**Sector Erase**	**Mass Erase(229)**
Read		OK	OK	OK	
Margin Read(227)		OK(228)			
Program					
Sector Erase				OK	